Analysis of Lag Phenomena and Current Collapse in Field-Plate AlGaN/GaN HEMTs with High-*k* Passivation Layer

K. Komoto, Y. Saito, and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan, horio@sic.shibaura-it.ac.jp

ABSTRACT

We study how a high-*k* passivation layer affects lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs. The drain lag, gate lag and current collapse appear as the drain current reduction ΔI_D from the steady state drain current I_D. So, we evaluate the current reduction rate $\Delta I_D/I_D$ as functions of field-plate length L_{FP}, passivation-layer thickness T_i and its relative permittivity ε_r. We plot $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse as a function of T_i. Then it is found that the drain lag and current collapse curves take minimum values depending on ε_r. When ε_r is 7, the minimum occurs at T_i = 0.03 μm. When ε_r is 20, 30 and 50, the minimum occurs at T_i = 0.1 μm, 0.1 μm, and 0.2 μm, respectively. Therefore, at the minimum, the value of ε_r/T_i, which is proportional to the capacitance, becomes nearly constant around 250±50/μm between ε_r = 7 and 50. In this condition for T_i, the lags and current collapse are reduced when L_{FP} becomes long for all ε_r.

Keywords: GaN, HEMT, current collapse, field plate, high-*k* passivation layer, buffer layer

1 INTRODUCTION

In AlGaN/GaN HEMTs, slow current transients are often observed even if the gate voltage or the drain voltage is changed abruptly [1]. This is called gate lag or drain lag, and is problematic for circuit applications. The slow transients mean that dc *I-V* curves and RF *I-V* curves become quite different, resulting in lower RF power available than that expected from the dc operation [2]. This is called current collapse. These are serious problems, and many experimental works are reported [1-5], and several theoretical works are made [5-10]. In previous theoretical works, the semi-insulating buffer is treated as undoped, and a deep donor and a deep acceptor are considered in it [6, 7], and the effects of a field plate on buffer-related lags and current collapse are also studied [9, 10]. Recently, a Fe-doped semi-insulating buffer layer is often adopted, and Fe acts as a deep acceptor [11, 12]. Then, some theoretical works regarding current collapse including the Fe-doped semi-insulating buffer layer are also made [13, 14]. By the way, recently, it is reported that introducing a high-*k* passivation layer can improve the breakdown voltage of AlGaN/GaN HEMTs [15, 16]. However, few or no works have not been reported on how the high-*k* passivation layer affects the lag phenomena. Therefore, in this work, we analyze how the high-*k* passivation layer affects the lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs.

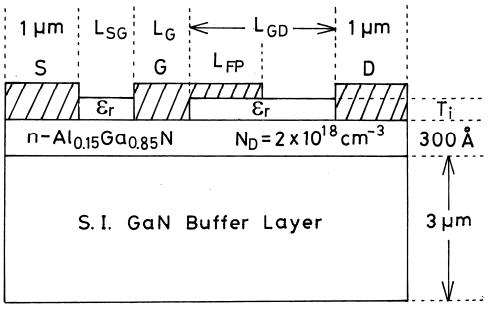

Figure 1: Device structures analyzed in this study.

2 PHYSICAL MODELS

Figure 1 shows a modeled device structure analyzed in this study. The gate length L_G 0.3 μm and the gate-to-drain distance L_{GD} is set to1.5 μm. The field-plate length L_{FP} is varied between 0 and 1 μm. The thickness of passivation layer T_i is also varied between 0.01 μm and 0.4μm, and its relative permittivity ε_r is varied between 7 and 50. As a buffer layer, we consider a Fe-doped semi-insulating buffer layer. The Fe level (E_{DA}) is set 0.5 eV below the bottom of conduction band [11, 12], and it is considered to be a deep acceptor. In this case, the deep acceptors act as electron traps. The deep-acceptor density is set to 10^{17} cm^{-3}.

Basic equations to be solved are Poisson's equation including ionized deep-acceptor terms, continuity equations for electrons and holes which include carrier loss rates via the deep acceptor and rate equations for the deep acceptor [7, 17-19]. These are expressed as follows.

1) Poisson's equation

$$\nabla \bullet (\varepsilon \nabla \psi) = -q(p - n + N_D - N_{DA}^-) \quad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - R_{n,DA} \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - R_{p,DA} \quad (3)$$

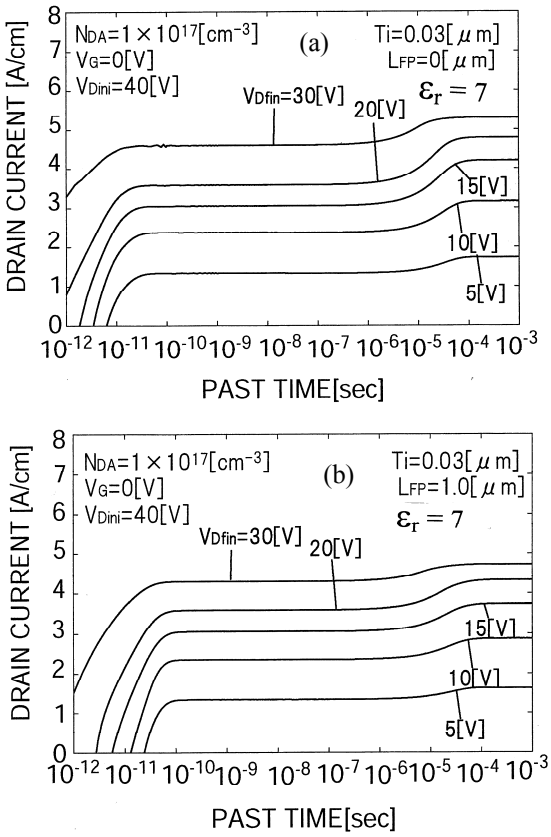

Figure 2: Calculated drain-current responses when V_D is lowered from 40 V to respective voltage. T_i = 0.03 μm and ε_r = 7. (a) L_{FP} = 0, (b) L_{FP} = 1 μm.

where

$$R_{n,\mathrm{DA}} = C_{n,\mathrm{DA}}(N_{\mathrm{DA}} - N_{\mathrm{DA}}^-)n - e_{n,\mathrm{DA}}N_{\mathrm{DA}}^- \qquad (4)$$

$$R_{p,\mathrm{DA}} = C_{p,\mathrm{DA}}N_{\mathrm{DA}}^- p - e_{p,\mathrm{DA}}(N_{\mathrm{DA}} - N_{\mathrm{DA}}^-) \qquad (5)$$

3) Rate equation for the deep acceptor

$$\frac{\partial}{\partial t}N_{\mathrm{DA}}^- = R_{n,\mathrm{DA}} - R_{p,\mathrm{DA}} \qquad (6)$$

where N_{DA}^- represents the ionized deep-acceptor density. $C_{n,\mathrm{DA}}$ and $C_{p,\mathrm{DA}}$ are the electron and hole capture coefficients of the deep acceptor, respectively, $e_{n,\mathrm{DA}}$ and $e_{p,\mathrm{DA}}$ are the electron and hole emission rates of the deep acceptor, respectively. These are given as functions of the deep acceptor's energy level and the capture cross sections.

These basic equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

3 RESULTS AND DISCUSSIONS

Fig.2 shows calculated drain current responses of AlGaN/GaN HEMTs (a) without and (b) with a field plate when V_D is changed abruptly from V_{Dini} = 40 V to the respective voltage V_{Dfin}. Here V_G is not changed at 0 V.

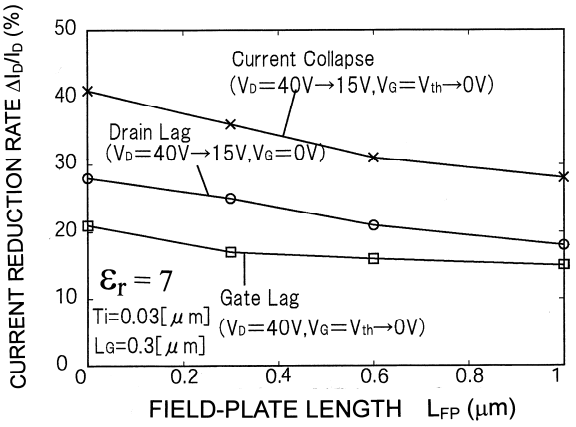

Figure 3: Current reduction rate $\Delta I_D/I_D$ due to date lag, gate lag, and current collapse as a function of the gate length L_{FP}. T_i = 0.03 μm and ε_r = 7.

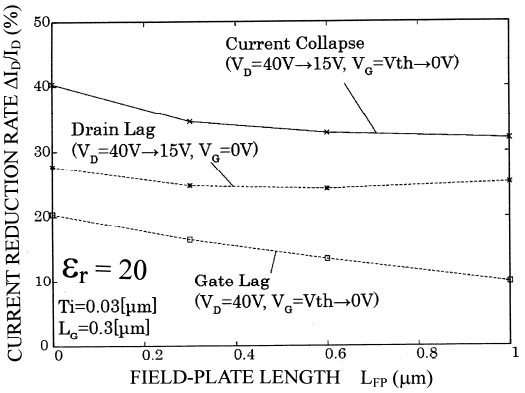

Figure 4: Current reduction rate $\Delta I_D/I_D$ due to date lag, gate lag, and current collapse as a function of the gate length L_{FP}. T_i = 0.03 μm and ε_r = 20.

Here ε_r = 7 (SiN) and T_i = 0.03 μm. The drain current I_D remains a low value for some periods, and begins to increase gradually, showing drain lag. It is understood that I_D begins to increase when the deep acceptors in the buffer layer begin to emit electrons. When the turn-on characteristics are calculated, slow transients are also observed, showing gate lag and current collapse. The current collapse is a combined effect of drain lag and gate lag. Fig.3 shows current reduction rate $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse at T_i = 0.03 μm and ε_r = 7. It is seen that the lags and current collapse are reduced as L_{FP} becomes long.

Fig.4 shows $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse when T_i = 0.03 μm and ε_r = 20. In this case, the drain lag is not reduced even if L_{FP} becomes long. We will discuss below why this happens. Fig.5 shows $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse as a function of T_i. Here L_{FP} = 1 μm. Fig.5(a) shows the case of ε_r = 7, and Fig.5(b) shows the case of ε_r = 20. When ε_r = 7, the drain-

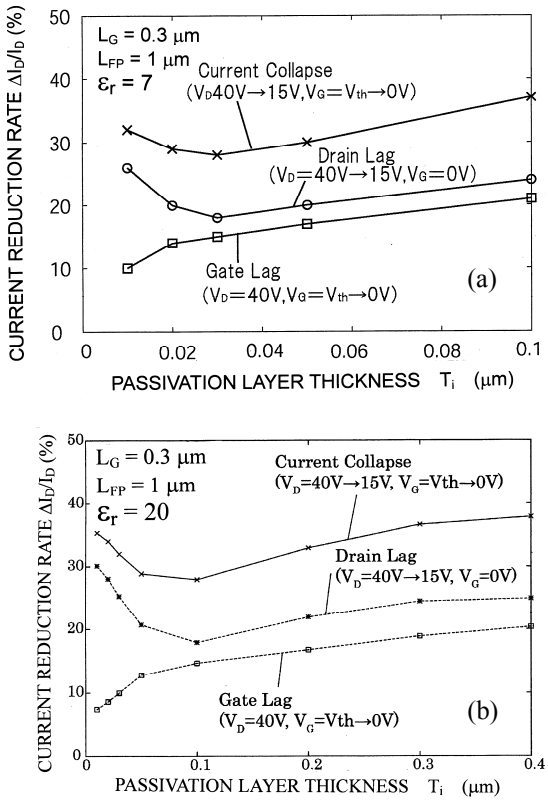

Figure 5: Current reduction rate $\Delta I_D/I_D$ due to date lag, gate lag, and current collapse as a function of T_i. L_{FP} = 1 μm. (a) ε_r = 7, (b) ε_r = 20.

lag rate takes a minimum value at T_i = 0.03 μm. But, when ε_r = 20, it takes a minimum value at T_i = 0.1 μm and it is rather large at T_i = 0.03 μm. This may be because the field plate acts like a gate electrode when T_i = 0.03 μm and ε_r = 20. Fig.6 shows $\Delta I_D/I_D$ versus L_{FP} curves when T_i = 0.1 μm and ε_r = 20. In this case, the lags and current collapse are reduced when L_{FP} becomes long, as in Fig.3.

Fig.7 shows $\Delta I_D/I_D$ versus T_i curves for (a) ε_r = 30 and (b) ε_r = 50 where L_{FP} = 1 μm. In the case of ε_r = 30, the drain-lag rate and the current-collapse rate take minimum values at T_i = 0.1 μm, and they take minimum values at T_i = 0.2 μm when ε_r = 50. Therefore, as ε_r increases, the value of T_i becomes thick when the drain lag and current collapse become minimum. In the case where they are minimum, the values of ε_r/T_i become about 233/μm, 200/μm, 300/μm and 250/μm, respectively when ε_r is 7, 20, 30 and 50. It is concluded that when the drain-lag rate and the current-collapse rate take minimum values, the values of ε_r/T_i which is proportional to the capacitance of the passivation layer become nearly constant around 250±50/μm between ε_r = 7 and 50. Although not shown here, in this condition for T_i, the lags and current collapse are reduced in the cases of ε_r = 30 and 50 when L_{FP} becomes long, as are similar to Figs.3 and 6.

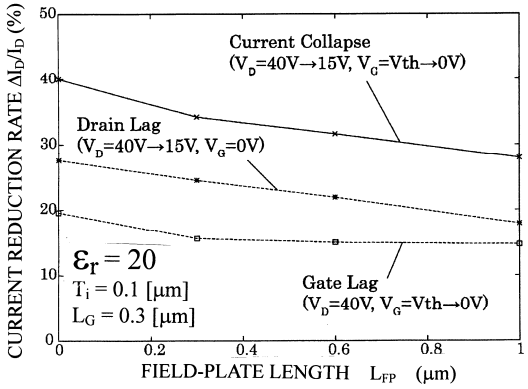

Figure 6: Current reduction rate $\Delta I_D/I_D$ due to date lag, gate lag, and current collapse as a function of L_{FP}. T_i = 0.1 μm and ε_r = 20.

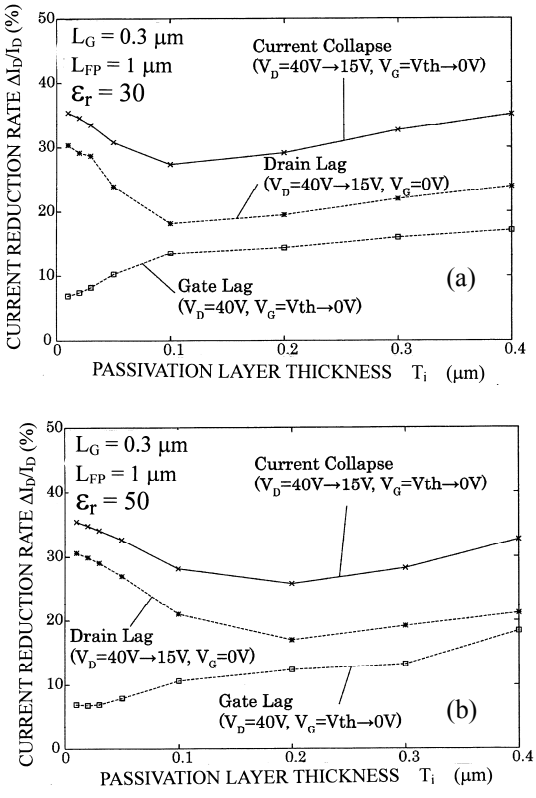

Figure 7: Current reduction rate $\Delta I_D/I_D$ due to date lag, gate lag, and current collapse as a function of T_i. L_{FP} = 1 μm. (a) ε_r = 30, (b) ε_r = 50.

4 CONCLUSION

It has been studied how the current reduction rate $\Delta I_D/I_D$ due to drain lag, gate lag and current collapse in field-plate AlGaN/GaN HEMTs are affected by field-plate length L_{FP}, passivation-layer thickness T_i and its relative permittivity ε_r. We have plotted the drain-lag rate, gate-lag rate and current-collapse rate as a function of T_i. Then it has been

found that the drain-lag rate and the current-collapse rate take minimum values depending on ε_r. When ε_r is 7, the minimum occurs at T_i = 0.03 μm. When ε_r is 20, 30 and 50, the minimum occurs at T_i = 0.1 μm, 0.1 μm, and 0.2 μm, respectively. Therefore, at the minimum, the value of ε_r/T_i, which is proportional to the capacitance of the passivation layer, becomes nearly constant around 250±50/μm between ε_r = 7 and 50. In this condition for T_i, the lags and current collapse are reduced when L_{FP} becomes long for all ε_r considered here.

REFERENCES

[1] S. C. Binari, P. B. Klein and T. E. Kazior, "Trapping effects in GaN and SiC Microwave FETs", Proc. IEEE, vol.90, pp.1048-1058, 2002.

[2] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers", Proc. IEEE, vol.96, pp.287-305, 2008.

[3] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rarnpazzo, A. Chini, U. K. Mishra, C. Canali and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN/GaN HEMTs", IEEE Trans. Electron Devices, vol.51, pp.1554-1561, 2004.

[4] A. Koudymov, V. Adivarahan, J, Yang, G. Simon and M. A. Khan, "Mechanism of current collapse removal in field-plated nitride HFETs", IEEE Electron Device Lett., vol.26, pp.704-706, 2005.

[5] J. Tirado, J. L. Sanchez-Rojas and J. I. Izpura, "Trapping Effects in the transient response of AlGaN/GaN HEMT devices", IEEE Trans. Electron Devices, vol.54, pp.410-417, 2007.

[6] K. Horio, K. Yonemoto, H. Takayanagi and H. Nakano, "Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors" J. Appl. Phys., vol.98, pp.124502 1-7, 2005.

[7] K. Horio and A. Nakajima, "Physical mechanism of buffer-related current transients and current slump in AlGaN/GaN high electron mobility transistors", Jpn. J. Appl. Phys., vol.47, pp.3428-3433, 2008.

[8] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, and F. Fantini, "Investigation of high-electric-field degradation effects in AlGaN/GaN HEMTs", IEEE Trans. Electron Devices, vol.55, pp.1592-1602, 2008.

[9] K. Horio, A. Nakajima, and K. Itagaki, "Analysis of field-plate effects on buffer-related lag phenomena and current collapse in GaN MESFETs and AlGaN/GaN HEMTs", Semicond. Sci. Technol., vol.24, pp.085022-1–085022-7, 2009.

[10] K. Horio, H. Onodera, and A. Nakajima, "Analysis of backside-electrode and gate-field-plate effects on buffer-related current collapse in AlGaN/GaN high electron mobility transistors", J. Appl. Phys., vol.109, pp.114508-1–114508-7, 2011.

[11] M. Silvestri, M. J. Uren and M. Kuball, "Iron-induced deep-acceptor center in GaN/AlGaN high electron mobility transistors: Energy level and cross section", Appl. Phys. Lett., vol.102, pp.073051-1–073501-4, 2013.

[12] Y. S. Puzyrev, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Role of Fe impurity complexes in the degradation of GaN/AlGaN high-electron mobility transistors", Appl. Phys. Lett., vol.106, pp.053505-1–053505-4, 2015.

[13] R. Tsurumaki, N. Noda and K. Horio, "Similarities of lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with different types of buffer layers", Microelectronics Reliability, vol.73, pp.36-41, 2017.

[14] Y. Saito, R. Tsurumaki, N. Noda and K. Horio, "Analysis of reduction in lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with high acceptor density in a buffer layer", IEEE Trans. Device Mater. Rel., vol.18, no.1, pp.46-53, 2018.

[15] H. Hanawa, H. Onodera, A. Nakajima, and K. Horio, "Numerical analysis of breakdown voltage enhancement in AlGaN/GaN HEMTs with a high-*k* passivation layer", IEEE Trans. Electron Devices, vol.61, pp.769-775, 2014.

[16] T. Kabemura, S. Ueda, Y. Kawada, and K. Horio, "Enhancement of breakdown voltage in AlGaN/GaN HEMTs: Field plate plus high-*k* passivation layer and high acceptor density in buffer layer", IEEE Trans. Electron Devices, vol.65, no.9, pp.3848-3854, 2018.

[17] K. Horio, A. Wakabayashi and T. Yamada, "Two-dimensional analysis of substrate-trap effects on turn-on characteristics in GaAs MESFET's", IEEE Trans. Electron Devices, vol.47, pp.617-624, 2000.

[18] A. Wakabayashi, Y. Mitani and K. Horio, "Analysis of gate-lag phenomena in recessed-gate and buried-gate GaAs MESFETs", IEEE Trans. Electron Devices, vol.49, pp.37-41, 2002.

[19] A. Nakajima, K. Fujii and K. Horio, "Numerical analysis of buffer-trap effects on gate lag in AlGaN/GaN high electron mobility transistors", Jpn. J. Appl. Phys., vol.50, pp.104303-1–104303-6, 2011.