Graphene Based Field Effect Transistor Analog/RF Performance Analysis from Non-equilibrium Green's Function Simulation

Yuqin Chen, Jin He, Chunlai Li, Xiaomeng He, Pan Jun, Guojing Hu, Jingjing Liu, Yuan Ren, and Xiaomeng Ma

SoC Key Laboratory, Peking University Shenzhen Institute and PKU-HKUST Shenzhen-Hong Kong Institution, Shenzhen, China, frankhe@pku.edu.cn

ABSTRACT

Based on the non-equilibrium Green's function simulation, the Graphene Field Effect Transistor (GFET) analog/RF performance including the trans-conductance efficiency gm/Id, cutoff frequency ft, and maximum oscillation frequency fmax are analyzed in details. The analysis method is described and the GFET analog/RF performance dependence on the operation bias, device parameter, and gate oxide thickness are demonstrated. These results will be useful for the device scientists and circuit engineers to optimize the GFET structure and improve its circuit performance for the potential analog/RF application in near future.

Keywords: Graphene field effect transistor, GFET, Analog/RF performance, Green function simulation, energy band.

1 INTRODUCTION

With the rapid scalding of MOSFET channel length beyond 10nm generation, many kinds of new semiconductor device structures are proposed to be the replacement of the traditional silicon structure for the fundamental limitations [1-2]. Among them, the graphene based represent a promising alternative for future nanoelectronics due to their unique advantages such as ideal scalability, tunable band gap, strong covalent bonding, high-speed carriers, high group velocity, possible ballistic transport, and high thermal conductivity [3]. While graphene is an ideal candidate for use in fRF-FETs, because it offers both exceptional electronic properties (room temperature mobility in excess of 110,000 cm2/ V/s and saturation velocity of 1-5 x10^7/ cm), as well as outstanding mechanical performance (strain limits up to 25%) [4-13]. However, there has a little report on analysis of the analog/RF performance of GFET so far.

In this paper, the analog/RF figures of the GFET are discussed from the non-equilibrium Green's function simulation. The dependence of the trans-capacitances, cutoff frequency, and maximum oscillation frequency of the GFETs on the operation bias, device parameter, and gate oxide thickness are demonstrated. The organization of this paper is as follows: The simulation approach is first described. And then, its application in the GFETs is demonstrated, from it, the comparisons of analog/RF performance of coaxial GFETs of different structures are obtained and analyzed. A summary concludes the paper.

2 SIMULATION OF GFETS

The non-equilibrium Green's function (NEGF) formalism provides a sound basis for atomic-level quantum mechanical simulation [11]. In this study, a high-K carbon nanotube field effect transistor (GFET) shown in Fig.1 is considered. As done in common NEGF formulation based device simulation [11], one can take GFET as a device connected to the contacts where some charge is transferred into or out of the device. Through the self-consistently iterative solution between the Poisson equation and Schrödinger equation, the potential and electron density are obtained.

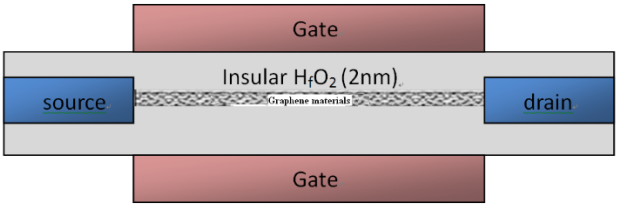
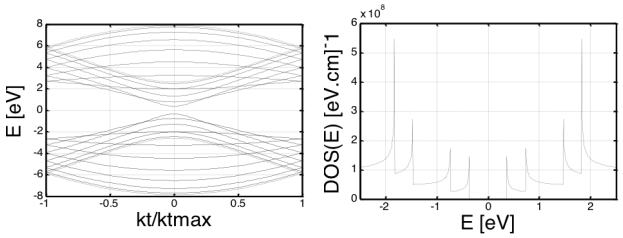


Fig.1 Sketch of the device structure of GFET, the channel length is 10nm, the doping concentration of the source/drain is 10^{20}/cm, the oxide is H_fO_2 with a dielectric constant of k=17.3 and oxide thickness t_{ox}=2nm.



(a) (b)

Fig.2 (a) The energy band of semi-conducting Graphene film based on Ultra-GFET. (b) The density of states of Graphene film based on Ultra-GFET.

According to the energy band structure and the density of states given by the Ultra-GFET simulator [13] as shown in Fig.2, we take the effective mass model [10-12] to describe the conduction band property. For the effect of the contact on device, self energy is introduced in Hamiltonian matrix to describe the connection [13]. The Green's function formulation is written as:

$$G = [(E + i\eta) - H - \sum]^{-1} \approx [EI - H - \sum] \quad (1)$$

Where $\sum = \tau g_R \tau^+$, $g_R = [(E + i\eta)I - H_R]^{-1}$

Based on this formulation, we use the eigenstate representation for the transverse dimension and a discrete real

space lattice for the longitudinal direction so the overall Hamiltonian H is separated into a longitudinal part H_L and a transverse part H_T (x axis stands for the longitudinal direction, polar coordinates is taken in cross section):

$$H_L = E_C - \frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} \quad U(x) \tag{2}$$

$$H_T = -\frac{\hbar^2}{2m^*}\left(\frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r}\right) + U_t(r,\theta) \tag{3}$$

Here, m^* stands for the effective mass.

To dialogize the Hamiltonian matrix, introduce the two variables: $\Gamma_1 = i(\Sigma_1 - \Sigma_1^+)$, $\Gamma_2 = i(\Sigma_2 - \Sigma_2^+)$. The eigenstate of contact-device-contact structure is divided into two groups associated with wave incident from the left and the right contacts respectively, which remain in equilibrium with the responding contact, thus, the density is written as:

$$\rho_k = \int \frac{dE}{2\pi}[f_0(E+\varepsilon_k-\mu_1)A_1 + f_0(E+\varepsilon_k \quad {}_2)A_2] \tag{4}$$

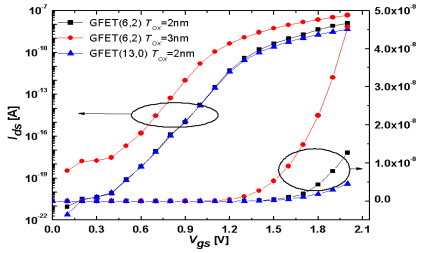
Where $A_1 = G\Gamma_1 G^{=}, A_2\Gamma \quad G \quad {}_2G^+$

From these results, the density matrix is calculated by solving Poisson's equation self-consistently with the law of equilibrium mechanics described above. Once getting the density matrix, the current is obtained:

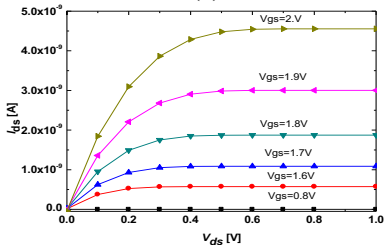
$$I = (-q)Trace(\rho J_{op}) \tag{5}$$

Where J_{op} is the current operator .

We apply the method described above to the GFETs to get the numerical simulation results. Fig.3 (a) and (b) plot the NEGF simulation result for the current-voltage characteristics of different chiral GFETs. It is found from Fig.3 that the electronic characteristics of GFET are similar to the traditional silicon MOSFETs not only for I_{ds} versus V_{gs} curves, but also for I_{ds} versus V_{ds} curves. It also shows that GFET (6,2) has a higher current response to same gate bias compared to GFET(13,0).



(a)



(b)

Fig.3. I-V results for GFET (6,2) and GFET(13,0) using NEGF simulation. (a) I_{ds}-V_{gs} with V_{ds}=0.6V and V_{gs} varied from 0V to 2V in steps of 0.1V. (b) I_{ds}-V_{ds} results of GFET (13,0) with V_{gs} varied from 0.8V to 2.0V.

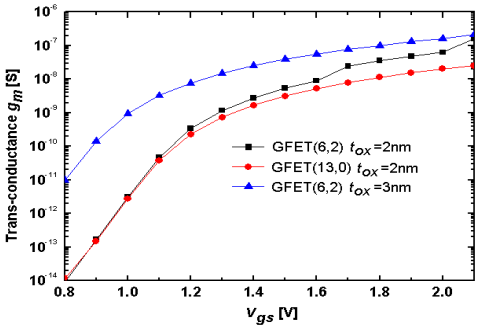
Based on the current-voltage and charge-voltage characteristics obtained from the NEGF simulation, we can further to calculate the corresponding large and small signal parameters such as g_m, g_{ds}, and trans-capacitances. From these results, the analog/RF performance of the GFET can be analyzed as shown in the following section.

3 GFET ANALOG/RF PERFORMANCE

3.1 Analog performance

From the simulation results got in section II, including the relation between I_{ds} and V_{gs}, I_{ds} and V_{ds}, carrier distribution in carbon nanotube and other key figures, we can calculate the important parameters of analog performance and discuss the related figures in the GFET structures.

The significant figures of GFET for analog integrated circuits include the trans-conductance g_m, the output conductance g_d, intrinsic gain g_m/g_d, and the g_m/I_{ds} ratio. Among these, the g_m/I_{ds} ratio stands for the efficiency to translate current into trans-conductance. The greater it is, the larger trans-conductance it can obtain at a constant current value [7]. While intrinsic gain g_m/g_d is used as a measure of the performance of operational amplifiers.



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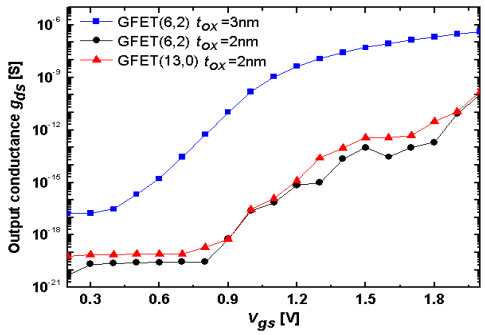

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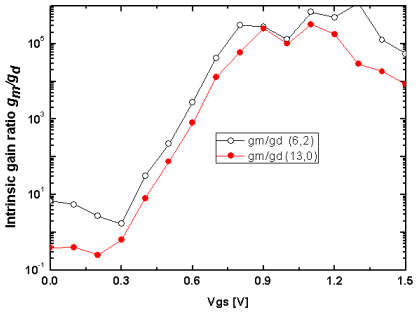


(c)

Fig.4 (a) transconductance g_m and (b) output conductance g_d as a function of gate overdrive voltage in CNEFET (6,2) and GFET(13,0). (c) Intrinsic gain ratio (g_m/g_d) in GFET (6,2) and GFET(13,0), at drain bias of 0.6V.

Fig.4(a) shows that the trans-conductance g_m of GFET (6,2) rises faster with gate voltage than that of GFET(13,0) for the higher gate control capability. It also reflects that the greater the thickness of oxide is, the larger g_m becomes, similar to silicon based device. The comparison of output conductance g_d is shown in Fig.4 (b). Thicker oxide leads higher g_d. In low gate voltage, the g_d of GFET(13,0) is larger than that of GFET(6,2). This reflects higher carrier mobility of GFET(13,0). But as the gate bias increased, g_d of two types become close together. Fig.4(c) illustrates the intrinsic gain of two kinds of GFETs. It is obvious that the intrinsic gain of GFET(6,2) is higher out of better g_m. On the other hand, they both present a peak during the increase of gate voltage, while at higher gate voltage their intrinsic gain begins to decline with the increase of g_d.

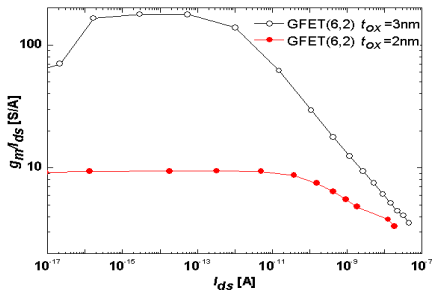
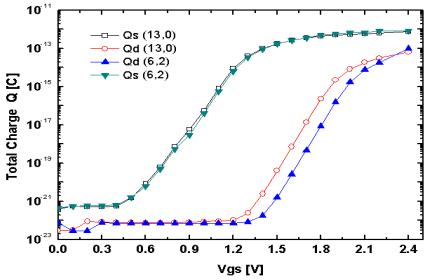


Fig.5 g_m/I_{ds} ratio as a function of the drain current in the GFET(6,2) at drain bias of 0.6V.

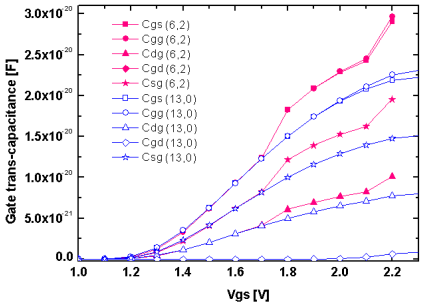
Another parameter of importance in analog circuits: the g_m/I_{ds} ratio is shown in Fig 5. As gate voltage changes, it is controlled by different parameters. In low gate bias, it increases as $V_{gs,}$ increases, it is the gate control capability that dominates the value of g_m/I_{ds}. While in high gate bias, the g_m/I_{ds} descends by the drain current. It is obvious that g_m/I_{ds} of GFET with 3nm thick oxide is larger than GFET of 2nm thick oxide in some range of I_{ds} .

In the quasi-static model, the capacitance effects of the drain and source on the gate are discussed so a nine-capacitance matrix is given [5]. Settled by related analysis and discussion [6], the last expressions of capacitances only contain inversion charge density solved in simulation of section II. In this way, trans-capacitances are calculated.

Fig.6(a) shows the total charge in source terminal and drain terminal of GFETs from NEGF simulation. The charge density changes as the gate bias increases, nearly the same as normal MOSFET in subthreshold and strong inversion region. At the beginning, the charge density in the drain of GFET (13,0) is greater than that in GFET(6,2), while under large gate bias, they become close both in source and drain.



(a)



(b)

Fig.6. (a) Charge distribution as a function of gate voltage in source and drain of GFET(6,2) and GFET(13,0), at drain bias of 0.6V. (b) Trans-capacitance as a function of gate voltage changing from 1V to 2.2V in step of 0.1V, at drain bias of 0.6V.

With these results, trans-capacitances are obtained, illustrated in Fig.6.(b). It is obvious that increasing gate voltage brings larger capacitances in some area. According to the comparison of two different GFETs, the capacitances of GFET(6,2) are clearly larger than those of GFET(13,0) when gate voltage increases.

3.2 High frequency performance

Based on the results given above, the key parameters of high frequency performance containing the cutoff frequency f_t and the maximum frequency of oscillation f_{max} are discussed. f_t stands for the transition frequency at which the current gain is unity. f_t is decided by the ratio of trans-conductance to capacitance:

$$f_t \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (6)$$

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Fig.7 reflects the trend of f_t with the change of drain current for GFET(6,2) and GFET(13,0). It shows the excellent high frequency performance of GFETs. f_t of GFET(6,2) is higher than that of GFET(13,0) due to the higher g_m. As well, it illustrates that f_t begins to decline when drain current is high enough. This is because in early period, f_t can be increased together with V_{gs}, however, when V_{gs} is large enough, the saturation voltage V_{ds} takes effect so that the effect of V_{gs} diminishes and f_t declines.

f_{max} is the maximum frequency of oscillation, at which the ratio of the load power to the input power is unity.

$$f_{\max} \approx \frac{g_m / (2\pi C_{gs})}{2\sqrt{R(g_{ds} + g_m \frac{C_{gd}}{C_{gd}})}} \quad (7)$$

Here, we set the extrinsic resistance R =12.5k Ω [8].

Fig.8 shows the trend of f_{max} in different I_{ds}. Both the f_t and f_{max} have a peak during the increase of gate voltage, because in high gate voltage, the trans-capacitance increase much more compared to the increase of g_m and g_d.

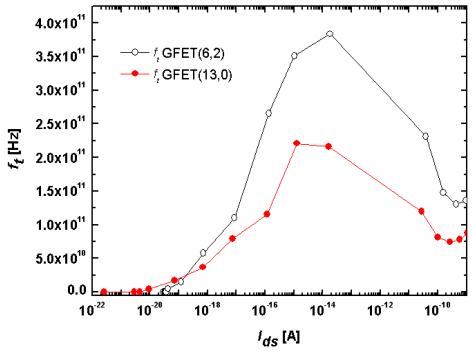

Fig.7. Cutoff frequency (f_t) as a function of drain current in GFET(6,2) and GFET(13,0), at drain bias of 0.6V.

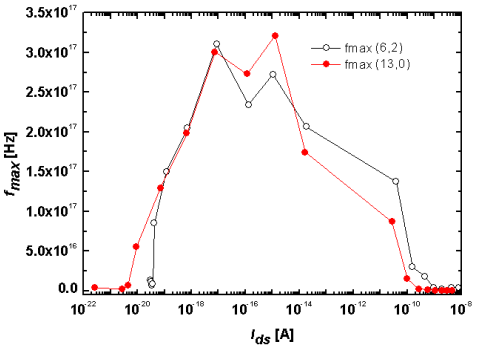

Fig.8. Maximum oscillation frequency (f_{max}) as a function of drain current I_{ds} in GFET(6,2) and GFET(13,0) at drain bias of 0.6V.

4 CONCLUSION

In this paper, the grapheme base field effect transistor analog/RF performance including the high trans-conductance efficiency g_m/I_{ds}, trans-capacitances, cutoff frequency f_t and maximum frequency of oscillation f_{max} are studied from different device geometry and CNT material characteristics. It shows that the high frequency performance of GFET(6,2) is better than GFET(13,0) although its trans-capacitances may be larger. These predicted results indicate that GFET is an excellent successor to silicon and the coaxial GFET is likely to operate excellently.

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REFERENCES

[1] A.K.GeimandK.S.Novoselov,"The rise of graphene," Nature Mater., vol. 6, no. 3, pp. 183–191, 2007.

[2] X.Li, et al.,"Large area synthesis of high-quality and u niform graphene films on copper foils," Science, vol. 324, no. 5932, pp. 1312–1314, 2009.

[3] W. Mehr, et al.,"Vertical graphene base transistor," IEEE Electron Device Lett., vol. 33, no. 5, pp. 691–693, May 2012.

[4] V. Di Lecce, et al.,"Graphene-base heterojunction transistor: An attractive device for terahertz operation," IEEE Trans. Electron Devices, vol. 60, no. 12, pp. 4263–4268, 2013.

[5] Q. Zhang, G. Fiori, and G. Iannaccone, "On transport in vertical graphene heterostructures," Electron Device Letters, IEEE, vol.35, no.9, pp. 966–968, Sept 2014.

[6] S. Venica, F. Driussi, P. Palestri, and L. Selmi, "Backscattering and common-base current gain of the Graphene Base Transistor (GBT)," Microelectronic Engineering, vol. 147, no. 0, pp. 192 – 195, 2015.

[7] S. Vaziri, et al.,"graphene-based hot electron transistor," Nano Lett., vol. 13, no. 4, pp. 1435–1439, 2013.

[8] C. Zeng, et al.,"Vertical graphene-base hot-electron transistor," Nano Lett., vol. 13, no. 6, pp. 2370–2375, 2013.

[9] D. Sinha and J. U. Lee, "Ideal Graphene/Silicon Schottky Junction Diodes," Nano Letters, vol. 14, no. 8, pp. 4660–4664, 2014.

[10] S. Riazimehr, et al., "Spectral sensitivity of a graphene/silicon pn-junction photodetector," in Ultimate Integration on Silicon (EUROSOI-ULIS), 2015 Joint International EUROSOI Workshop and International Conference on, Jan 2015, pp. 77–80.

[11] G. Fisichella, et al.,"Current transport in graphene/AlGaN/GaN vertical heterostructures probed at nanoscale," Nanoscale, vol. 6, pp. 8671–8680, 2014.

[12] V. Di Lecce, et al.,"Impact of crystallographic orientation and impurity scattering in graphene-base heterojunction transistors for terahertz operation," in 2014 44th European Solid State Device Research Conference (ESSDERC), Sept 2014, pp. 313–316.

[13] Y. Tao, X. Zhang, T. Y. Man, Molecule Simulation, vol.45,p.73,2018.