Improved Electric Field Decomposition Capacitance Model with 3-D Terminal and Fringe Components in Sub-28nm Interconnect

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Abstract

In this paper, a parasitic capacitance model for a finite single three-dimensional (3-D) wire above an infinite plate in the nano-scale 3-D integrated circuit application is developed based on electric field decomposition (EFD). The capacitance components at wire ends, i.e., the 3-D terminal and terminal fringe capacitance, are considered by the 3-D electric field analysis. Verified by extensive COMSOL simulations, the model can accurately predict parasitic capacitance for a wide range of 3-D BEOL wire dimensions in the beyond 28nm CMOS process technology.

Keywords: Capacitance model; 3-D terminal; terminal fringe; electric field decomposition; 3-D interconnect, TSV process.

I. INTRODUCTION

The parasitic capacitance of back-end-of-the-line (BEOL) interconnect wires is increasing dramatically, emerging as a limiting factor to the circuit performance in the three-dimensional (3D) integrated circuits with the advanced through silicon void (TSV) process [1, 2]. Compared to numerical approaches [3, 4], a model as function of wire dimensions is preferred for analyzing and optimizing purpose.

Previous capacitance modeling works mainly focused on two-dimensional (2-D) cases [5-9, 11, 12], using either overly simplified physical solutions [5-7], or empirical fitting process [7-9]. As for 3-D structures, models were usually roughly estimated as $C_{2\text{-D}}{\cdot}L$, so important components at wire ends were ignored. Thus, such approaches often underestimated 3-D wire parasitic capacitances, especially for those of short wires. As it will be shown, those 3-D native components constitute more than 15.8% of the total capacitance when wire length is smaller than ten times of wire width, which is often the case for local CMOS interconnects beyond 28nm CMOS process. Empirical fitting method was also extended to complicated 3-D interconnect wires [10], but it offers little physical insights for the circuit designers.

In this paper, the parasitic capacitance model is improved based on EFD [12] by modeling the native 3-D wire components, i.e., the 3-D terminal and terminal fringe capacitance. The model is verified by extensive COMSOL simulations. It indicates the wire ends play an important role in the total parasitic capacitance calculation, particularly for local short wires in the beyond 28nm CMOS process technology.

II. Capacitance Model Development

As shown in Fig. 1, C_{bottom} is the capacitance between a finite wire and an infinite plate. Based on EFD, the electric field of this 3-D structure is assigned into five major regions. The partition is verified by simulations. The three normal regions, i.e., the plate, fringe and terminal of the wire, are natural extensions of 2-D cases. The other two regions at wire ends are unique in 3-D cases, which are defined as followings.

1) 3-D terminal region: its electric field is from the terminal of two sidewalls and bottom plate to ground plate.

2) Terminal fringe region: its electric field is from the perpendicular wire terminal between two sidewalls to ground.

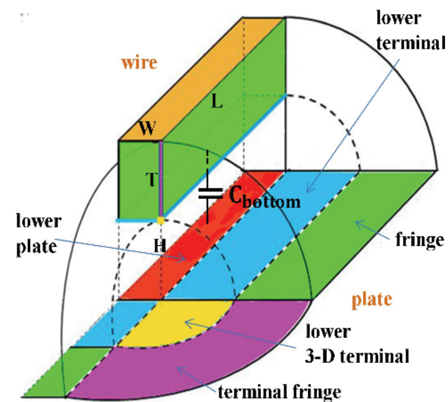

Fig. 1. Electric field decomposition of a 3-D single wire above a plate.

A. 2-D Terminal Capacitance Model Improvement

Different from fringe region as shown in Fig. 2 (a), the magnitude of electrical field of the terminal region increases as it gets closer to the terminal of the wire. Thus, deriving terminal capacitance as (3) in [12] overestimates its value. Though it then gives a rough deduction as (5), it is still not accurate especially when H is large.

A new method is used here. As shown in Fig. 2 (b), a camber capacitor with a radius $r_{2\text{-D}}$ and a central angle θ, which is approximately $\pi/2$, is used to model the terminal electric field. It is equivalent to half of the lower part of a

circle-over-plate capacitor, and the ratio of the lower terminal capacitance to the total circle capacitance is p_1.

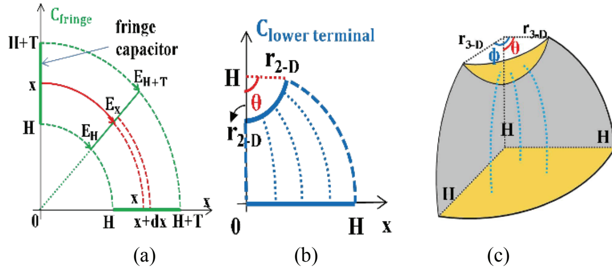

Fig. 2. (a) Fringe capacitance calculation. (b) Lower 2-D terminal capacitor mimicked by half of the lower part of a circle-over-plate capacitor. (c) Lower 3-D terminal capacitor mimicked by a capacitor of a quarter of the lower part of a sphere over an infinite plate.

$$\frac{C_{lower\ terminal}}{\varepsilon} = p_1 \frac{C_{circle}}{\varepsilon} = \frac{2 p_1 \pi}{\ln(2H/r_{2-D})} \quad (1)$$

$$\frac{C_{upper\ terminal}}{\varepsilon} = (1/2 - p_1)\frac{C_{circle}}{\varepsilon} = \frac{(1-2p_1)\pi}{\ln[2(H+T)/r_{2-D}]} \quad (2)$$

The radius $r_{2\text{-}D}$ is a function of wire dimensions, which can be estimated as $0.13W^{0.25}H^{0.6}T^{0.15}$ based on simulation results. Note that p_1 can be derived by the surface charge density distribution function of a circle-over-plate capacitor. For a wide range of wire dimensions, p_1 is limited between 0.26 and 0.29. For simplicity, p_1 is assigned as 0.275.

B. 3-D Terminal Capacitance Modeling

The 3-D lower terminal capacitor is substituted by a capacitor of a quarter of the lower part of a sphere over an infinite plate, as shown in Fig. 2 (c). Both the θ and φ are approximately $\pi/2$. The ratio of the lower 3-D terminal capacitance to the total sphere capacitance is p_2. The 3-D terminal capacitances are given accordingly in (3) and (4).

$$\frac{C_{lower\ 3-D\ terminal}}{\varepsilon} = p_2 \frac{C_{sphere}}{\varepsilon} = 4 p_2 \pi r_{3-D} (1 + \frac{r_{3-D}}{2H}) \quad (3)$$

$$\frac{C_{upper\ 3-D\ terminal}}{\varepsilon} = (\frac{1}{4} - p_2)\frac{C_{sphere}}{\varepsilon} = (1-4p_2)\pi r_{3-D}[1 + \frac{r_{3-D}}{2(H+T)}] \quad (4)$$

Again, $r_{3\text{-}D}$ is estimated as $0.15L^{0.15}W^{0.15}H^{0.4}T^{0.3}$ according to simulations, and for a wide range of wire dimensions, p_2 can be assigned as 1/8 for simplicity.

C. Terminal Fringe Capacitance Modeling

The electric field of the terminal fringe region is mimicked by that from a quarter of the sidewall of a perpendicular cylinder. To estimate the electric flux, the sidewall of the cone in Fig. 3 (a), which represents the equipotential surface, is flattened as Fig. 3 (b) for area infinitesimal calculation.

$$d(area) = \pi[(x+dx)^2 - x^2]\frac{\pi/2\, H \sin\theta}{2\pi H} = \frac{\pi}{2}\sin\theta\, x\, dx \quad (5)$$

The electric field is calculated as shown in Fig. 3 (c). Thus, the electric flux through the blue area can be integrated as below.

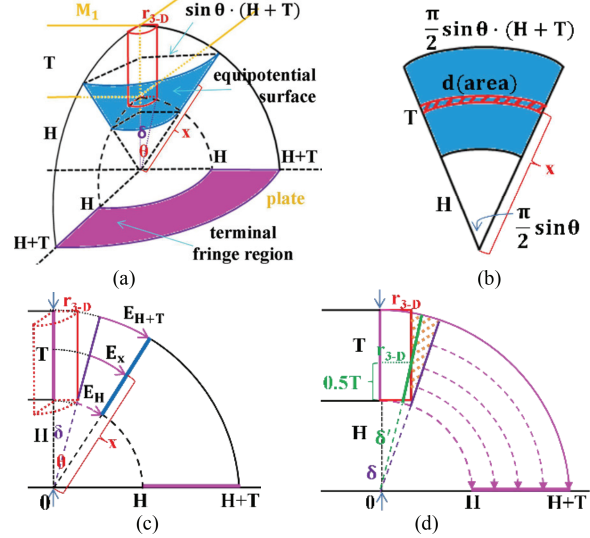

Fig. 3. (a) Equipotential surface for terminal fringe region, (b) Orthographic projection of the sidewall of the cone. (c) The equipotential surface in (a) can be obtained by rotating the blue line around the center axis in (c) by $\pi/4$. (d) Angle compensation.

$$\Phi = \int_H^{H+T} E_x d(area) = \int_H^{H+T} \frac{HE_H}{x} d(area) = \frac{\pi}{2}\sin\theta E_H HT \quad (6)$$

According to the Gaussian Law,

$$\int_\delta^{\frac{\pi}{2}} E_H H\, d\theta = V = \frac{Q/4}{C} = \frac{\varepsilon\Phi}{C}, \quad (7)$$

where $\delta \approx r_{3-D}/H$ as shown in Fig. 3 (c). Thus, by substituting the expression of E_H from (6) in (7), the terminal fringe capacitance can be given as following,

$$\frac{C_{terminal\ fringe}}{\varepsilon} = \frac{\pi T}{2\int_\delta^{\frac{\pi}{2}} \frac{1}{\sin\theta} d\theta} = \frac{\pi T}{2\ln\frac{1}{\tan(0.5\delta)}}. \quad (8)$$

Since δ is a tiny value, the terminal fringe capacitance is approximately proportional to T. The above approach assumes that either the radius is infinitely small, or the radius increases as x, as shown in Fig. 3 (c). However, when T is large, this assumption leads an error since the electric field in the shaded area in Fig. 3 (d) is not considered. One simple solution to compensate for this without changing the preceding derivation is to use $\delta = r_{3-D}/(H+0.5T)$ instead of $\delta = r_{3-D}/H$, which is marked in green in Fig. 3 (d).

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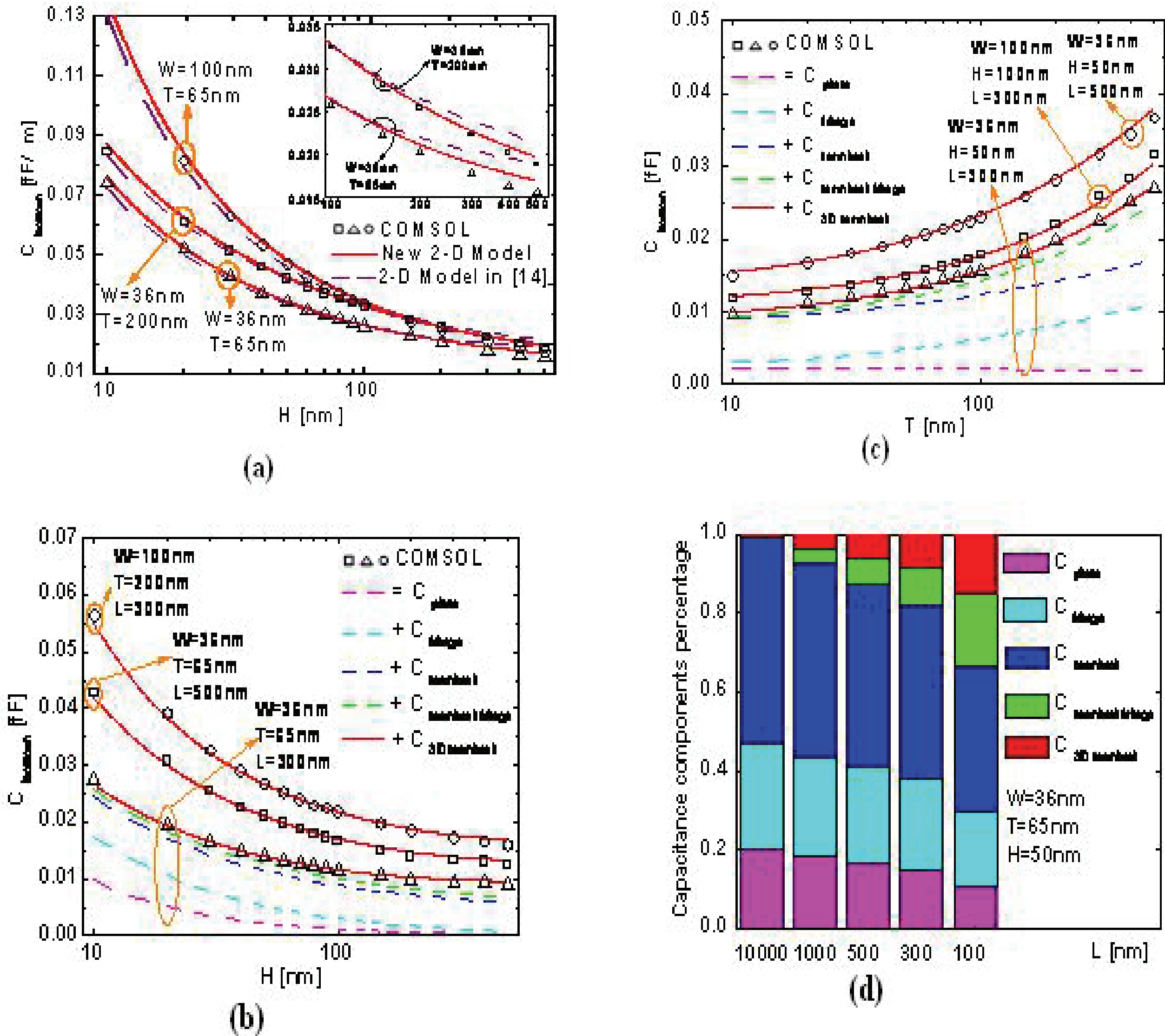

Fig. 4. (a) Verification of 2-D single line-over-plate capacitance model versus wire height; verification of 3-D single wire-over-plate capacitance model versus (b) wire height, (c) wire thickness, and (d) percentage of each capacitance component versus wire length. Vacuum is used as the dielectric is for better extension.

In 3-D case, the plate, fringe and terminal capacitance are calculated by multiplying 2-D models with the corresponding length and width. Finally, by combining all the components, C_{bottom} is given as below:

$$C_{bottom} = C_{plate} + C_{fringe} + 2C_{terminal} + 4C_{terminal\ fringe} + 4C_{3-Dterminal} \,. \quad \textbf{(9)}$$

III. Model Verification and Discussion

Fig. 4 (a) shows that the improved 2-D capacitance model is more accurate in general than the model in [12] according to CMOSOL simulations [3]. The inset figure highlights the improved accuracy when H is large.

Good agreement is shown in Fig. 4 (b) and (c) between the developed 3-D capacitance model and numerical results. Each capacitance component of a wire with typical dimensions (W, T, H, L) = (36 nm, 65 nm, 50 nm, 300 nm), is also shown in the figure. The terminal capacitance is again the most weighted component [12]. The 3-D components, i.e., the 3-D terminal and terminal fringe capacitance, also play important roles. They contribute nearly 20% of total capacitance in this case. Furthermore, the percentage of each component as L shrinks is illustrated in Fig. 4 (d). The 3-D terminal and terminal fringe capacitance becomes increasingly important as L decreases. Conceivably, without taking these components into account, the total capacitance will be underestimated.

The model's accuracy at different dimension corners is evaluated in Table I. For fair comparisons, both W and L are considered to multiply the 2-D model in [12]. The error of the 3-D model is well

below 5% for all cases, much better than the 2-D models.

TABLE I
COMPARISON OF THE MODEL WITH COMSOL SIMULATION

Dimensions (nm) {*W,T,H,L*}	Simula -tion	Our work		2-D model in [12]	
		Model	Error(%)	Model	Error(%)
{36,65,50,300}	0.0141	0.0139	-1.1667	0.0110	-22.284
{36,100,100,300}	0.0130	0.0132	1.6820	0.0094	-27.652
{36,65,100,300}	0.0116	0.0116	0.1396	0.0087	-25.141
{36,100,50,300}	0.0157	0.0157	-0.1515	0.0119	-24.175
{36,65,50,10000}	0.3454	0.3489	1.0225	0.3339	-3.3250

IV. Conclusion

Based on electric field decomposition, a model of parasitic capacitance for a basic interconnect structure of a 3-D single wire above a plate is developed. The study shows that the components at wire ends, i.e., the 3-D terminal and terminal fringe capacitance, cannot be neglected for 3-D interconnect, and become increasingly significant as the wire length shrinks. This model is validated by extensive numerical simulations; therefore, it may be useful for the nano-scale 3-D CMOS circuit simulation and design with TSV process in the beyond 28nm CMOS process technology.

V. ACKNOWLEDGMENT

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