Analysis of Gate-Length Dependence of Lags and Current Collapse in Field-Plate AlGaN/GaN HEMTs

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ABSTRACT

We make 2-D transient simulations of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer, where a deep acceptor above the midgap is considered. We particularly study how the gate lag, drain lag and current collapse in AlGaN/GaN HEMTs are influenced by the gate length and field-plate length. As a result, it is shown that the gate lag increases as the gate length becomes short, but the drain lag is not so dependent on the gate length. Then, the current collapse, which is a combined effect of gate lag and drain lag, tends to increase as the gate length becomes short due to the gate-lag effect.

Keywords: GaN, HEMT, deep acceptor, current collapse, gate length, field plate

1 INTRODUCTION

In AlGaN/GaN HEMTs, slow current transients are often observed even if the gate voltage or the drain voltage is changed abruptly [1]. This is called gate lag or drain lag, and is problematic for circuit applications. The slow transients mean that dc *I-V* curves and RF *I-V* curves become quite different, resulting in lower RF power available than that expected from the dc operation [2]. This is called current collapse. These are serious problems, and many experimental works are reported [1-5], and several theoretical works are made [5-10]. In previous theoretical works, the semi-insulating buffer is treated as undoped, and a deep donor and a deep acceptor are considered in it [6, 7], and the effects of a field plate on buffer-related lags and current collapse are also studied [9, 10]. Recently, a Fe-doped semi-insulating buffer layer is often adopted, and Fe acts as a deep acceptor [11, 12]]. Then, some theoretical works regarding current collapse including the Fe-doped semi-insulating buffer layer are also made [13, 14]. By the way, experimentally, it is suggested that the current collapse is more significant when the gate length is shorter. However, few theoretical works have not been made on this point. Therefore, in this work, we have simulated the dependence of lags and current collapse on the gate length of field-plate AlGaN/GaN HEMTs, and studied how they are influenced by the gate length and the field-plate length.

2 PHYSICAL MODELS

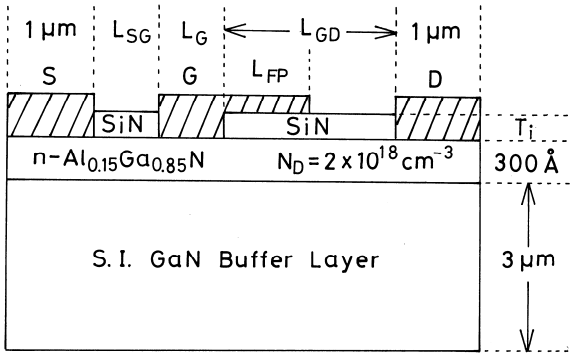

Figure 1: Device structures analyzed in this study.

Figure 1 shows a modeled device structure analyzed in this study. The gate length L_G is varied between 0.3 μm and 1.5 μm and the gate-to-drain distance L_{GD} is set to1.5 μm. The field-plate length L_{FP} is varied between 0 and 1 μm. The SiN layer thickness T_i is also varied between 0.01 μm and 0.1μm, but typically set to 0.03 μm. As a buffer layer, we consider a Fe-doped semi-insulating buffer layer. The Fe level (E_{DA}) is set 0.5 eV below the bottom of conduction band, and it is considered to be a deep acceptor. The energy levels of around E_C - E_{DA} = 0.5 eV are reported in the literature [11, 12]. In this case, the deep acceptors act as electron traps. The deep-acceptor density in the buffer layer is se to 10^{17} cm^{-3} here.

Basic equations to be solved are Poisson's equation including ionized deep-acceptor terms, continuity equations for electrons and holes which include carrier loss rates via the deep acceptor and rate equations for the deep acceptor [7, 15-19].

1) Poisson's equation

$$\nabla \bullet (\varepsilon \nabla \psi) = -q(p - n + N_D - N_{DA}^-) \quad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - R_{n,DA} \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - R_{p,DA} \quad (3)$$

where

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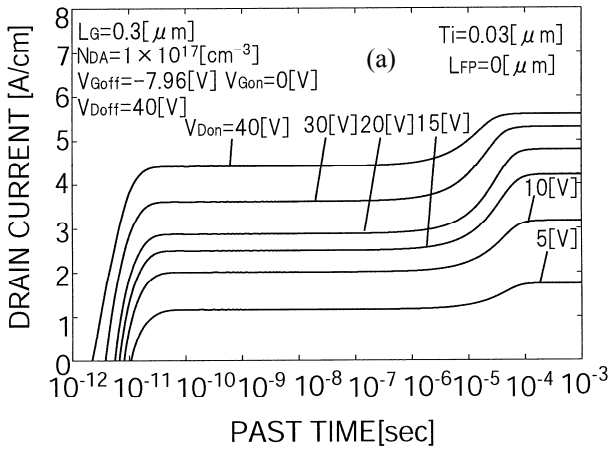


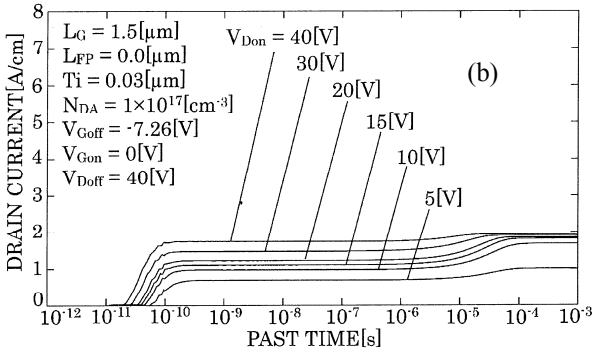


Figure 2: Calculated turn-on characteristics of AlGaN/GaN HEMTs when V_G is changed abruptly from the threshold voltage V_{th} to 0 V and V_D is changed from 40 V to V_{Don}. L_{FP} = 0. (a) L_G = 0.3 μm, (b) L_G = 1.5 μm.

$$R_{n,\mathrm{DA}} = C_{n,\mathrm{DA}}(N_{\mathrm{DA}} - N_{\mathrm{DA}}^-)n - e_{n,\mathrm{DA}}N_{\mathrm{DA}}^- \qquad (4)$$

$$R_{p,\mathrm{DA}} = C_{p,\mathrm{DA}}N_{\mathrm{DA}}^- p - e_{p,\mathrm{DA}}(N_{\mathrm{DA}} - N_{\mathrm{DA}}^-) \qquad (5)$$

3) Rate equation for the deep acceptor

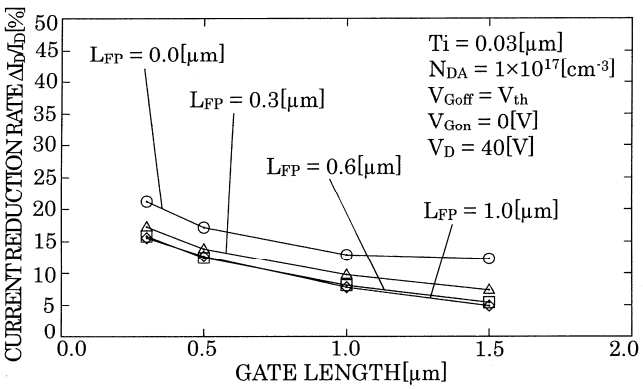
$$\frac{\partial}{\partial t}N_{\mathrm{DA}}^- = R_{n,\mathrm{DA}} - R_{p,\mathrm{DA}} \qquad (6)$$

where N_{DA}^- represents the ionized deep-acceptor density. $C_{n,\mathrm{DA}}$ and $C_{p,\mathrm{DA}}$ are the electron and hole capture coefficients of the deep acceptor, respectively, $e_{n,\mathrm{DA}}$ and $e_{p,\mathrm{DA}}$ are the electron and hole emission rates of the deep acceptor, respectively. These are given as functions of the deep acceptor's energy level and the capture cross sections.

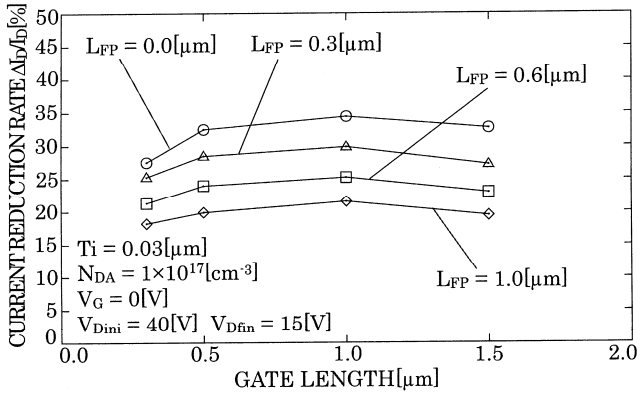
These basic equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

3 RESULTS AND DISCUSSIONS

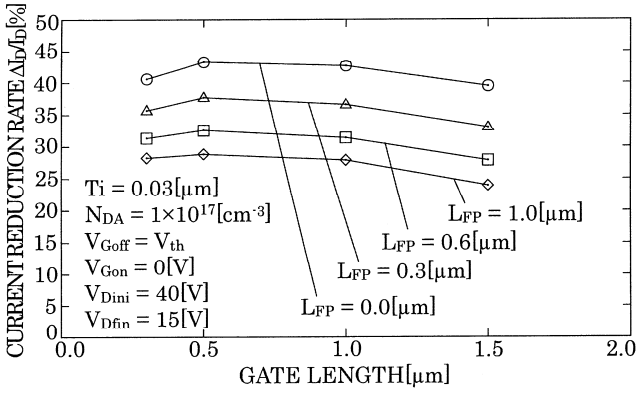
Fig.2 shows a comparison of calculated turn-on characteristics between the two cases with (a) L_G = 0.3 μm and (b) L_G = 1.5 μm when V_G is switched on from the threshold voltage V_{th} to 0 V and V_D is changed from 40 V to V_{Don}. Here, L_{FP} = 0. In both cases, the drain current I_D remains at a low value for some periods and begin to increase gradually, showing current collapse and gate-lag behavior. It is understood that I_D begins to increase when the deep acceptors in the buffer layer begin to emit



(a) Gate Lag



(b) Drain Lag



(c) Current Collapse

Figure 3: Current reduction rate $\Delta I_D/I_D$ due to (a) gate lag, (b) drain lag, and (c) current collapse as a function of the gate length L_G. The parameter is the field-plate length L_{FP}.

electrons. When V_{Don} = 40 V where only V_G is changed, the slow transients correspond to the gate lag. It seems that the gate lag rate is smaller for L_G = 1.5 μm. The current collapse is a combined effect of gate lag and drain lag, and hence the drain lag seems to be rather large in both cases.

Fig.3 shows current reduction rate $\Delta I_D/I_D$ (ΔI_D: current reduction, I_D: steady-state current) due to (a) gate lag, (b) drain lag, and (c) current collapse as a function of L_G. The parameter is the field-plate length L_{FP} where it is varied between 0 and 1 μm. It is clearly seen that the gate lag rate increases when L_G becomes short [20]. It is also seen that by introducing a field plate ($L_{FP} > 0$), the gate lag is reduced, although it is not so dependent on L_{FP} when $L_{FP} \geq 0.3$ μm. From Fig.3(b), we see that the drain lag is not so dependent on L_G, although it decrease clearly when L_{FP} becomes long. Finally, from Fig.3(c), we see that the current collapse tends to increase when L_G becomes short. This is due to the increase in gate lag because the current collapse is a combined effect of gate lag and drain lag. It is also clearly seen that the current collapse is reduced by increasing the field-plate length.

Fig.4 shows a comparison of electron density profiles between the two cases with (a) L_G = 0.3 μm and (b) L_G = 1.5 μm, where L_{FP} = 0. The left figures show the cases of ON state (V_D = 40 V and V_G = 0 V) and the right figures show the cases of OFF state (V_D = 40 V and $V_G = V_{th}$). Note that V_D is the same. When $V_G = V_{th}$ (negative), electrons are injected deeper into the buffer layer and captured by the deep acceptors. So, the gate lag arises. The electron injection occurs entirely under the gate when L_G = 0.3 μm, but it occurs only at the drain side of the gate when L_G = 1.5 μm. Therefore, we can say that the gate lag and current collapse become large when L_G is short.

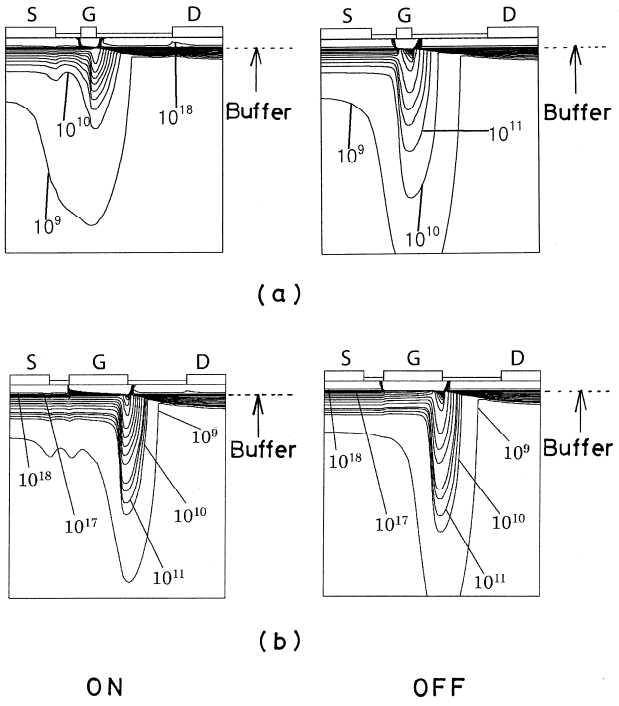


Figure 4: Comparison of electron density profiles between the two cases of ON state (V_D = 40 V, V_G = 0 V) and OFF state (V_D = 40V, $V_G = V_{th}$). L_{FP} = 0. (a) L_G = 0.3 μm, (b) L_G = 1.5 μm.

4 CONCLUSION

We have made a 2-D transient simulation of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer, where a deep acceptor above the midgap is considered. We have particularly studied how the gate lag, drain lag and current collapse in AlGaN/GaN HEMTs are influenced by the gate length. As a result, it has been shown that the gate lag increases as the gate length becomes short, but the drain lag is not so dependent on the gate length. Then, the current collapse, which is a combined effect of gate lag and drain lag, has been shown to increase as the gate length becomes short due to the gate-lag effect.

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