The Multifunctional 3D Interposer Platform for HPC and Power Discretes Development, Measurements, Design Guidelines

Grzegorz Janczyk*, Tomasz Bieniek**

* Instytut Technologii Elektronowej, Department of Integrated Circuits and Systems Design, Al. Lotników 32/46, 02-668 Warszawa, Poland, janczyk@ite.waw.pl
** Instytut Technologii Elektronowej, Department of Silicon Microsystem and Nanostructure Technology Okulickiego 5E, 05-500 Piaseczno, Poland, tbieniek@ite.waw.pl

ABSTRACT

This paper presents results of the research focused on advanced integration and high performance computing (HPC) cooling techniques for Integrated Circuits (IC) along with their adaptation for subsequent application in power electronics. Part of the research presented here was carried out in frame of the European FP7 project CarrICool (*Modular Interposer System Architecture providing scalable Heat Removal, Power Delivery and Optical Signaling*) [1] lead in by Authors cooperation with the project leader IBM-Zurich. This paper also refers to the novel application of the liquid cooling interposers developed in frame of CarrICool project adapted for high power applications being developed in frame of the R3-PowerUp (*BCD and Power Discretes 300mm Pilot Line*) [2] project lead in H2020 perspective.

Keywords: 3D interposer, 3D integration, Power Discretes, Signal Integrity, CarrICool, R3-PowerUp, Cooling, Power Electronics, Modeling, TSV, Simulation, Interconnects, RF, RDL, CPL.

1. CARRICOOL ACHIEVEMENTS

The CarrICool research was focused on development of the advanced modular cooling interposer (CiC) providing scalable heat removal, local power delivery and optical signaling features (Fig. 1). Dozens of technical aspects critical for high performance computer systems (HPC) like signal transmission in coolant channel proximity have been investigated up to 50GHz bandwidth (effectively 40GHz) and optimized for HPC environment application.

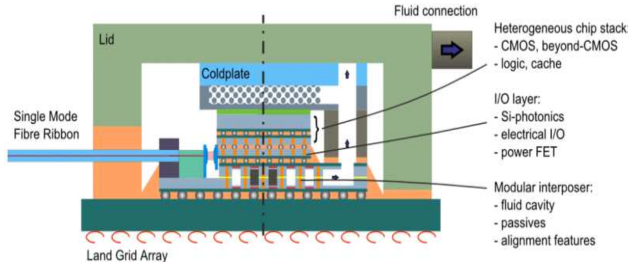

Fig. 1: The idea of CarrICool interposer and its application [1][3].

Buck converters have been integrated within the CiC Interposer enabling customized power delivery features for deep system optimization and reliability improvement. Optical link interfacing opened the Interposer for cutting edge, high speed data transmission technologies. Signal integrity (SI) aspects [4] were critical for electric buses still dominating in IC design. Data buses are routable across and through the CiC Interposer using top and bottom redistribution layers (RDL) and through silicon VIA interconnects (TSV). Wafer / IC / chip / stack / system level optimization in power delivery, cooling, data transmission, reliability and performance domains has been effectively performed in frame of CarrICool project. Therefore the coplanar line (CPL) has been selected as the interconnecting structure formed in the redistribution layer (RDL) of the CiC interposer. Signal loses optimization led authors to formulate a set of design guidelines. One of them is to use RDL layer exceeding 1µm thickness due to optimized loses reduction. The resistivity of the substrate has been estimated to exceed 1kΩcm to minimize loses up to 40GHz [5]. Due to CarrICool project budget constraints, low resistivity substrates (20Ωcm) also have been used for integration technology testing purposes.

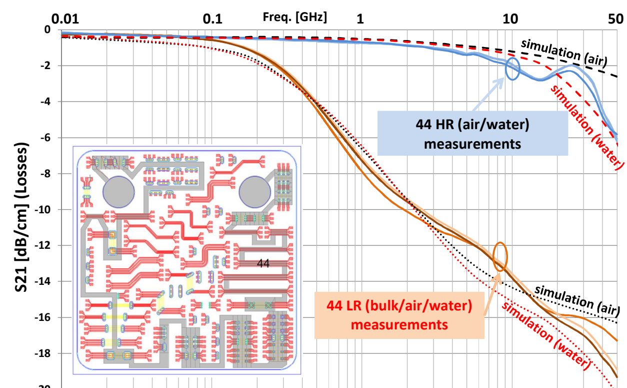

Fig. 2: Test chip with various CPL and TSV test structure configurations. Losses [dB/cm] simulation vs. measurements on signal integrity test chip for various up to 50 GHz for high (HR – air/water filled channels) and low (LR – air/water filled channels, no channels) resistivity of the substrate.

The CarrICool related research activity covered analysis of the signal path neighborhood: proximity of cooling channels, TSVs and other CPLs. The cooling liquid has been fixed due to the applied technology to the deionized water only. The subset of technology guidelines has been effectively formulated along with dozens of dedicated test structures (Fig. 2). The set of simulations performed confirmed that EM field penetration depth does not exceed

50µm for substrate resistivity over 1kΩcm (high resistivity - HR) and 20Ωcm (low resistivity - LR) variant substrates. The vertical integration forced application of the TSVs made available in the technology shared for the project by FhG IZM-ASSID (the CarrICool project partner). Various TSV configurations and CPL have been examined by modeling, simulation and real measurements (Fig. 2). Test structures have been fabricated using 3µm-thick copper RDL technology variant [6][7].

Media in fluidic (cooling) channel	TSVs on separate Si islands	TSVs on one common Si islands	TSVs on separate Si islands	TSVs on one common Si islands
Air	0.5	2	0.8	1.9
Water	>10	2.5 ÷ 4	>10	2

Fig. 3: Average losses [dB/cm] for 50GHz for various copper TSV configuration of cooling channel proximity on high resistivity substrate. Common silicon island, separate islands for water/air filled cooling channels in four variants of interconnecting topology.

The simulations performed lead the authors to the set of conclusions (Fig. 3) that separate islands with TSV assure better performance than common-island interconnecting structures for air-filled cooling channels. It is opposite for water-filled cooling channels where water proximity affects performance and makes common-island geometry more effective than separate-island layout. Simulations of signal loses have been verified by measurements up to 40GHz. Another conclusion is that due to the shielding effect, the specific configuration of ground and signal leading TSVs with the signal-TSV surrounded by numerous ground-TSVs is more effective than simple, three node GSG (ground-signal-ground) TSV for common-island configuration.

2. TECHNOLOGY CHALLENGES

The CarrICool project achievements and authors professional experience profit in subsequent research projects activities, like the R3-PowerUp [2] covering setup of the first 300mm pilot line in Europe oriented on smart power and discrete power devices featuring 90-110nm process node for single chip integration of power modules, analogue modules and high-density logic (digital) optionally assisted by embedded non-volatile memories (available in BCD9) for the implementation support of complex Systems-on-Chip (SoC). One of the IC fabrication technology validators is the electronic speed controller (ESC) for brushless motors applied in unmanned aircraft vehicles (UAV). The current range depends on application and UAV size varying from 2A for small vehicles up to 100A burst current for advanced powerful applications. The ESC specification relies on the 110nm process node (BCD9) technology by STMicroelectronics. There are numerous technical issues to be resolved, from the system partitioning, trough power delivery issues and cooling requirements, physical integration constrains up to the interfacing and firmware development (IP). System partitioning [8] has been discussed in [9] along with the ESC specification and available implementation scenarios. There are several technical issues of the ESC development related to CarrICool project achievements in the field and cooling capabilities of the CarrICool-based interposer which can be adapted and useful for power applications.

One of the fundamental constrains faced using any power technology is heat dissipation from the power module. Hence an idea of the CarrICool-like interposer technology application for power electronics development to improve performance and reliability. The liquid cooling technique developed in frame of the CarrICool project assured the cooling efficiency around 600W/cm^2 [10]. It leveraged designers to a new level of unprecedented 3D integration capabilities [11] to keep thermal regime margin sufficient for operation of analogue and digital parts of the power SoCs with advanced data processing modules on board. Power applications require high currents and voltages on RDL layer to assure communication and power delivery outside the chip. It is not necessary to use TSV structures for power applications. Therefore the standalone case of the cooling structure (Fig. 4) has been analyzed to conclude if the RDL wiring over the oxidized silicon is capable to get through the high voltage stress or will break.

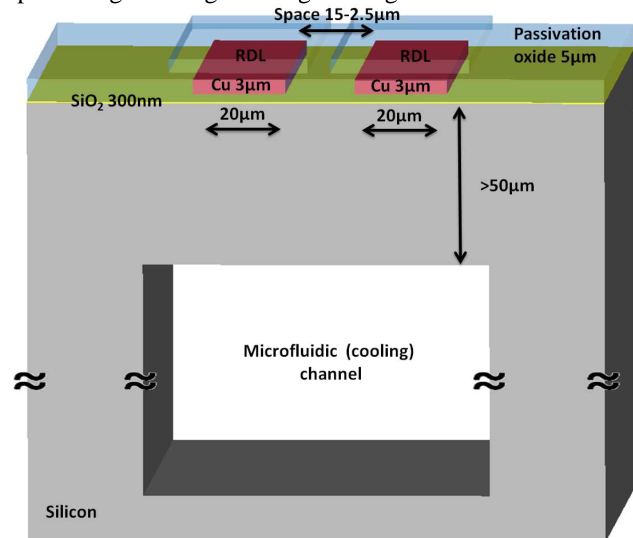

Fig. 4: Sample cross-section of structure for evaluation of the CarrICool-like interposer RDL structure in power application conditions including cooling channels.

Whole the modeling and simulation activities [12] for voltage stress aware exploitation along with specific estimations for power dissipation capabilities have been conducted by the authors team using Atlas (TCAD) for two spacing of 5µm and 15µm vs. two bottom RDL oxide thicknesses 300nm (Fig. 5) and 1000nm (Fig. 6) and using Comsol for 6 bottom RDL oxide thicknesses and four different spacing. Comsol results have been intentionally parameterized by oxide thickness (Fig. 7) and by gap between planar interconnects in RDL (Fig. 8). The

modeling experiment has been performed for CarrICool-based CPL (coplanar) structure formed in 3µm thick copper RDL layer with interconnecting strips spaced for 2.5-15µm formed over 300nm silicon dioxide on high (1kΩcm) and low (20Ωcm) resistivity wafers user for power delivery and routing. Extrapolating power supply transient conditions the peak voltage has been limited to 400V. As it comes from Atlas (TCAD) simulations 300nm thick oxide allows electric field to enter the substrate (Fig. 5), whereas 1000nm thick oxide (Fig. 6) limits the electric field to the SiO_2 layer.

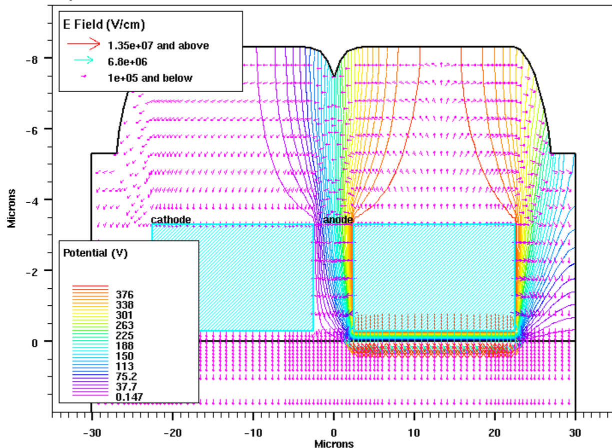

Fig. 5: Sample structure cross section for evaluation of the CarrICool-like interposer RDL layer behavior in case of power application conditions. Electrical field distribution by TCAD Atlas: 5µm spacing, 300nm oxide thickness (T_{OX}).

COMSOL simulations have been performed to address more configurations. The oxide thickness (T_{OX}) was in the range of 100-1000nm, inter-strip gap in the range between 2.5µm and 15µm. Results have shown that there is no risk to SiO_2 break due to electric stress by high voltage if there is sufficient space between polarized metal strips of planar interconnects and the oxide is thick enough.

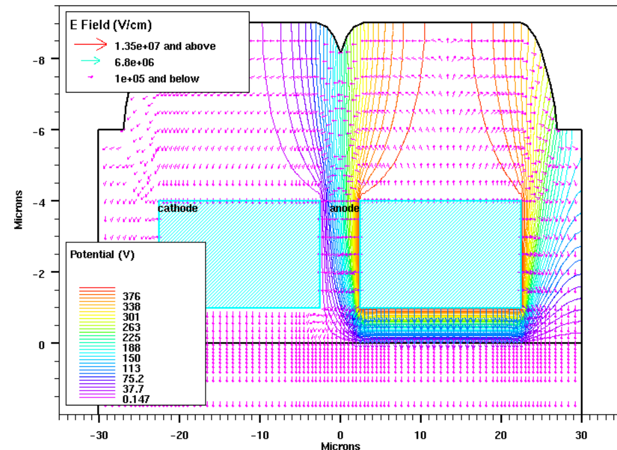

Fig. 6: Sample structure cross section for evaluation of the CarrICool-like interposer RDL layer behavior in case of power application conditions. Electrical field distribution by TCAD Atlas: 5µm spacing, 1µm oxide thickness (T_{OX}).

Only one examined configuration with 2.5µm spacing between strips during simulations exceeded the SiO_2 breakdown threshold (Fig. 7) for oxide thickness below 200nm. For 100nm oxide thickness under 400V DC voltage applied to the test structure the E field reaches the 9MV/cm (the break threshold level).

The dominant voltage drop forms within the SiO_2 layer. COMSOL simulations have been performed for both substrate resistivities (HR=1kΩcm, LR=20Ωcm) for various oxide thicknesses and 2.5µm, 5µm, 10µm, 15µm gaps between interconnects (Fig. 8).

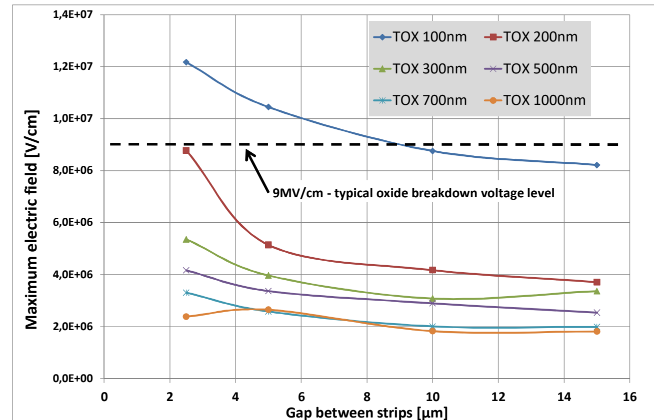

Fig. 7: Peak values of the E field across the SiO_2 layer under the RDL for 2.5µm, 5µm, 10µm, 15µm gaps between interconnects and oxide thickness ranging from 100nm to 1µm.

The substrate (silicon wafer) resistivity influence on SiO_2 field does not affect DC electric field distribution. Top passivation slightly moderates peak E field distribution within the bottom oxide of the RDL, but it is of primary importance from reliability point of view taking into consideration electric breakdown through the air on top of the RDL. If passivated there is no risk on sparking between adjacent paths even if in 5µm proximity.

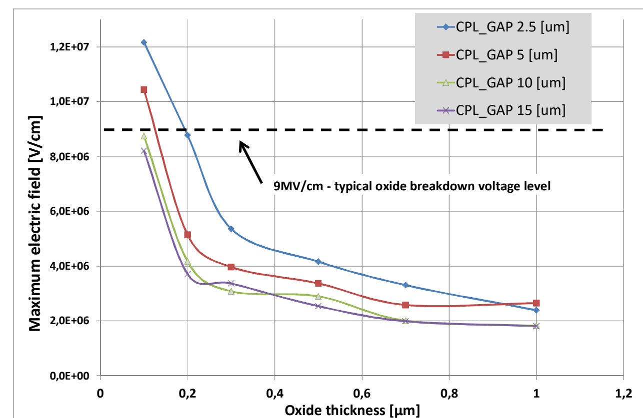

Fig. 8: Peak values of the E field across the SiO_2 layer under the RDL for 2.5µm, 5µm, 10µm, 15µm gaps between interconnects and T_{OX} ranging from 100nm to 1µm.

The test structure for simulation has been modeled with care to get the results not affected by limited test structure dimensions. As it comes from Fig. 9, the peak value of the normalized E field was limited to the volume or the silicon dioxide under the redistribution layer with interconnects.

3. CONCLUSIONS

COMSOL and TCAD simulations have shown that that CarrICool-like cooling interposer can be applied for high power applications. Although high power features of TSV structures have not been analyzed yet (it is planned to do so), the general conclusion from the research performed is that for high voltage (up to 400V) stresses there is no risk on SiO_2 electrical breakdown. As it comes from simulation results if there is sufficient space (over 5µm) between polarized metal strips of planar interconnects and oxide is thick enough (over 200nm) the 3µm thick copper RDL layer can lead power signals.

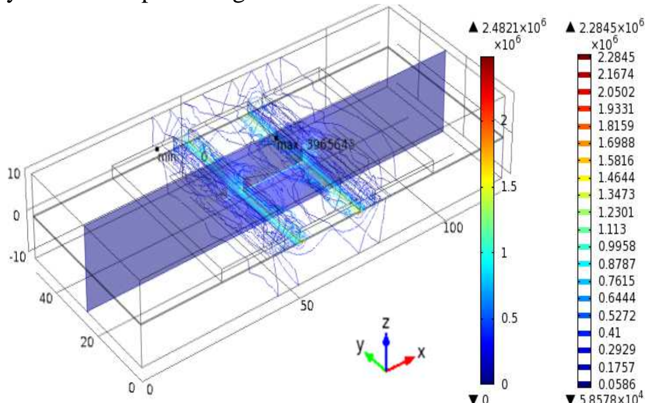

Fig. 9: Sample distribution of absolute E value across the power wiring formed in the RDL layer for 300nm oxide thickness and 5µm gap between them.

REFERENCES

[1] CarrICool FP7 EU project - more info available at www.carricool.eu

[2] R3-PowerUp JU ECSEL EU project - more info available at http://www.ecsel.eu/projects/r3-powerup

[3] Bieniek T., Janczyk G.: "Innovative 3D system development by multifunctional IC interposer platform - Signal Integrity and Thermal Management - solutions for High Performance Computing", 6th Electronic System-Integration Technology Conference (ESTC), Grenoble, France, 2016, DOI: 10.1109/ESTC.2016.7764716

[4] Janczyk G., Bieniek T., Bajurko P.: "CarrICool – the Innovative 3D Interposer Platform for HPC Systems: Analysis, Simulations, Optimization, Practice for Reliability Improvement and Performance Increase", TechConnect Briefs, Volume: 4, Informatics, Electronics and Microsystems, 2017, pp: 47 – 50

[5] Sun X., Van der Plas G., Detalle M., Beyne E.: "Analysis of 3D interconnect performance: effect of the Si substrate resistivity", IEEE International Conference on 3D Systems Integration 3D IC, Kinsale, Ireland, 2014, DOI: 10.1109/3DIC.2014.7152156.

[6] Kleff J., Schlottig G., Mrossko R., Steller W, Oppermann H., Keller J., Brunschwiler T.: "Intra-stack sealing of tier interconnects using the interconnect alloy", 6th Electronic System-Integration Technology Conference (ESTC), Grenoble, France, 2016, DOI: 10.1109/ESTC.2016.7764489

[7] Stiebing M., Lörtscher E., Steller W., Vogel D., Wolf M. J., Brunschwiler T., Wunderle B.: "Stress Investigations in 3D-integrated Silicon Microstructures", 17th International Conference on IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2016), Montpellier, France, 2016, DOI: 10.1109/EuroSimE.2016.7463368

[8] Janczyk G., Bieniek T., Grabiec P., Wymysłowski A., Swierczynski R.: "Optimization of MEMS-IC SiP Development Reliable Design Methods", Third IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (3D TEST), Anaheim, USA

[9] Bieniek T., Janczyk G.: "European Activity for Smart Power Electronics and Power Discretes - The R3-PowerUP EU Project", TechConnect Briefs 2018

[10] International Roadmaps for Semiconductors (ITRS) 2012 - http://www.itrs2.net/itrs-reports.html

[11] Ruch P., Brunschwiler T, Escher W., Paredes S., and Michel B.: "Toward five-dimensional scaling: How density improves efficiency in future computers", IBM Journal of Research and Development, 55(5):1–13, 2011

[12] Ortloff D., Schmidt T., Hahn K.; Bieniek T., Janczyk G., Bruck R.: "MEMS Product Engineering. Handling the diversity of an Emerging Technology. Best Practices for Cooperative Development", Springer 2013, DOI: 10.1007/978-3-7091-0706-5

ACKNOWLEDGMENTS

Presented works has been partially financed under:

- the CarrICool project co-fund by EU's 7FP and the Polish Ministry of Science and Higher Education (MNiSW) - agreement 619488,
- the statutory ITE projects (1.02.078, 1.09.078),
- the R3-PowerUp project co-fund by JU ECSEL and The National Centre for Research and Development (NCBR) under the agreement no.737417,
- the statutory ITE projects (1.02.094, 1.09.099).

This paper also profits from excellent collaboration with CarrICool project partners (IBM Zurich, FhG IZM-ASSID, and TU Chemnitz), the Warsaw University of Technology Team, especially dr. Eng. Pawel Bajurko supporting ITE Team for RF. Special thanks also to dr. Eng. Daniel Tomaszewski who supported Authors Team in TCAD simulation and to whom Authors are grateful for scientific support and fruitful discussions.