

# Hot Carrier Effect and Oxide Reliability of T-FinFET Devices

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## Abstract

Hot-carrier effect and oxide reliability of CMOS T-FinFET with 2.1nm-thick gate-SiO<sub>2</sub> were investigated. It was found that hot-carrier immunity improves as the T-FinFET fin width (body thickness) decreases, which facilitates gate-length scaling, while it is degraded at elevated temperature due to the self-heating effect. High values of Q<sub>BD</sub> are achieved for devices with very small gate area. A post-fin-etch hydrogen anneal is helpful for improving hot-carrier immunity and Q<sub>BD</sub>.

**Keywords:** Integrated Circuits, Semiconductor devices, Field effect transistor, Tunneling FET, FinFET, Hot carrier effect, oxide reliability, Interfacial traps.

## Introduction

The T-FinFET offers the superior scalability over the conventional double-gate FinFET structure with a conventional process flow; hence, it is attractive for scaling CMOS technology to sub-7nm gate lengths. Several groups have recently reported on the fabrication and performance of CMOS T-FinFET devices [1-4]. In this work, the reliability of T-FinFETs is investigated. Hot-carrier reliability for various bias stress conditions, device dimensions, and substrate temperature are reported. Gate oxide charge-to-breakdown (Q<sub>BD</sub>) distributions are also presented.

## Experiment

Fabrication process details for the T-T-FinFETs used in this work have already been reported elsewhere [1-5]. Two different types of T-FinFETs were investigated: P+ poly-Si<sub>0.6</sub>Ge<sub>0.4</sub> gated T-FinFETs with gate lengths down to 23nm, fabricated using e-beam lithography (Group I); and N+ poly-Si gated T-FinFETs of gate length 120nm, fabricated using spacer lithography (Group II). In Group II, one wafer was annealed in hydrogen (5min @ 900°C and 1atm) to smoothen the fin sidewall surfaces prior to gate oxidation [5]. The gate dielectric in all devices was 2.1nm thermally grown SiO<sub>2</sub>. For Group I, significant boron penetration through the gate oxide into the channel/fin resulted in a high threshold voltage (V<sub>T</sub>=0.8V) and gate-underlapped structure for the n-channel T-FinFETs. (The

p-channel T-FinFETs have a conventional gate-overlapped structure.) This work is primarily focused on the reliability of sub-100nm L<sub>g</sub> T-FinFETs (Group I). Only the effects of post-fin-etch annealing in H<sub>2</sub> were studied using the longer-channel devices from Group II.

First, the worst-case bias condition for hot-carrier stress was determined, for V<sub>d</sub>=1.8V. The V<sub>T</sub> shift was found to be larger when the gate voltage was equal to the drain voltage (V<sub>g</sub>=V<sub>d</sub>), compared to V<sub>g</sub>=V<sub>d</sub>/2. Degradation in device performance parameters under V<sub>g</sub>=V<sub>d</sub>=1.8V stress was then tracked over time, for T-FinFETs of various gate lengths and fin widths (W<sub>fin</sub>), and several substrate temperatures. Q<sub>BD</sub> distributions were also obtained for CMOS T-FinFETs of various sizes.

## Results

In a double-gate n-channel T-FinFET, energetic electrons generated by impact ionization near the drain can become trapped at the gate-oxide interface or in the gate oxide to cause an increase in V<sub>T</sub>, while the generated holes flow to the region of lowest potential (*i.e.* the source), as shown in Fig. 1. For gate-underlapped n-channel T-FinFETs, holes can become trapped at the gate-oxide interface in this region, causing a decrease in V<sub>T</sub>. Thus, electron trapping and hole trapping have opposite effects on V<sub>T</sub>. For fixed V<sub>g</sub>-V<sub>T</sub>=1V, the dominant V<sub>T</sub>-shift mechanism depends on V<sub>d</sub>. Hole trapping is dominant for V<sub>d</sub>≤1.8V, so that the magnitude of V<sub>T</sub> decreases with increasing stress time, while electron trapping becomes dominant at higher values of V<sub>d</sub>, so that V<sub>T</sub> eventually increases with increasing stress time (Fig. 2).

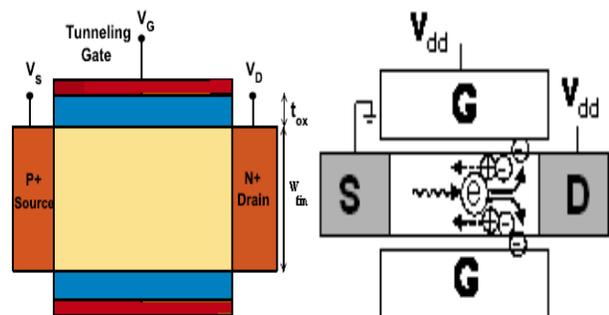


Fig. 1 T-FinFET Schematic and carrier movement in an n-channel device under hot-carrier stress bias conditions.

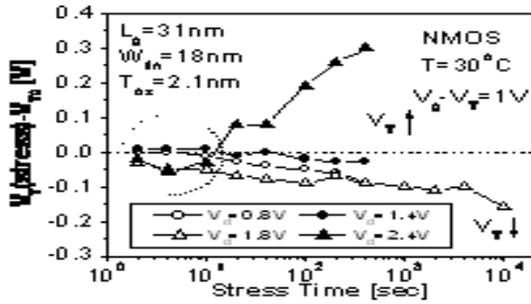


Fig. 2 N-channel T-FinFET (gate-underlapped structure) VT shift vs. stress time for different drain bias stress voltages. Electron trapping eventually dominates for very high Vd.

The magnitude of the VT shift decreases with increasing channel length due to the decreasing lateral electric field as shown in Fig. 3; however it increases with increasing fin width, as shown in Fig. 5a and Fig. 5b. To explain this dependence on W<sub>fin</sub>, the electron-hole pair generation rate (G) – due to impact ionization – and electron temperature (T<sub>e</sub>) profile in an n-channel double-gate MOSFET were studied using the device simulator MEDICI [6].

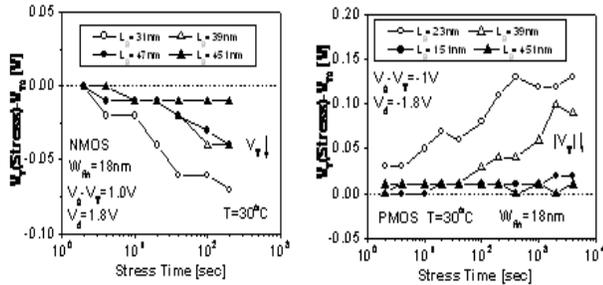


Fig. 3(a) N- and (b) P-Channel T-FinFET VT shift vs. stress time for different gate lengths. Longer-channel devices show better hot-carrier immunity due to the reduced lateral electric field.

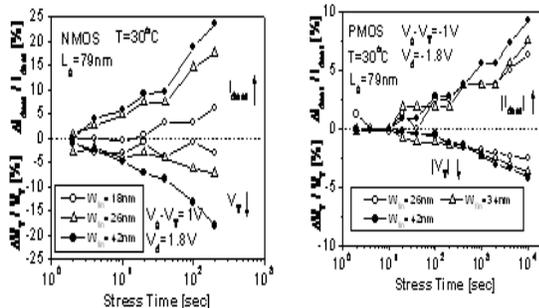


Fig.4 Relative shifts in VT and Idsat for N- (a) and for P- (b) T-FinFETs (gate-underlapped structure) vs. stress time, for different fin widths. Better hot-carrier immunity is achieved with a narrower fin.

The gate is assumed to be perfectly aligned (zero overlap) to the abrupt source/drain (S/D) junctions, and its

doping concentration is  $2 \times 10^{20} \text{cm}^{-3}$ . The simulation results (Figures 5-7) show that both T<sub>e</sub> and G increase with increasing W<sub>fin</sub>, which is consistent with the reliability measurement data. Fig. 5 shows that the potential profile becomes increasingly "one-dimensional" as the body thickness decreases. In the thicker body case, hot electrons are more strongly driven towards the gate oxide by the 2D curvature of the potential. The paths of generated hot carriers are indicated schematically by the bold arrows in Fig. 6a. Thus, hot-carrier immunity is improved by thinning the body of a T-FinFET, which also improves short-channel effects. The simulations show that G is insensitive to channel (fin) doping concentration (Fig. 6b).

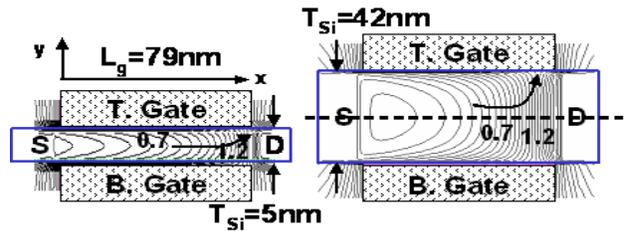


Fig.5 Simulated 2-D potential profile in a T-FinFET with Lg = 79 and TSi = 5 nm. The gate is perfectly aligned (zero overlap) to the abrupt S/D junctions (NS/D=2x1020cm3). The potential lines are more straight than for the thick-body device at the drain side.

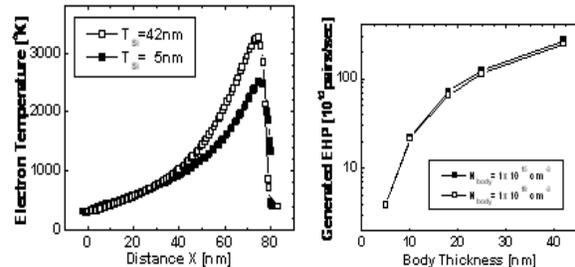


Fig. 6a Comparison of the electron temperature vs. distance along the center of the T-FinFET body, for thin vs. thick body. Fig.6b Simulated impact ionization induced electron-hole-pair generation rate in a T-FinFET (Lg=79nm) vs. body thickness. The impact ionization rate is reduced by thinning the body.

Degradation of the drain saturation current (I<sub>dsat</sub>) is observed after swapping the source and drain during device measurement after each stress interval, as shown in Fig.7. The degradation is more significant in an n-channel T-FinFET (n-T-FinFET) than a p-channel T-FinFET (p-T-FinFET) because the n-T-FinFET has an underlapped-gate structure and p-T-FinFET has an overlapped-gate structure. More hot carriers are trapped in the underlapped region. The trapped electrons at the drain, which becomes the source after the swapping, suppress the inversion charge. They result in an increase in VT, hence a decrease in I<sub>dsat</sub>. In the n-T-FinFET, I<sub>dsat</sub> is degraded 4.6% for W<sub>fin</sub> = 18nm and 24% for W<sub>fin</sub> = 42nm. This proves that more carriers are trapped for a thick body as compared with a thin body, consistent with the simulation results shown in Fig.5, and

also consistent with the improved hot-carrier immunity observed for a thinner body.

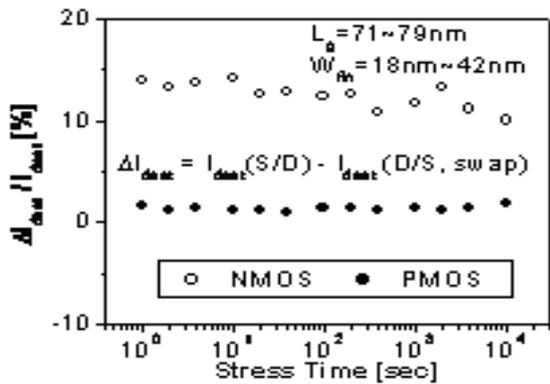


Fig.7 VT shift measured after each stress interval.  $I_{dsat}$  is decreased for measurement with swapped S/D.

Hot-carrier DC lifetime is plotted in **Fig. 8a** and **Fig. 8b**. The criteria for failure used for these plots are 10% change of  $V_T$ , 10% change of  $g_m$  (transconductance), and 10% change of  $I_{dsat}$ . Ref. 3 also reports hot-carrier DC lifetime results for T-FinFETs. However, the results presented here are not directly comparable to the previously reported results because the oxide thicknesses are different and the failure criteria were not noted. The lifetime is improved slightly for devices that received a post-fin-etch anneal in  $H_2$  (**Fig. 7**). These results indicate that T-FinFETs should be able to meet the 10-yr lifetime requirement for normal operating conditions, if  $W_{fin}$  is sufficiently small. The effect of substrate temperature during stress is shown in **Fig. 9** and **Fig. 10**. Ordinarily,  $G$  increases when the temperature is decreased, because of increased mean free path [7]. Thus, worse degradation (due to electron trapping) is seen at  $-50^\circ C$  compared to  $30^\circ C$ . At elevated temperatures, self-heating effects are significant in SOI MOSFETs and can enhance  $G$  [8]. Thus, we also find worse degradation (due to electron trapping) at  $120^\circ C$  vs.  $30^\circ C$ .

The gate voltage was linearly ramped for charge-to-breakdown ( $Q_{BD}$ ) measurements. The area of a single-fin device is  $7.11 \times 10^{-3} \mu m^2$  ( $L_g=79nm$  and fin height=45nm). The measured  $Q_{BD}$  is approximately  $10^4 C/cm^2$  for these T-FinFETs with extremely small gate area (**Fig.11**). Degraeve *et al.* [9] reported that  $Q_{BD}$  becomes a strong function of the channel area as the gate-oxide thickness decreases. A similar trend (increasing  $Q_{BD}$  as the channel area decreases) is also observed in this work, as shown in **Fig. 11** and **Fig. 12**. Higher and more uniform  $Q_{BD}$  is achieved when a post-fin-etch anneal in  $H_2$  is employed (**Fig. 16**).

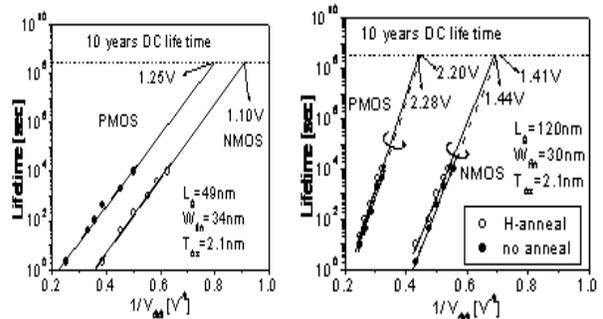


Fig. 8a Hot-carrier DC lifetime for CMOS T-FinFETs (P+ poly-Si $0.6Ge0.4$  gate, no hydrogen anneal after fin etch).

Fig.8b Hot-carrier DC lifetime for CMOS T-FinFETs (N+ poly-Si gate), showing the benefit of a hydrogen anneal ( $5^\circ$  @  $900^\circ C$ ) after fin etch.

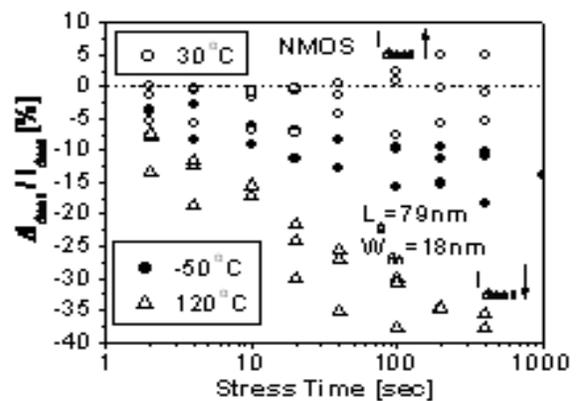


Fig.9 Effect of substrate temperature on relative  $I_{dsat}$  shift with stress time, for NMOS T-FinFETs.

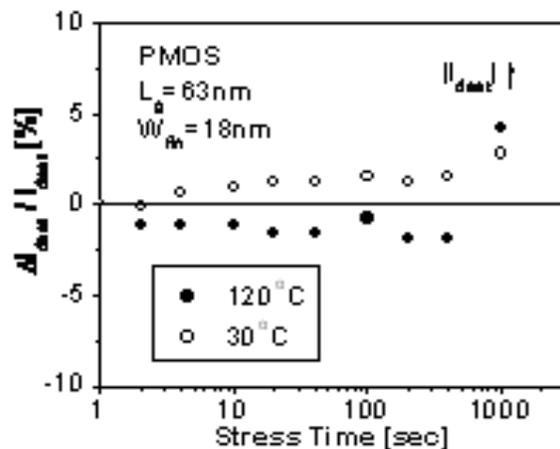


Fig. 10 Effect of substrate temperature on relative  $I_{dsat}$  shift with stress time, for PMOS T-FinFETs.

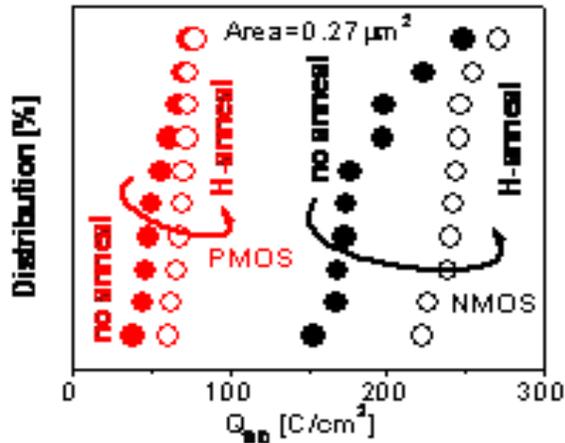


Fig. 11 QBD distributions for CMOS T-FinFETs (P+ poly-Si<sub>0.6</sub>Ge<sub>0.4</sub> gate, no hydrogen anneal after fin etch). QBD is extremely high for very small gate areas.

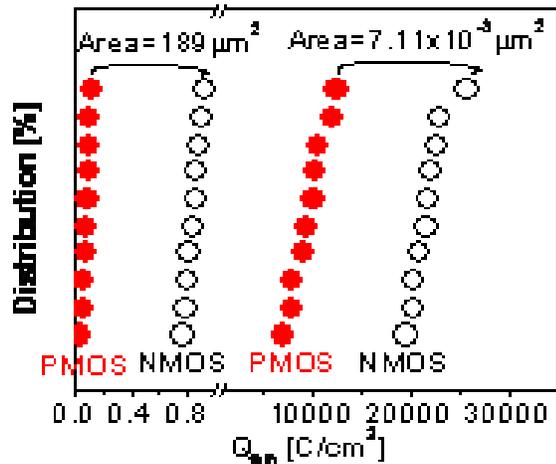


Fig. 12 QBD distributions for CMOS T-FinFETs (N+ poly-Si gate). QBD is higher and more tightly distributed for devices which received a post-fin-etch anneal in hydrogen to smoothen the fin sidewall surfaces.

## Summary

The reliability of CMOS T-FinFETs has been studied. Hot-carrier immunity is found to improve with decreasing  $W_{fin}$ , and is degraded at high substrate temperature (120°C) due to the self-heating effect, as well as at low substrate temperature (-50°C). High values of QBD (>104 C/cm<sup>2</sup>) are achieved for 2.1nm gate oxide, for very small gate area. Hydrogen annealing to smoothen the fin sidewalls is effective for improving both hot-carrier lifetime and QBD.

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