Flexible virtual source compact model for efficient modeling of emerging channel materials and device architectures
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Abstract -- The virtual source (VS) compact model has been shown in the literature to describe nano-scale MOSFETs quite well. It is therefore an attractive alternative to sophisticated and complicated established compact models due to its small number of model parameters. The latter can also fairly easily be determined from the electrical characteristics of a single transistor structure. In this paper, VS model has been modified with the goal of enabling a circuit and system simulation based comparison of diverse emerging FET technologies. Examples for the application of the extended more flexible X-VS model to experimental data of a Si MOSFET, an InGaAS HFET and a carbon nanotube (CNT) FET are shown.

Keywords: Carbon nanotube, CNTFET, field-effect transistor, linearity, quantum capacitance limit, semiclassical transport, Schottky barrier.

1 INTRODUCTION
The end of bulk silicon-based transistor technology has often been predicted in the scientific and technical literature [1]. As a result, many new channel materials (such as III-V semiconductors, 2D materials, nanowires and -tubes) and device concepts (such as FinFETs, nanosheets, lateral or vertical nanowires and -tubes) have been explored and suggested to replace silicon-based MOSFETs. However, for evaluating the pros and cons of these large number of alternatives in applications under realistic conditions, comparisons at the circuit level are needed. Therefore, a simple and versatile compact model is required that also provides an intuitive understanding of its material and device structure related parameters. The model should have an as low as possible number of parameters to facilitate an easy and quick parameter extraction since most of these new technologies are not mature and often characteristics of only a few or even a single fabricated device are available that do not allow the extraction of parameters for sophisticated compact models like BSIM.

These modeling challenges are addressed by the extended Virtual Source (X-VS) compact model presented in this paper.

2 X-VS COMPACT MODEL
The equivalent circuit of the X-VS compact model in Fig. 1 can be divided into an internal and external portion. The latter comprises finger and metallization represented by the resistances $R_{sf}$, $R_{df}$, $R_g$ and the parasitic capacitances $C_{gs,par}$, $C_{gd,par}$ and $C_{ds,par}$. The internal portion consists of the source and drain related contact resistances $R_{sc}$ and $R_{dc}$ as well as a nonlinear transfer current source $I_{vs}$ and nonlinear mobile charges $Q_s$ and $Q_d$. The equations for the latter ones are based on the Virtual Source compact model [2] but augmented here with new material and structure related formulations as well as a few fitting parameters, that enable its application to a diverse set of process technologies. The model equations of the X-VS model are summarized below along with hints towards the physical meaning of the modifications and their parameters. Model parameters are indicated by bold faced letters.

$$I_{vs} = WgQ_{ix0}v_{x0}F_{ds}$$

$$Q_{ix0} = C_{ch}n_{ss}V_T \ln \left[ 1 + \exp \left( \frac{V_{gisi} - V_{th} + \alpha V_T F_{ds}}{n_{ss}V_T} \right) \right]$$

where $W_g$ is the total gate width. $Q_{ix0}$ is the channel charge per unit area and $v_{x0}$ is the carrier velocity at the virtual source point $x_0$. The channel charge is given by
\[ V_{th} = V_{th0} - \delta V_{disi} \]  

(3)

with the DIBL factor \( \delta \). The function

\[ F_f = \left[ 1 + \exp\left( \frac{V_{gisi} - V_{th} + \alpha V_T/2}{\alpha V_T} \right) \right]^{-1} \]  

(4)

is of Fermi type and allows a smooth reduction of the threshold voltage in eq. (2) by \( \alpha V_T \) from the subthreshold to the strong inversion region in MOSFETs. \( \alpha \) is a fitting factor and \( V_{th0} \) a model parameter.

A possible degradation of the channel charge in eq. (2) with large vertical electrical fields (i.e. large gate voltages) is taken into account by the factor

\[ f_{deg} = 1 - \exp\left( -\frac{1}{\gamma V_{g,eff}} \right), \]  

where \( \gamma > 0 \) is a fitting parameter and \( V_{g,eff} \) is given by

\[ V_{g,eff} = n_{ss} V_T \ln \left[ 1 + \exp\left( \frac{V_{gisi} - V_{th} + \alpha V_T F_f}{n_{ss} V_T} \right) \right] \]  

(6)

Fig. 2 displays the behavior of \( f_{deg} \) as a function of \( V_{gisi} \). The original VS-model [2] is recovered by \( f_{deg} = 1 \) which switches off this effect.

The channel material may consist of either a bulk semiconductor or a certain number \( n_t \) of tubes/wires or fins of a FINFET per gate width \( W_q \) given by the tube/wire/fin density \( \rho_t = n_t / W_q \).

In the original VS model the channel capacitance \( C_{ch} \) is a model parameter which describes the inversion capacitance of the MOSFET. However, the X-VS compact model uses a series combination of the quantum capacitance \( C_q \) and the oxide capacitance \( C_{ox} \) to model \( C_{ch} \):

\[ C_{ch} = \frac{C_{ox} C_q}{C_{ox} + C_q} \]  

(7)

In case of one-dimensional channels, \( C_q \) is given by the tube/wire/fin quantum capacitance \( C_{q,t} \) multiplied with the oxide capacitance \( C_{ox} \), tube/wire/fin density \( \rho_t \).

Different device architectures (see Fig. 3) are being handled by the availability of the corresponding formulations for the oxide capacitance. For bulk semiconductors \( C_{ox} = e_{ox} \rho_t / t_{ox} \). For nanotube and -wires with radius \( r_{semi} \) the oxide capacitance depends, among others, on the gate geometry. For gate-all-around structures one obtains

\[ C_{ox} = \frac{2\pi e_{ox} e_0 \rho_t}{\ln(h/r_{semi})} \]  

(8)

with \( h = r_{semi} + r_{semi} \). A single planar gate can be modeled with

\[ C_{ox} = \frac{2\pi e_{ox} e_0 \rho_t}{h}, \]  

(9)

which includes the impact of screening effects between tubes or wires. Finally, for FinFETs with \( U = W_{fin} + 2*H_{fin} \) as the effective channel width per fin

\[ C_{ox} = \frac{e_{ox} e_0 U \rho_t}{t_{ox}}. \]  

(10)

Fig. 3: Schematic cross sections of the different device architectures.

The drain voltage dependence of \( I_{vs} \) in eq. (1) is described by the function

\[ F_{ds} = F_s F_a F_d, \]  

(11)

where

\[ F_s = \frac{V_{disi} / V_{dsat}}{[1 + (V_{disi} / V_{dsat})^\beta]^{1/\beta}} \]  

(12)

represents the velocity-field dependence of carriers in the channel and

\[ F_a = 1 + \frac{V_T}{V_a} \ln \left( 1 + \exp\left( \frac{V_{disi} - V_{dsat}}{V_T} \right) \right) \]  

(13)

accounts for channel length modulation (i.e. Early effect) and thus a finite output conductance. For \( V_{disi} >> V_{dsat} \) eq. (13) reduces to \( F_a = 1 + (V_{disi} - V_{dsat}) / V_T \), otherwise \( F_a \approx 1 \). The
The original VS model with $F_s=1$ is recovered by an infinite $V_s$.

The possible influence of source/drain Schottky barriers on the drain current characteristics is taken into account by the empirical function

$$F_d = \left[ 1 + \exp\left( \frac{V_{\text{dist}} - V_{\text{th,d}}}{n_d V_T} \right) \right]^{-1}$$  \tag{14}

which can be used to model s-shaped output characteristics.

The saturation voltage in eq. (12) and eq. (13) is given by

$$V_{\text{d,sat}} = (V_{\text{d,sat,s}} + V_{\text{d,sat,q}})(1 - F_d) + V_T F_d$$  \tag{15}

with

$$V_{\text{d,sat,s}} = \frac{V_x 0 L_{\text{ch}}}{\mu_{\text{app}}}.$$  \tag{16}

The apparent mobility $\mu_{\text{app}}$ is calculated according to Matthiessen’s rule

$$\mu_{\text{app}}^{-1} = \mu_{\text{ball}}^{-1} + \mu_{\text{eff}}^{-1},$$  \tag{17}

from the ballistic mobility

$$\mu_{\text{ball}} = \frac{v_{\text{ball}} L_{\text{ch}}}{2V_T}$$ \tag{18}

and the effective scattering related mobility

$$\mu_{\text{eff}} = \frac{v_{\text{ball}} \lambda_q}{2V_T}.$$ \tag{19}

The virtual source velocity $V_x 0$ in eq. (1) and eq. (16) is given by

$$V_x 0 = v_{\text{ball}} \left( \frac{\lambda_0}{\lambda_0 + 2L_q} \right).$$  \tag{20}

with the model parameter $v_{\text{ball}}$ as the ballistic carrier velocity and $L_q$ as the critical length defined by the distance over which the electric potential drops by $V_T$ from the virtual source point. For ballistic transport ($L_{\text{ch}}<<\lambda_0$ and $L_q<<\lambda_0$) $V_{\text{d,sat,s}}$ reduces to $2V_T$. This leads to very large values of the channel resistance for $V_{\text{dist}}<V_{\text{d,sat,s}}$. In order to increase the saturation voltage $V_{\text{d,sat}}$ in eq. (16), the following formulation is used

$$V_{\text{d,sat,q}} = \frac{p_{\text{qcl}} Q_{\text{ix0}}}{C_{\text{ch}}}.$$  \tag{21}

The original VS model can be recovered without changing the saturation voltage, i.e. setting $p_{\text{qcl}}=0$.

In the ballistic regime the implemented model equations can limit the output conductance and transconductance to the theoretical maximum values expected for the transistor operating in the quantum capacitance limited regime. For $V_{\text{dist}}>>V_{\text{th}},F_d=0$ and if additionally $V_{\text{d,sat,q}}>>2V_T$, one gets the drain current $I_{\text{d,sat}}=I_{\text{d,sat,q}}$. For ballistic transport ($p_{\text{qcl}}=1$) in the linear region $(V_{\text{dist}}<<V_{\text{d,sat}})$ $F_{\text{ds}}=V_{\text{dist}}/V_{\text{d,sat}}$ and thus $L_{\text{ch}}=C_{\text{qcl}} v_{\text{ball}}^{-1}$. In quantum capacitance limited operation, where $C_{\text{ox}}=C_q$, one gets $C_{\text{ch}}=C_q$ and thus, one can write the output conductance as $g_{\text{ds}}=W q_{\text{ch}} V_{\text{ball}}^{-1}$. For CNTFETs, the quantum capacitance for $V_{\text{dist}}>>V_{\text{th}}$ can be written as $C_{\text{qcl}}=4q^2/(h v_{\text{ball}})$. Then one gets $g_{\text{ds}}=2q_{\text{ch}} g_0$, where $q_{\text{ch}}=W g_0$ is the number of nanotubes in the channel and $g_0=2q^2/h$ is the quantum conductance (the additional factor 2 accounts for the two degenerate bands in the CNT channel).

Assuming the same conditions in saturation ($V_{\text{dist}}>>V_{\text{d,sat}}$) one can show that the transconductance approaches the theoretical limit of $g_m=2q_{\text{ch}} g_0$.

The charge model for $Q_s$ and $Q_d$ is based on [4],

$$Q_{s/d} = Q_{s/d,\text{dd}} (1 - F_{\text{sat,b}}) + Q_{s/d,\text{ball}} F_{\text{sat,b}}^2,$$  \tag{22}

where the drift-diffusion charge components are given by [5]

$$Q_{s,\text{dd}} = Q_{\text{ch}} \left[ 6 + 12 \eta + 8 \eta^2 + 4 \eta^3 \right] \frac{15(1+\eta)^2}{15(1+\eta)^2}$$  \tag{23}

and

$$Q_{d,\text{dd}} = Q_{\text{ch}} \left[ 4 + 8 \eta + 12 \eta^2 + 6 \eta^3 \right] \frac{15(1+\eta)^2}{15(1+\eta)^2}$$  \tag{24}

with

$$\eta = 1 - F_{\text{sat,b}}.$$  \tag{25}

The function

$$F_{\text{sat,b}} = f_b \frac{V_{\text{dist}}/V_{\text{sat,b}}}{\left[ 1 + (V_{\text{dist}}/V_{\text{sat,b}})^{\beta_{\text{ch}}} \right]^{1/\beta_{\text{ch}}}}$$  \tag{26}

with

$$V_{\text{sat,b}} = \frac{f_b V_T^2}{\left( Q_{\text{ch}} C_{\text{ch}} \right)^2} + (Q_{\text{ix0}}/C_{\text{ch}})^2,$$  \tag{27}

represents the field dependence of the channel charge similar to eq. (12) and eq. (15). The fitting parameter $f_b$ can be used to adjust the saturation voltage for the charge. The channel charge is given by

$$Q_{\text{ch}} = W g_L Q_{\text{ix0}}.$$  \tag{28}

The ballistic charge in eq. (22) is given by [4]

$$Q_{\text{ch}} = Q_{\text{ch}} \left[ \sinh^{-1} \left( \frac{f_b}{q_{\text{ch}}} \right) - \frac{\sqrt{k_q}}{k_q} - \frac{1 - \frac{1}{k_q}}{k_q} \right]$$  \tag{29}

and

$$Q_{\text{ch}} = Q_{\text{ch}} \left[ \sinh^{-1} \left( \frac{f_b}{q_{\text{ch}}} \right) - \frac{\sqrt{k_q}}{k_q} - \frac{1 - \frac{1}{k_q}}{k_q} \right]$$  \tag{30}

The new X-VS model has been applied to both experimental and TCAD generated data of a variety of device structures with different channel materials. The corresponding model parameter values are listed in Table 1.

Fig. 4 displays the comparison to measurements of a carbon nanotube (CNT) FET [6]. Here, the formulation of the transconductance behavior still needs some improvement. This also applies to highly linear CNTFETs which cannot be described with the present model formulations.

As shown in Fig. 5, good agreement with measurements of a 120nm channel length bulk Si-MOSFET has been obtained for both drain current, transconductance and transit frequency. The comparison to measurements of a 200nm InGaAs nanowire FET [7] in Fig. 6 also exhibits quite good agreement.

Additional devices with smaller channel lengths and from different technologies with carrier transport ranging from ballistic to diffusive have been modeled and will be shown elsewhere. In all cases, after adding capacitive and resistive parasitics from the metalization, at least satisfactory agreement has been obtained using the same compact model framework. This enables the exploration of device and circuit performance under realistic conditions and a fair technology comparison especially in terms of circuit design.

Table 1 X-VS-CM parameters for FETs from different technologies. Calculated parameters (from device physics) are indicated in italic.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Si</th>
<th>InGaAs</th>
<th>CNT</th>
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<td>FETtype</td>
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<td>Lch/μm</td>
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<tr>
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<td>-</td>
</tr>
<tr>
<td>Vth/V</td>
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<td>0.162</td>
<td>0.22</td>
</tr>
</tbody>
</table>

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REFERENCES


Fig. 4: Characteristics of a 100 nm MT-CNTFET [6] in comparison with the X-VS CM: (a) transfer characteristic (V_{ds} = -1.5V), (b) output characteristics (V_{gs}/V = 0, -0.4, -1.2, -2), (c) transconductance (V_{ds} = -1.5V), (d) output conductance (V_{gs}/V = 0, -0.4, -1.2, -2), (e) and (f) transit frequency and maximum oscillation frequency (measurement at V_{ds} = -1.5V and V_{gs} =-1.2V, simulations at V_{ds}/V = -0.5, -1, -1.5).

Fig. 5: Characteristics of a 120 nm bulk MOSFET in comparison with the X-VS CM: (a) transfer characteristic (V_{ds}/V = 0.05, 1.5), (b) output characteristics (V_{gs}/V = 0.3...1.5), (c) transconductance (V_{ds}/V = 0.05, 1.5), and (d) transit frequency (V_{ds} = 1V).

Fig. 6: Characteristics of a 200 nm InGaAs FET [7] in comparison with the X-VS CM: (a) transfer characteristic (V_{ds}/V = 0.05, 0.5), (b) output characteristic (V_{gs}/V = 0.2...1), (c) transconductance (V_{ds}/V = 0.05, 0.5), and (d) output conductance (V_{gs}/V = 0.2...1).