A Compact Model for SiC Junction Barrier Schottky Diode for High-Voltage and High-Temperature Applications

D. Navarro*, F. Herrera*, M. Miura-Mattausch*, H. J. Mattausch*,
M. Takusagawa**, J. Kobayashi**, and M. Hara**

*HiSIM Research Center, Hiroshima University
1-3-1 Kagamiyama, Higashihiroshima, Hiroshima 739-8530 Japan, dondee-navarro@hiroshima-u.ac.jp
**Toyota Motor Corporation, Aichi, Japan

ABSTRACT

SiC-based Junction Barrier Schottky (JBS) Diode is employed in power conversion applications because of its low-leakage current and high switching speed characteristics even at elevated temperatures. JBS structure originates from Schottky Barrier Diode (SBD) structure, with an addition of *p*+ implant to reduce the reverse current in SBD. In this work, we report a compact model developed for JBS. The model consists of the thermionic emission current occurring at the metal/SiC junction together with the resistive effects of the *p*+ implant in the lightly doped drift region of the diode. The developed model can calculate the current-voltage characteristics of JBS for varying geometries of the *p*+ implant without introducing model parameters. Measured current characteristics is well-reproduced for varying temperatures. The model is also applicable for the SBD structure.

Keywords: junction barrier schottky diode, schottky barrier diode, thermionic emission, sic, compact model

1 INTRODUCTION

SiC-based devices have achieved rapid technological development and commercialization owing to the wide bandgap and high critical field properties of SiC [1]. SiC-Schottky Barrier Diode (SBD) and Junction Barrier Schottky (JBS) Diode are employed in low threshold voltage and high switching speed circuits for power conversion applications [2, 3]. JBS is based on SBD as shown in Fig. 1. A *p*+ implant is added in the *n*− drift region below the metal contact. The implant creates a depletion region to minimize the large tunning current at reverse bias condition.

The goal of this work is to develop a unified model for JBS and SBD structures that can be utilized for circuit simulation. Existing models are either for SBD or JBS alone, which are based on fitting using ideality factor and macro-models [4-6]. Our approach is to model SBD based on thermionic emission theory combined with the resistive effect of the drift region. We extend the SBD model for JBS by considering the distributed resistance effects introduced by the *p*+ implant [7, 8]. 2D device simulation [9] and measurements are used to validate the developed model.

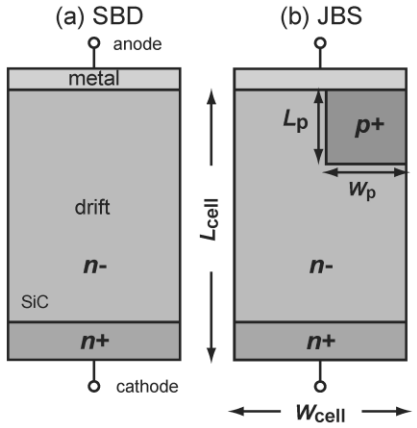

Figure 1: SBD and JBS diode structures.

2 SCHOTTKY BARRIER DIODE (SBD) AND JUNCTION BARRIER SCHOTTKY (JBS) MODELING

The transport of carriers across a metal-semiconductor contact follows the thermionic emission theory. The thermionic current I_{th} through the Schottky barrier at forward bias condition is [10]

$$I_{th} = \mathrm{AREA} \cdot A^* \cdot T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \cdot \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1)$$

$$\phi_B = \phi_M - \chi \quad (2)$$

where ϕ_B is the Schottky barrier height, ϕ_m is the metal work function, χ is the electron affinity, q is the unit charge, k is Boltzmann's constant, T is the temperature, V is the applied bias, and A^* is Richardson's constant.

The potential along the drift region which sustains the high electric field applied on the SBD device is shown in Fig. 2a. The potential reduces linearly which means that the drift region introduces a resistive effect. Thus, the equivalent circuit of the SBD model is a diode and a resistor connected in series as shown in Fig. 2b. The current through the resistor R_1 is

$$I_{R1} = V_{\mathrm{N1,cathode}} \Big/ \left(\frac{1}{q \cdot \mathrm{NEPI} \cdot \mu_0} \cdot \frac{L_{\mathrm{cell}}}{\mathrm{AREA}}\right) \quad (3)$$

where $V_{\mathrm{N1,cathode}}$ is the potential across R_1, L_{cell} is drift layer length, NEPI is the doping concentration of the drift region

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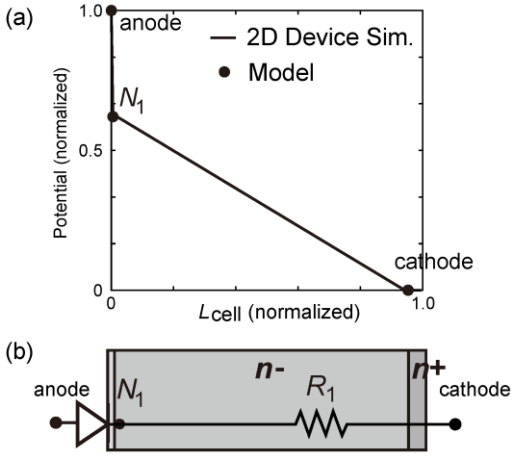

Figure 2: (a) Potential distribution along the drift region of the SBD. (b) Equivalent circuit of SBD model.

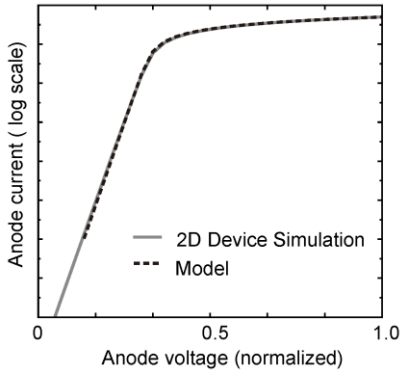

Figure 3: SBD current characteristics.

and μ_0 is the carrier mobility. The model can reproduce the current characteristics calculated by device simulation as shown in Fig. 3 without introducing any model parameters. The potential calculated by the model is denoted by circles in Fig. 2b. The temperature dependence is modeled as

$$I_{\text{th}} \cdot \left(\frac{T}{\text{TNOM}} \right)^{-\text{ISATTMP}} \tag{4}$$

where ISATTMP is a model parameter. At high bias, carriers acquire energy above the thermal energy due to the high field applied. The modification of high field mobility is modeled as

$$\mu = \frac{\mu_0 \cdot \left(\frac{T}{\text{TNOM}} \right)^{-\text{MUETMP}}}{\left(1 + \left(\frac{\mu_0 \cdot \text{ELEC}}{\text{VSAT}} \right)^{\text{BETA}} \right)^{1/\text{BETA}}} \tag{5}$$

where BETA is a model parameter. ELEC and VSAT are SiC-related parameters. At high temperature, the carriers are scattered due to phonons which reduces the effective mobility. Thus, the temperature-dependence is also modified for carrier mobility with model parameter MUETMP. TNOM is the nominal temperature. Fig. 4 shows the *I-V* characteristics of the model in comparison

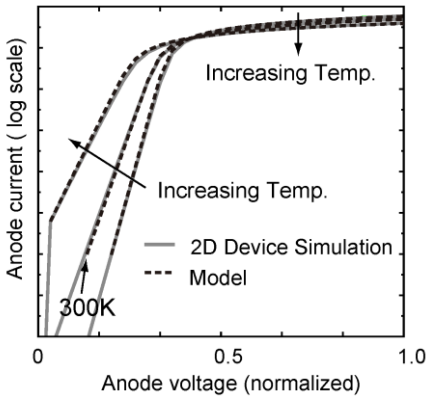

Figure 4: *I-V* characteristics at different temperatures.

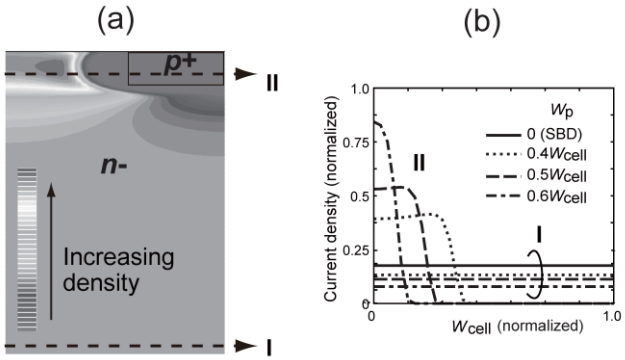

Figure 5: Current density distribution in SBD structure. (a) SBD cross-section. (b) Along lines I and II.

with 2D device simulation results at different temperatures.

To extend the SBD model to JBS, device simulation is performed to investigate the changes in carrier dynamics caused by the *p*+ implant. In JBS, the current density distribution becomes concentrated in the *n*− drift region adjacent to the *p*+ implant as shown in Fig. 5(a). Fig 5(b) shows the extracted current densities along I and II. As the width of the implant increases, the current density increases in the adjacent *n*− region while the carrier injection from the bottom decreases. Therefore, the *p*+ implant introduces a distributed resistance in the drift layer.

The relation of the current I_2 in the region with respect to I_0 and I_1 in the diode body is

$$I_2 = I_0 + I_1 \tag{6}$$

as illustrated in Fig. 6. Considering the geometrical relation of the effective widths [11], the relation

$$J_2 \cdot \left(W_{\text{cell}} - W_{\text{p}} \right) = J_0 \cdot \left(W_{\text{cell}} - W_{\text{p}} \right) + J_1 \cdot W_{\text{p}} \tag{7}$$

holds. For a uniform current in the body where J_0 is equal to J_1,

$$J_2 = J_0 \cdot \left[1 + W_{\text{p}} / \left(W_{\text{cell}} - W_{\text{p}} \right) \right] \tag{8}$$

is derived. Therefore, the increase of the current in the *n*− region near the *p*+ implant can be desribed using the geometry of the the implant.

Fig. 7(a) shows the potential distributions along the drift region of JBS for different W_{p} in comparison with the

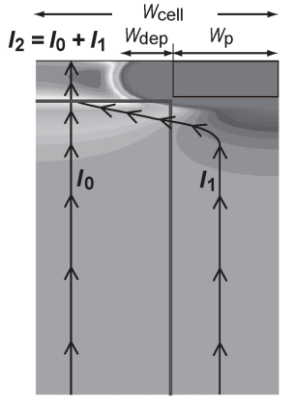

Figure 6: Current relation.

potential of SBD calculated by 2D device simulation. In JBS, the potential along the diode body is lower and bends up near the *p*+ implant length.

To model the change in potential distribution of JBS, an additional resistor R_2 is added in series with the diode and R_1 in the equivalent circuit of the model as shown in Fig. 7b. R_2 represents the distributed resistance of the *n*– region adjacent to the *p*+ implant. Considering Eq. 8, the currents through R_1 and R_2 are

$$I_{R_1} = qN_{\mathrm{d}}\mu \cdot \frac{AREA}{\left(L_{\mathrm{cell}} - L_{\mathrm{p}}\right)} \cdot V\left(N_1, cathode\right) \tag{9}$$

$$I_{R_2} = qN_{\mathrm{d}}\mu \cdot \frac{AREA'}{L_{\mathrm{p}}} \cdot \frac{1}{1 + W_{\mathrm{p}} / \left(W_{\mathrm{cell}} - W_{\mathrm{p}}\right)} \cdot V\left(N_2, N_1\right) \tag{10}$$

where

$$AREA' = AREA \cdot \frac{W_{\mathrm{cell}} - W_{\mathrm{p}}}{W_{\mathrm{cell}}} \tag{11}$$

AREA is the cathode area.

2D device simulation results in Fig. 6 show that depletion occurs around the *p*+/*n*– junction. The extracted depletion width along I in Fig. 5 is 0.3μm, which is almost non-varying for different W_{p}. The depletion width is then approximated as

$$W_{\mathrm{dep}} = \mathrm{WDEPTH} \cdot \sqrt{\frac{2\varepsilon_{\mathrm{SiC}} V_{\mathrm{bi,dep}}}{q \cdot \mathrm{NEPI}}} \tag{12}$$

where WDEPTH is a model parameter to approximate the effect of the potential between the *p*+ implant and *n*– regions.

$V_{\mathrm{bi,dep}}$ is calculated as

$$V_{\mathrm{bi,dep}} = \frac{kT}{q} \cdot \ln\left(\frac{\mathrm{NEPI} \cdot \mathrm{NIMP}}{n_i^2}\right) \tag{13}$$

where NIMP is the doping concentration of the *p*+ implant.

At reverse-bias condition, the term inside the square bracket in Eq. 1 can be neglected because the reverse bias voltage V_{r} is greater than kT/q. The leakage current is then written as

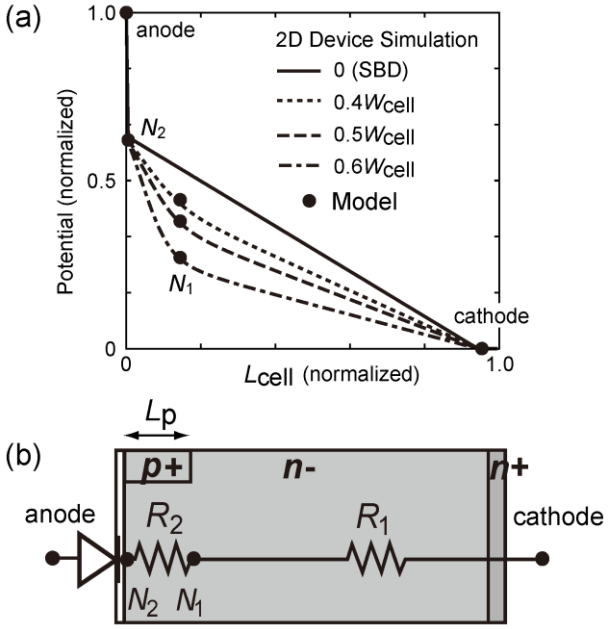

Figure 7: (a) Potential distribution along the JBS diode body. (b) Equivalent circuit of JBS model.

$$I_{\mathrm{th}} = -\mathrm{AREA} \cdot A^* \cdot T^2 \exp\left(-\frac{q\phi_{\mathrm{B}}}{kT}\right) \tag{14}$$

Schottky barrier height reduces because of image force lowering phenomena at reverse-bias condition. The electron in the *n*– body has a mirror image charge in the metal that produces electrostatic force. The barrier height reduction due to the phenomena is given by [10, 12]

$$\Delta\phi_{\mathrm{BL}} = BLM \cdot \sqrt{\frac{q \cdot E_M}{4 \cdot \pi \cdot \varepsilon_{SiC}}} \tag{15}$$

$$E_M = \sqrt{\frac{2 \cdot q \cdot NEPI}{\varepsilon_{SiC}} \cdot \left(V_R + VBI\right)} \tag{16}$$

where BLM is a model parameter. EM is the maximum electric field at the Schottky contact. ϕ_{B} in Eq. 14 is then reduced by ϕ_{BL}.

3 MODEL VERIFICATION

The model is verified to reproduce the *I-V* characteristics of 2D device simulation for different W_{p} by changing only the *p*+ geometry as shown in Fig. 8. The important potential nodes along the diode calculated by the model are shown in Fig. 7b.

The model calculation results is also compared with the *I-V* measurements of a JBS diode with $W_{\mathrm{p}} = 0.4W_{\mathrm{cell}}$ in Fig. 9 at different temperatures. Good agreement is achieved.

The model results of leakage current in comparison with 2D device simulation results is shown in Fig. 10(a). Fig. 10(b) shows the enlarged image focusing on the characteristics at reverse bias.

The model is written in Verilog-A, where the geometry of the *p*+ implant are implemented as instance parameters.

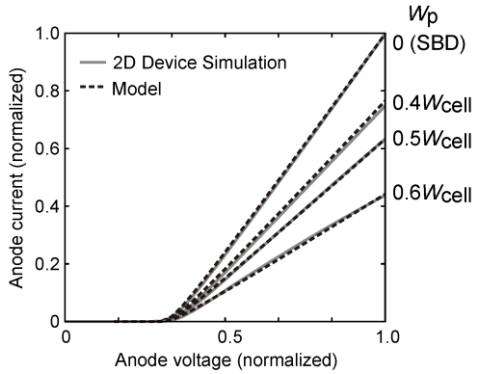

Figure 8: SBD and JBS model calculation results in comparison with 2D device simulation results for different *p*+ implant widths.

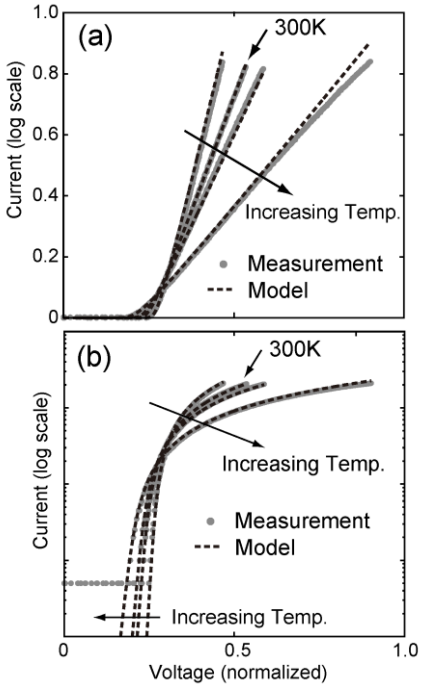

Figure 9: Forward current characteristics calculated by the model in comparison with measurement for W_p=0.4W_{cell}. (a) Linear and (b) log plots.

Therefore, the model can easily be utilized in SBD or JBS mode by changing only the *p*+ implant geometry.

4 CONCLUSION

A compact model for SBD and JBS diode structure is developed. The model consists of the thermionic emission current occurring at the metal/SiC junction together with the resistive effects of the lightly doped drift region and *p*+ implant of the diode. The developed model can calculate forward and reverse current characteristics as validated by 2D device simulations. Measured current characteristics at different temperatures is well-reproduced. The model can be utilized for optimizing JBS diode structures.

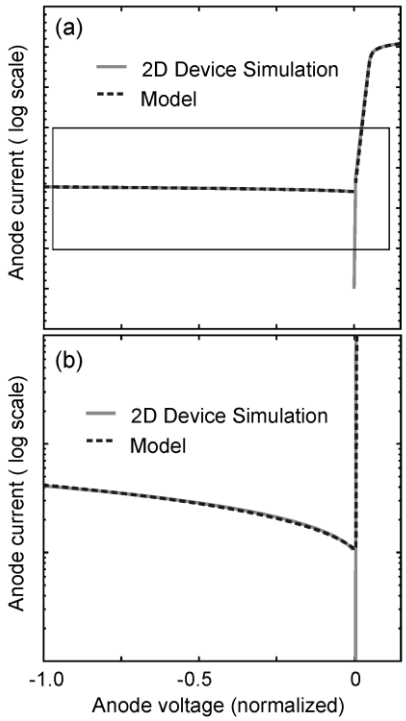

Figure 10: Leakage current due to image force lowering phenomena. (a) Negative to positive anode voltage. (b) Enlarged image of leakage current.

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