Analytical Surface Potential Solution for Low Effective Mass Channel Common Double Gate MOSFET

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ABSTRACT

An accurate and computationally efficient analytical solution for the surface potential is essential to develop a compact model for a transistor. In this work we propose an algorithm to solve the implicit surface potential equation for low effective mass Common Double Gate (CDG) MOSFETs that significantly simplifies the implementation of their compact model. The algorithm needs a single iteration to compute accurate solution for the surface potential equation. Drain current, and capacitances calculated using the algorithm are found to be in good agreement with numerical device simulation for a wide range of channel thickness, effective mass, oxide thickness asymmetry, and bias voltages. The proposed algorithm is implemented in a standard circuit simulator through its Verilog-A interface and simulation of standard circuits like CMOS inverter, NAND gate, flip-flop etc is demonstrated.

Keywords: surface potential, III-V, algorithm, double-gate MOSFET

1 INTRODUCTION

Owing to the inherent low effective mass (resulting into high mobility), III-V materials have been in the focus of semiconductor research for quite some time [1]. In our previous works ([1],[2]), we developed a compact model for long channel III-V material CDG MOSFETs. There we obtained completely physical expressions for surface potential Equation (SPE), drain current and terminal charges under quantum drift diffusion transport, compatible for a wide range of effective masses, material thickness, gate-oxide asymmetry and supply voltage in the devices. The SPE is an implicit equation, solution of which is necessary to implement the full-compact model. Hence it is imperative that a computationally efficient robust algorithm needs to be obtained to solve the implicit SPE [1].

Design of efficient and robust algorithms to obtain precise solutions of complicated surface potential equation has been a target for compact model developers [3]. In this work, our main objective is to obtain a computationally efficient algorithm to solve the implicit SPE [1] for low effective mass material CDG MOSFET and implement it in a standard circuit simulator. To the best of our knowledge, this work is the first that extends the quantum drift-diffusion formalism into circuit simulation, which has so far been limited only to device simulations.

2 ALGORITHM DEVELOPMENT

The input voltage equation for the long channel III-V material CDG MOSFETs is shown in (1), ([1],[2]). We use the first order Newton-Raphson algorithm to solve the implicit SPE using a smart initial guess. The initial guess helps in reducing the number of iterations necessary to converge. Subsequently we show that using this initial guess, it takes just one iteration of Newton-Raphson to obtain an accurate solution for the SPE.

$$(C^e_{oxf} + C^e_{oxb})(V_{GS} - \phi_m)$$

$$= U_t \sum_{i=1}^{n_{max}} C_{qi} ln(1 + e^{[\frac{q\phi_m - E_i - 0.5E_{g,se} - V}{kT}]}) \qquad (1)$$

In order to obtain a solution for ϕ_m from (1), we write (1) in following form,

$$f = (C^e_{oxf} + C^e_{oxb})(V_{GS} - \phi_m)$$

$$- U_t \sum_{i=1}^{n_{max}} C_{qi} ln(1 + e^{[\frac{q\phi_m - E_i - 0.5E_{g,se} - V}{kT}]}) \qquad (2)$$

Here, ϕ_m = electrostatic potential at zero electric field point inside the channel, $U_t = kT/q$, $C_{q,i}$ is the associated capacitance term for i-th sub-band ([1][2]), V_{GS} is the effective gate to source voltage, V =channel potential varying from 0 to V_{DS} from source to drain terminal, $E_{g,se}$ =band gap of the channel material, n_{max} =total number of sub-bands which is maximum 3 in our case. E_i is the i-th sub-band energy which is given as,

$$E_i = E_i^{(0)} - M_i'(V_{GS} - \phi_m) - M_i''(V_{GS} - \phi_m)^2 \qquad (3)$$

Here $E_i^{(0)}$ is sub-band energy under flat-band condition, M_i' and M_i'' are respectively coefficients of 1^{st} and 2^{nd}

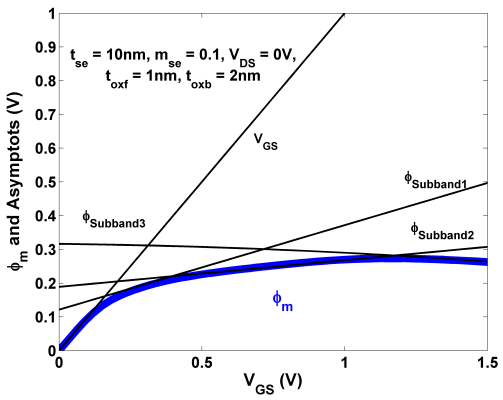

Figure 1: ϕ_m vs effective gate to source voltage plot along with asymptotes. Here the computation of ϕ_m has been done using exact numerical solution requiring multi-fold iterations.

order energy perturbation terms [1][2]. To obtain the solution for ϕ_m using a first degree Newton-Raphson algorithm, we need to find the first derivative $f\prime$ of f (2) with respect to ϕ_m,

$$f\prime = -(C^e_{oxf} + C^e_{oxb}) - \sum_{i=1}^{n_{max}} C_{qi} \frac{1 - \frac{M_i'}{q} - \frac{2M_i''}{q}(V_{GS} - \phi_m)}{1 + e^{[-\frac{q\phi_m - E_i - 0.5E_{g,se} - V}{kT}]}} \quad (4)$$

An initial guess $\phi_{m,init}$ is used in first order Newton-Raphson to have a quick convergence. We recall from [1],[2] that due to low effective mass channel material (III-V) and ultrathin dimension of the device, the carriers are strongly confined in different sub-bands, which results into the staircase pattern in the gate capacitance characteristics in [1] and [2]. We break (1) into sub-band-wise asymptotes ($\phi_{subband,i}, i \in \{1,2,3\}$), to work out an intelligent initial guess $\phi_{m,init}$. This is depicted in following Fig.(1).

Hence, considering $n_{max} = 3$, the algorithm can be summarized in three simple steps,

1. $\phi_{subband1(2)} = V_{GS} - \frac{\sum_{i=1}^{1(2)} C_{q,i}(E_i^{(0)} + V - V_{GS} + 0.5E_{g,se})}{\sum_{i=1}^{1(2)} C_{q,i}(\frac{M_i'}{q} - 1) - (C^e_{oxf} + C^e_{oxb})}$

   $\phi_{subband3} = V_{GS} - \frac{-c_b - \sqrt{c_b^2 + 4c_a c_c}}{2c_a}$

   where $c_a = \sum_{i=1}^{3} C_{q,i} \frac{M_i''}{q}$

   $c_b = \sum_{i=1}^{3} C_{q,i}(\frac{M_i'}{q} - 1) - (C^e_{oxf} + C^e_{oxb})$,

   $c_c = \sum_{i=1}^{3} \frac{C_{q,i}}{q}[E^{(0)} + 0.5E_{g,se} + q(V - V_{GS})]$

2. $\phi_{m,init}$
   $= min(\phi_{subband3}, min(\phi_{subband2}, min(\phi_{subband1}, V_{GS})))$

3. $\phi_m = \phi_{m,init} - f(\phi_{m,init})/f\prime(\phi_{m,init})$

As discussed in detail in [1] and [2], a major merit of this model is that it gives the designer the liberty to choose an appropriate n_{max} based on the the device dimension and material effective mass. In case the device has very high quantum confinement and $n_{max} \in \{1,2\}$, the designer just needs to ommit the $\phi_{subband3}$ term from the initial guess. In the following section, the proposed three step algorithm is validated against the device simulation obtained from ATLAS device simulator of the SILVACO TCAD suit [4]. The effectiveness of the algorithm in terms of maximum iteration taken and number of special functions taken is also discussed. The algorithm is implemented in SmartSpice circuit simulator of SILVACO TCAD suit [5] through its Verilog-A interface. Standard circuits like CMOS inverter, dual input NAND gate, level triggered D-flip flop and ring oscillator are simulated in SPICE using the low effective mass CDG MOSFET model described in [1], [2] .

3 RESULTS AND DISCUSSION

Table 1 shows the number of times the special functions (ln, exp and $\sqrt{\ }$) are called into the computation of the algorithm. The algorithm needs a maximum of one iteration ($MaxItr = 1$) for computation of the functions. The number of function calls scale with sub-bands used in the computation of (2). Similarly, as the iterations ($MaxItr$) used in computation increase, the number of function calls increase.

Figures 2 and 3 demonstrate the effect of sub-band variation on the drain current and gate to drain capacitance for varying drain and gate bias, using the proposed model. The results of the algorithm (line) are compared with those obtained through exact numerical simulation involving multiple iterations (star) and the TCAD data values (circles), which are all in good agreement. Further it could be noticed that modeling sub-band variation is critical to obtain the accurate drain current and gate to drain capacitance, since n_{max} determines the total charge density in the material.

Figures 4 and 5 show the DC and transient characteristics of a CMOS inverter implemented using the CDG MOSFET models described in [1] and [2] and the algorithm. The sub-band variation has significant impact on the switching delay of the transistor (Fig. 4). As the n_{max} reduces, the number of charge carriers and the average drain current through the MOSFET drops, resulting in increased delay.

Figures 6 and 7 portray a two input NAND gate and a NAND based level triggered D-flip flop.

The effect of sub-band variation is more pronounced in a 75-stage ring oscillator. Fig. 8 shows the output of a 75-stage ring oscillator, for a device of high quantum confinement with maximum supply voltage,

Table 1: Table showing number of special functions used in f and $f\prime$ (maximum iteration count: $MaxItr = 1$)

	ln	exp	$\sqrt{}$
f	$MaxItr * n_{max}$	$MaxItr * n_{max}$	0
$f\prime$	0	0	0
$\phi_{m,init}$	0	0	$MaxItr * 1$ (if $n_{max} = 3$), 0 (otherwise)

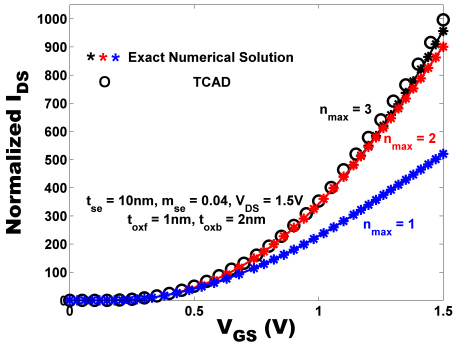

Figure 2: Drain current variation with gate voltage (Line: Algorithm).

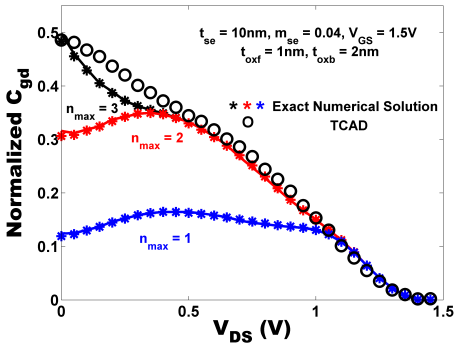

Figure 3: Gate to drain capacitance variation with drain voltage (Line: Algorithm).

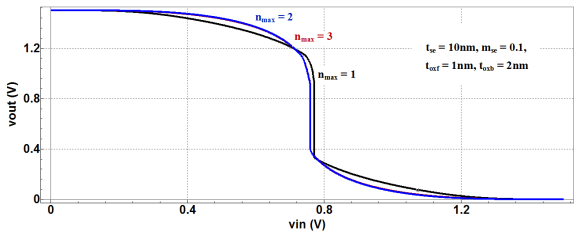

Figure 4: CMOS Inverter DC characteristics, including the effect of sub-band variation ($W = 1\mu m, L = 1\mu m$).

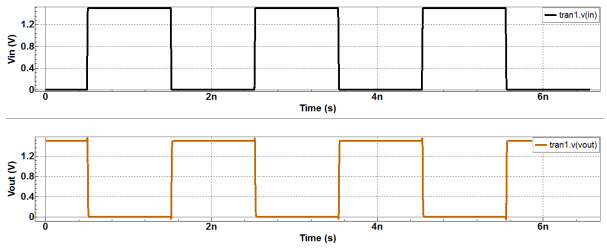

Figure 5: CMOS Inverter input and output waveform ($W = 1\mu m, L = 1\mu m$).

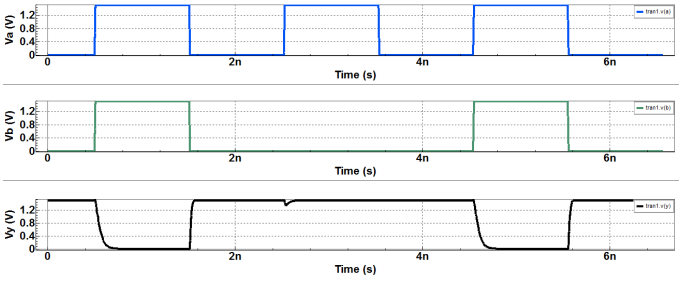

Figure 6: Dual input NAND gate input (1^{st} and 2^{nd} row) and output (3^{rd} row) waveform.

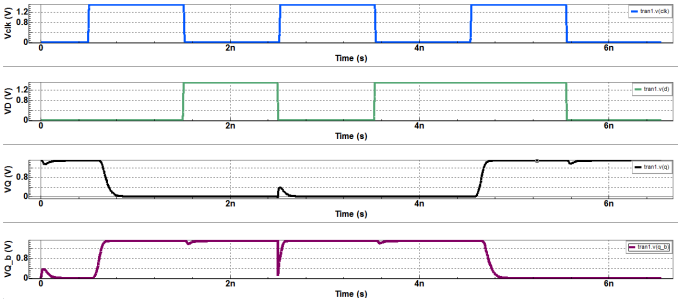

Figure 7: D-flip flop (level triggered) waveforms. Clock (1^{st} row), Input (2^{nd} row), Output (3^{rd} row), Inverted output (4^{th} row).

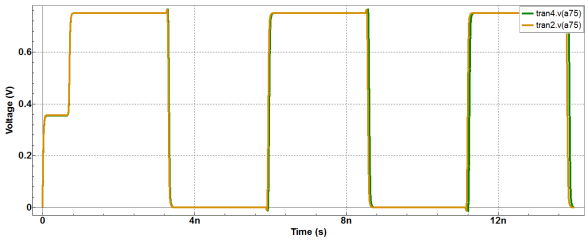

Figure 8: 75-stage ring oscillator output, including the effect of sub-band variation ($t_{se} = 7nm, m_{se} = 0.04, V_{supply} = 0.75V, t_{oxf} = 1nm, t_{oxb} = 2nm$).

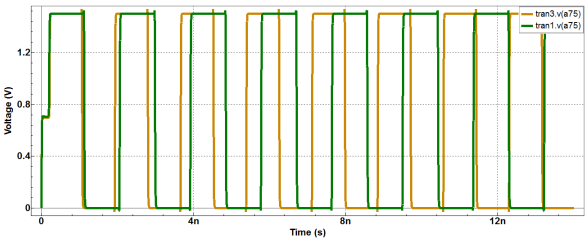

Figure 9: 75-stage ring oscillator output, including the effect of sub-band variation ($t_{se} = 7nm, m_{se} = 0.04, V_{supply} = 1.5V, t_{oxf} = 1nm, t_{oxb} = 2nm$).

V_{supply}, limited to a smaller value like 0.75V. In this scenario, the outputs obtained for $n_{max} = 1$(deep green) and $n_{max} = 2$(orange) are alike . Total simulation time as recorded in SmartSpice [4] run on an Intel(R) Core(TM) i5-3450 processor (3.1 GHz, 8 GB RAM), are $17.07Sec$ ($n_{max} = 1$) and $20.95Sec$ ($n_{max} = 2$). Hence in cases of high quantum confinement and low operating voltage, a designer can gain in terms of total simulation time ($\approx 20\%$ for the above case) by simply omitting higher sub-bands.

However, when the operating voltage V_{supply} assumes a higher value, higher sub-bands are activated in the device and notable difference is noticed in the obtained outputs (Fig. 9) for decreasing n_{max}. As the n_{max} considered reduces, the accuracy of the output reduces and subsequent output frequency also drops. Similar situation is observed for devices with lower quantum confinement, for $n_{max} \in \{2, 3\}$. In this case, the outputs for $n_{max} = 2$(orange) and $n_{max} = 3$(deep blue) match completely for lower operating voltage but not at higher operating voltage, as depicted in Figures 10 and 11.

4 CONCLUSION

A robust and computationally efficient surface potential solution for low effective mass material CDG MOSFET has been proposed. The model is completely physical and devoid of any empirical fitting parameter or polynomial. It captures the effect of quantum con-

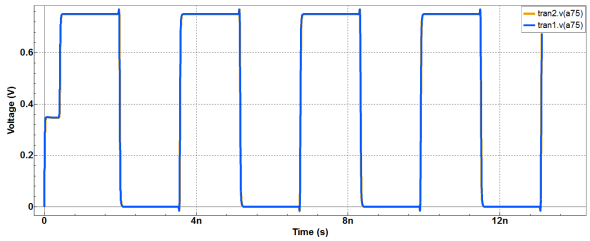

Figure 10: 75-stage ring oscillator output, including the effect of sub-band variation ($t_{se} = 10nm, m_{se} = 0.1, V_{supply} = 0.75V, t_{oxf} = 1nm, t_{oxb} = 2nm$).

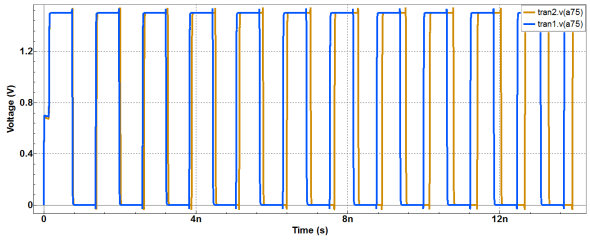

Figure 11: 75-stage ring oscillator output, including the effect of sub-band variation ($t_{se} = 10nm, m_{se} = 0.1, V_{supply} = 1.5V, t_{oxf} = 1nm, t_{oxb} = 2nm$).

finement through the sub-band variation. The proposed model is verified for accuracy over a wide range of channel thickness, effective mass, oxide thickness asymmetry and bias voltages using numerical device simulator. The model in implemented in a standard circuit simulator using its VerilogA interface and simulations for standard circuits like CMOS inverter, NAND gate, flip-flop etc are demonstrated using the proposed model.

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