Hybrid Process Design Kit: Single Chip Monolithic III-V/Si Cascode GaN HEMT

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Abstract

Double-layer bond-and-transfer (DL-BaT) process seamlessly integrates GaN HEMT and MOSFET on a common Si substrate. SMART-LEES hybrid process design kit (slh-PDK) in DL-BaT process platform offers monolithic III-V/Si designs under the commercial EDA toolsets for circuit designers.

This paper proposes the new design of a monolithic III-V/Si cascode GaN HEMT (M-CGH) in DL-BaT process platform. The design allows many M-CGHs to be fabricated in a single chip design, with electrical interconnections between GaN HEMT and Si MOSFET terminals being formed through CMOS back-end-of-line (BEOL) multi-level metallization processes. The slh-PDK allows a design to trace the parasitics in the post-layout simulation that is normally cannot be performed by the co-packing of a discrete cascode GaN HEMT (CGH) in one module.

Once the design of M-CGH with different types of device geometry configurations has been fabricated and proven on 8-inch multi-purpose wafers (MPW), the parameterized cell of M-CGH can be created and offered in the slh-PDK for circuit designers. The slh-PDK will then allow circuit designers to perform M-CGH SPICE simulation, layout design and verification. Most importantly, the slh-PDK provides cell-mapping for parasitic extraction and back-annotation of a design. It provides unlimited M-CGHs to be incorporated in a single chip design.

Keywords: Hybrid, integration, process design kit (PDK), SPICE, parametric cell, cascode GaN HEMT, MOSFET, III-V, Au-free, multi-purpose wafer (MPW), enhancement, depletion, foundry, tape out.

1. INTRODUCTION

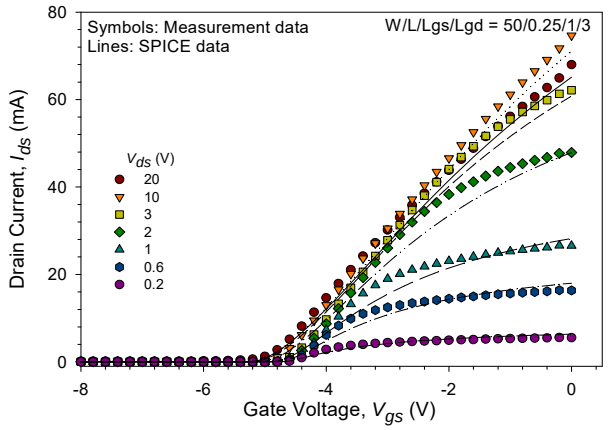
A GaN HEMT is a field-effect transistor with two dimensional electron gas (2DEG) as the electrical conduction channel. Aggressive research and development of GaN HEMT in various applications have been reported in the literature due to the advantageous material properties such as wide band-gap, high electron mobility, and high conductivity that offer large channel current, high breakdown voltage, and high power density. This makes GaN HEMTs the key building blocks for microwave [1–2] and power conversion [3–4] technologies.

The conventional depletion mode GaN HEMT (DGaNH) is conductive at zero gate bias voltage. It operates in the depletion mode with typical threshold voltage around –4 V due to high-density 2DEG being induced by spontaneous and piezoelectric polarization effects in the AlGaN/GaN heterostructure. An enhancement mode GaN HEMT (EGaNH) can also be made by more processing steps in comparison with a DGaNH. The current technique to fabricate EGaNH includes the use of a recessed-gate structure and a thin [5] AlGaN barrier layer capped by AlN layer to reduce 2DEG density, implanted AlGaN barrier layer to easily deplete the channel under the gate for normally-off operation or the use of Mg-doped p-Gate [6] in GaN HEMT fabrication process. However, there are reproducibility concerns regarding EGaNH process due to the complicated fabrication steps involved. Furthermore, the device features a narrow gate voltage swing that may require highly accurate control to prevent spikes.

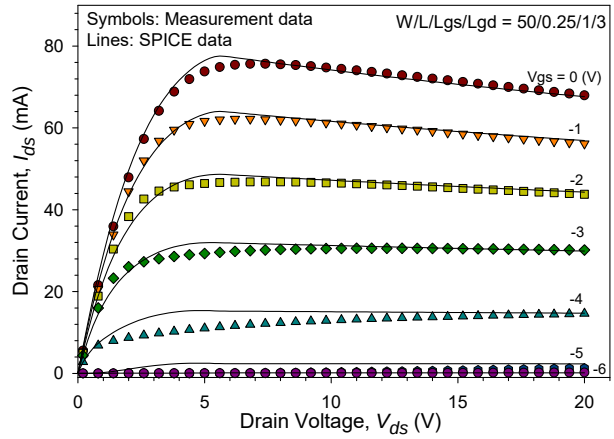
The driving voltage of a DGaNH could be from –30 to 2 V and around –4 V is required to fully turn on the device. This provides a better margin in comparison with an EGaNH. However, the negative drive voltage of DGaNH devices makes it challenging to drive the devices using conventional CMOS gate driver circuits that are usually designed for positive drive voltages in existing Si-CMOS technology. The combination of a DGaNH with a Si-based MOSFET forms a CGH which operates as an enhancement mode device, making it a better choice for the integration with conventional Si-CMOS positive gate drivers.

Commercial CGHs can be obtained in the form of TO-257 style metal package [7] on a direct bond copper AlN substrate in a metal-encapsulated package, or TO-220 on a heat sink. Wire bonding is usually used to form the electrical connectivity between the GaN HEMT and the Si MOSFET terminals in discrete packages. Unnecessary parasitics may be induced in discrete modules that cannot be traced in a design for back-annotation. Furthermore, the number of CGHs in one module is usually limited due to

the limited number of pads in co-packaging approaches. In this paper, we use the DL-BaT process [8] developed by SMART LEES to seamlessly integrate GaN HEMT and MOSFET on a common Si substrate to form M-CGH.



(a)

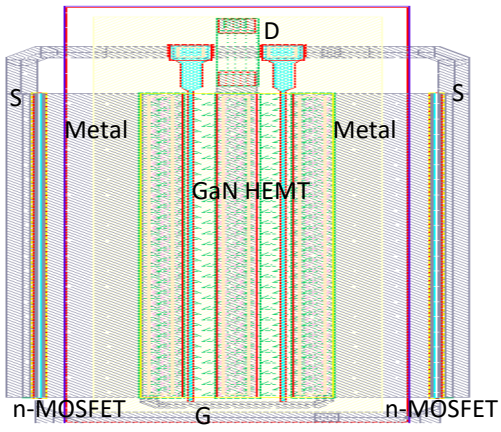


(b)

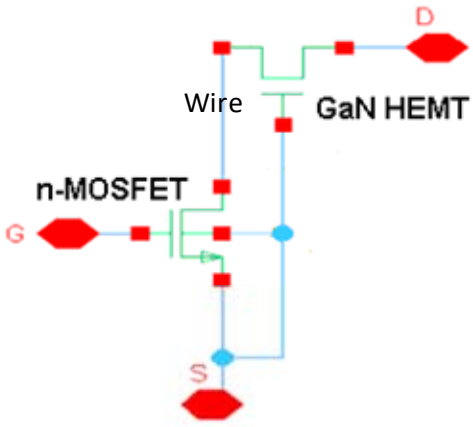
Figure 1: Comparison of the (lines) SPICE data with (symbols) measurement data in the (a) transfer and (b) output characteristics of a 2-finger DGaNH.

This approach allows many M-CGHs to be fabricated in a single circuit, with electrical interconnections between GaN HEMT and Si MOSFET terminals being formed through CMOS BEOL multi-level metallization process. This allows the parasitic extraction and back-annotation of an integrated circuit designed with M-CGH as one of the components in the design.

The DL-BaT integration process is seamlessly integrated with a standard 0.18-µm CMOS process, and we have created a slh-PDK [9] by augmenting the CMOS foundry's PDK that allows circuit designers to perform monolithic integrated circuit design using Si-CMOS and III-V devices. It supports SPICE simulation, layout design, design verification, and tape out of a circuit design under the commercial EDA toolsets.



(a)



(b)

Figure 2: The design of M-CGH with a 2-finger DGaNH in series connection with a 2-finger n-MOSFET. It shows the symmetric design in (a) layout with metal connections and (b) schematic with wire connections between DGaNH and n-MOSFET terminals.

We have used the slh-PDK to design M-CGH with different device geometries and configurations. These devices will be sent for fabrication on a multi-project wafer (MPW) using the SMART LEES integration process, and the measurement data obtained will be used to develop PCELL in the slh-PDK. M-CGH PCELL will be subsequently offered in the slh-PDK for circuit designers, as a design option besides the base DGaNH devices.

2. Design of Cascode GaN HEMT in monolithic CMOS/III-V Fabrication Platform

The base of DGaNH device is a 2-finger L = 0.25-µm and W = 50-µm GaN HEMT with drain and source recess regions of 3-µm and 1-µm, respectively. The device was developed by SMART-LEES [10], and was used to calibrate a GaN HEMT compact model that has been incorporated in the slh-PDK. The layout and schematic

symbol of DGaNH are drawn using commercial EDA toolsets to form one of the PCELL instances in the slh-PDK. The SPICE playback (lines) is shown in Fig. 1 for the output and transfer characteristics in comparison with the measurement data (symbols).

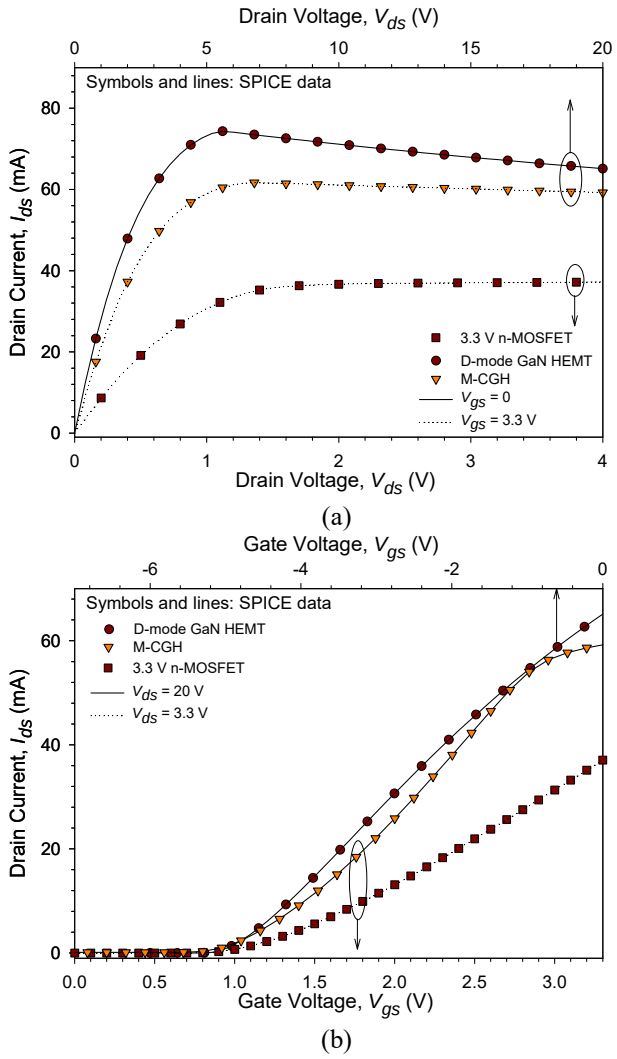


Figure 3: Comparison of (triangle) M-CGH with (circle) D-mode GaN HEMT and (square) n-MOSFET in the simulated (a) transfer and (b) output characteristics.

n-MOSFET from the CMOS foundry is selected from a device list through the slh-PDK for the design of M-CGH. The slh-PDK provides seamless SPICE simulation of M-CGH with DGaNH and n-MOSFET devices. The terminals of DGaNH and n-MOSFET are connected together by net wires in the schematic as shown in Fig. 2(b) for SPICE simulation. The terminals are physically connected by metals as shown in Fig. 2(a) in the layout design of M-CGH. The design of M-CGH has three terminals, namely, drain, source, and gate, as shown in Fig. 2 and labeled as D, S, and G. The D and S terminals of M-CGH are the drain and source terminals of DGaNH, and the G terminal is the gate terminal of n-MOSFET. It shows one 2-finger DGaNH in series connection with two one-finger n-MOSFETs in the layout. n-MOSFET in Fig. 2(b) is one 2-finger n-MOSFET represents two 1-finger n-MOSFETs in Fig. 2(a) that are symmetrically connected to one 2-finger DGaNH. The design shown in Fig. 2 has passed the layout-versus-schematic (LV) verification check. The layout in Fig. 2(a) shows M-CGH in the symmetric configuration with device width of 50 µm within the area of 56 x 83 µm^2.

Other M-CGH configurations can also be constructed by changing the device geometry such as the length of the drain recess region of a DGaNH or choosing 3.3/5V options of an n-MOSFET. The width of both devices in M-CGH configuration is set to the same value.

3. Simulations and The Test Structures

An exemplar M-CGH configuration is a DGaNH (2-finger W/L = 50/0.25-µm with drain and source recess regions of 3 and 1-µm, respectively) in series connection with a 2-finger 3.3V n-MOSFET (W/L = 50/0.7-µm). The calibrated model cards of DGaNH and 3.3V n-MOSFET in the slh-PDK are used to simulate the electrical characteristics of M-CGH and its individual devices. Fig. 3 shows the simulated data of M-CGH (triangle), compared with DGaNH (circle) and n-MOSFET (square). Besides the drain current of GaN HEMT and M-CGH being roughly twice that of n-MOSFET, both can be operated at higher drain voltage than n-MOSFET to supply higher power as shown in Fig. 3(a).

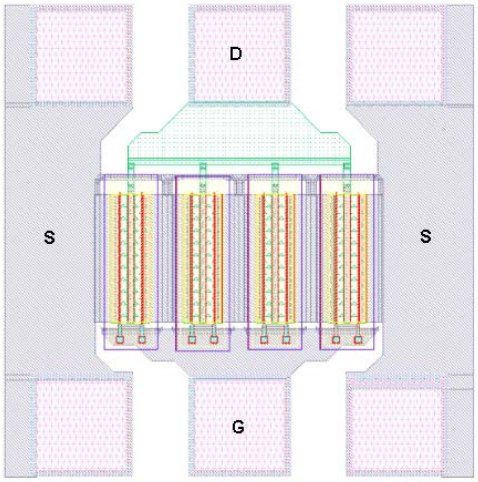


Figure 4: One of the demonstration structures to show a 4-finger M-CGH configuration with D, S, and G terminals in PCELL formation.

While the DGaNH and M-CGH achieve comparable drain currents for a given gate overdrive, it can be seen that the M-CGH (triangle in Fig. 3(b)) turns on at a positive gate drive voltage as compared with the DGaNH (circle in Fig. 3(b) that operates as a depletion-mode device. This makes M-CGH more attractive than DGaNH for circuit designers

due to the greater ease of designing positive gate drivers in Si-CMOS platform.

Another M-CGH demonstration structure is shown in Fig. 4 with D, S, and G terminals labeled on the pads. It shows a PCELL instance with four M-CGHs being connected in parallel to form a 4-finger M-CGH. It provides four times more drain current through D terminal at the pad than the current shown in Fig. 2(a). The structure in Fig. 4 can be created by M-CGH PCELL that allows circuit designers to view the list of editable parameters that control the total number of M-CGHs in PCELL formation, the drain-recess and gate lengths of each DGaNHs, and the type of n-MOSFET (e.g., 3.3V and 5V options).

The electrical characteristics and the breakdown performance of M-CGH are dependent on the geometry and the choices of the selected n-MOSFET. Along with the design of M-CGH and fabrication, SPICE characterization structures have been drawn in a layout to fabricate DGaNH in different geometric configurations for the development of M-CGH PCELL.

Looking at potential microwave and high-voltage applications, 2-finger DGaNH with 3/6/10-µm drain recess and 0.25-µm gate lengths and 3.3/5V n-MOSFET have been selected for the design of M-CGH in different configurations. The pads for M-CGH test structures have been arranged with the pitch between pads that are suitable for RF measurement in 100/150-µm G-S-G configurations.

4. Summary

DL-BaT process to seamlessly integrate GaN HEMT and MOSFET on a common Si substrate offers a new approach to designing M-CGH. The slh-PDK allows circuit designers to use M-CGH in integrated circuit designs for microwave and high-voltage applications. The net wire and physical metal connecting the terminals of the devices to form M-CGH in the schematic and the layout, respectively, enable parasitic extraction and back annotation of an integrated circuit designed with the slh-PDK.

The design of M-CGH has been presented with one of the configurations to demonstrate the electrical characteristics in comparison with its constituent DGaNH and Si MOSFET devices. M-CGH offers positive drive voltage with comparable amount of output power to a DGaNH.

The design of M-CGH with different types of device geometry configurations has been sent for fabrication on 8-inch multi-purpose wafers (MPW). All fabricated M-CGH in this work will be measured. The measurement data and the layout of the design will be used to develop PCELL in the slh-PDK. M-CGH PCELL will be offered in the slh-PDK for circuit designers.

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