Electric Field Assisted Placement of Carbon Nanotubes Using Sacrificial Graphene Electrodes

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ABSTRACT

Here we detail a complete process flow to overcome the challenge of placement of carbon nanotubes on solid surfaces, limiting "bottom-up", large-scale integration in semiconductor process technology. To date most bottom up placement strategies are based on surface functionalization having the drawback that chemical modifications can deteriorate the deposited carbon nanotubes. The application of dielectrophoretic techniques eliminates the chemical treatment, however, it necessitates the usage of conductive electrodes typically made out of metal. These metallic electrodes limit performance, scaling, and density of integrated electronic devices. Here, we report a method for electric-field assisted placement of purely semiconducting carbon nanotubes from solution at predefined locations by means of large-scale graphene layers having patterned nanoscale deposition sites. The patterned graphene layers can be removed residue-free after carbon nanotube deposition. In order to demonstrate the application potential, we have assembled at predefined substrate locations carbon nanotubes of varying density and integrated them into field-effect transistor. The graphene-based placement process, implemented with nanoscale resolution at wafer scale, could enable mass manufacturing of application-specific electronics based on carbon nanotubes.

Keywords: graphene, carbon nanotubes, nanoelectronics, dielectrophoresis, placement

1 INTRODUCTION

Deterministic placement of carbon nanotubes with nanoscale precision is the key challenge preventing its large-scale integration into modern micro-/nanoelectronics. Assembly methods based on chemical functionalization of surfaces[1] typically lead to degraded material quality with regards to electronic performance.

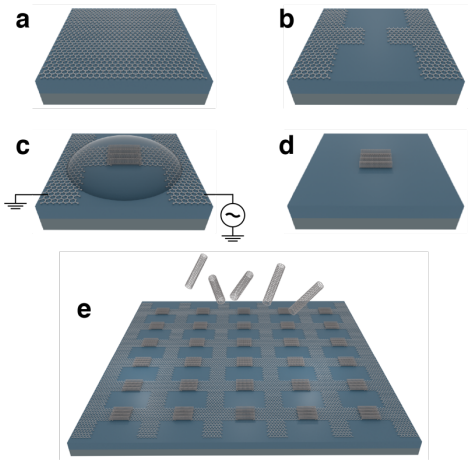

Figure 1: 3D illustration of sample fabrication flow. As transferred or grown graphene (a) is patterned (b) defining local deposition sites. (c) Carbon nanotubes are deposited from solution at pre-defined locations determined by the structured graphene. (d) Remaining carbon carbon nanotubes after graphene is removed. (e) High density assembly of carbon nanotubes by using large-scale patterned graphene.

The usage of electric-field driven assembly techniques[2] eliminate the necessity for chemical modifications. Electric-field assisted methods however require the presence of conductive electrodes that limit the performance, scaling, and density of integrated electronic devices[3]. Here, we detail a method for electric-field assisted placement of solution-processed carbon nanotubes by using large-scale, patterned graphene layers featuring predefined deposition sites. The patterned graphene layers are prepared by either transfer on to or synthesis on standard substrates, then are removed residual-free after nanotube deposition is completed, yielding carbon nanotube assemblies with nanoscale resolution that cover surface areas larger than 1mm^2. This graphene-based placement technique affords nanoscale resolution at wafer scale, and could enable mass manufacturing of carbon nanotube nanoelectronic[4], [5] and optoelectronic devices[6].

2 RESULTS

In Figure 1, we visualize the process flow of using patterned graphene layers in combination with electric-field assisted placement to assemble carbon nanotubes in predefined locations. We start with large with large-scale graphene layers prepared by direct synthesis[7],[8] on substrate or transfer on to the desired target substrate[9].

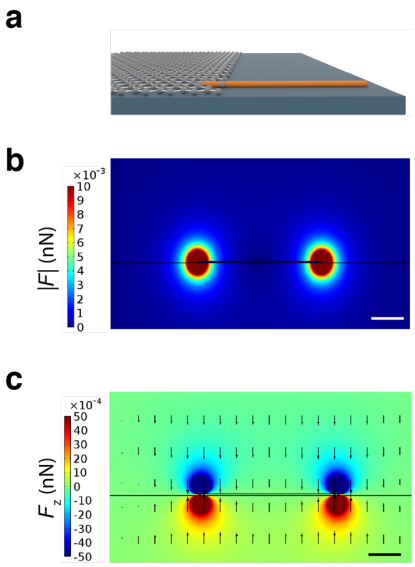

Figure 2: (a) 3D illustration of a single carbon nanotube on top of graphene showing the flat contact area between nanotube and graphene avoiding any bending. (b) Electric-field simulation showing the magnitude of the dielectrophoretic force generated by an AC voltage applied to a single graphene layer. (c) z-component of the dielectrophoretic force effectively pulling a carbon nanotube towards the graphene layer. Scale bars are 50nm.

Next, graphene layers are patterned by a combination of e-beam lithography and reactive plasma etching to form local deposition sites with nanometer resolution of arbitrary shape[10]. Carbon nanotube placement is achieved by applying an alternating voltage to the patterned graphene and dispensing a small volume of a highly diluted carbon nanotube suspension[11]. After carbon nanotubes have been placed, we remove the graphene layer by again a combination of e-beam lithography and reactive plasma etching. In Figure 2, we perform electric-field simulation to verify the suitability of using graphene as a conductive electrode for electric-field assisted placement of carbon nanotubes. The simulated electric field distribution is strongly localized at the edges of the graphene layer. This provides ideal deposition conditions right at the substrate surface. An addition benefit compared with a standard metal electrode is the reduced bending at the contact edge, which reduces the probability of device breakdown[12], [13].

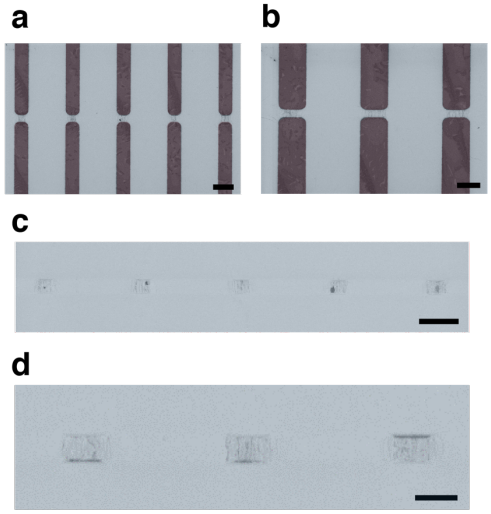

Figure 3: (a),(b) False color scanning electron micrographs of patterned graphene deposition sites (red) and carbon nanotubs inside depostion gaps after dielectrophoresis. (c),(d) False color scanning electron micrographs of remaining carbon nanotubes after graphene has been removed. Scale bars are 2µm

In Figure 3, we present an example of carbon nanotube deposition between pairs of structured graphene placement electrodes on top of silicon having an 300nm silicon oxide layer. The scanning electron micrographs clearly show the versatility of the method that allows us to control position and density of carbon nanotubes simply by adjusting the layout of the graphene placement electrodes. In this case carbon nanotubes have been deposited by sourcing an alternating voltage V_{pp}=10V at a frequency f=1MHz while simultaneously applying small amount (50µl) of highly diluted semiconducting nanotube suspension[14]. As is apparent from the microscopy images nanotube deposition only occurred inside the gap between electrodes without any auto-deposition outside the gap region demonstrating the high level of control this method offers. Post-deposition we remove the graphene electrodes by patterning a negative bi-layer resist (PMMA/HSQ) to protect the nanotubes and etch all exposed graphene layers by reactive ion etching. The final

result as shown in Figure 3c,d are arrays of nanotubes deterministically placed ready for further processing, i.e. integration into electronic or optoelectronic devices.

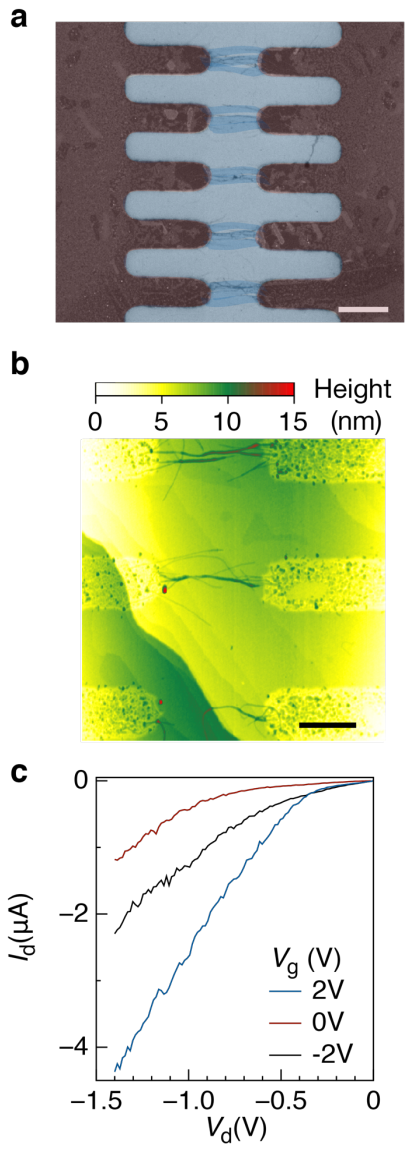

Figure 4: (a) False color scanning electron micrograph of as deposited carbon nanotubes (blue) between graphene placement electrodes (red). Scale bar is 1μm. (b) Atomic force microscope image from (a). Scale bar is 500nm. (c) Electric transport output characteristic I_d-V_d of one carbon nanotube device after graphene removal and metal contact fabrication.

In Figure 4, we provide another example of carbon nanotube placement but with sub-micron graphene deposition sites. We characterize as-deposited samples by atomic force microscopy. Measurements reveal that the deposited material mainly consists of individual nanotubes and small bundles. In order to demonstrate the viability of the method for electronic device integration we pattern metallic contacts on top of the nanotubes providing an electrical interface for device probing. We operate as-fabricated devices in a field-effect transistor configuration by applying a bias voltage across the nanotubes while varying the gate bias voltage to the underlying silicon acting as a global back gate electrode. In Figure 4c we plot an exemplary electric output characteristic I_d-V_d exhibiting clear semiconducting behavior as expected from the highly refined nanotubes source material[14].

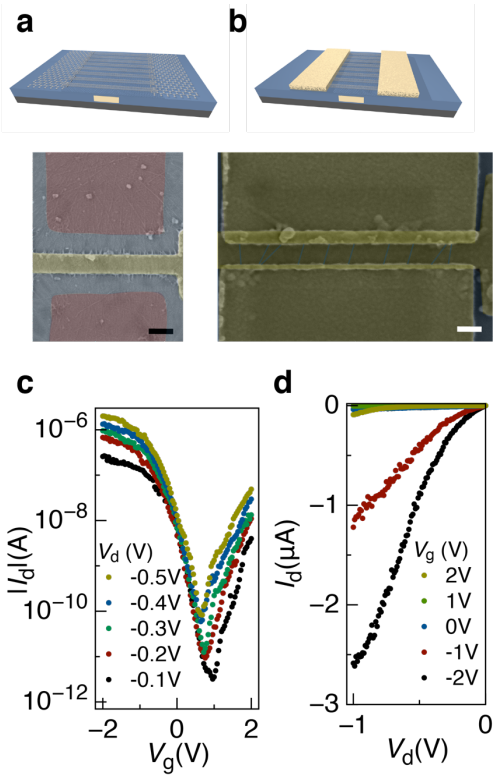

Figure 5: (a) 3D rendering and false color scanning electron micrograph from a highly integrated device architecture. Scale bar is 200nm. (b) 3D rendering and false color scanning electron micrograph from an as fabricated nanotube device. Scale bar is 100nm. (c), (d) Electric transport transfer I_d-V_g and output characteristic I_d-V_d of carbon nanotube device with local bottom gate.

In Figure 5, we employ an integration scheme that allows for fabrication of nanotube electronic devices with competitive performance. To that end we fabricate embedded local bottom gate electrodes with a thin high-k gate insulator prior to nanotube deposition and device fabrication. Local bottom gates are prepared by patterning with e-beam lithography followed etching of silicon oxide, subsequent refill with metal, and a lift-off process. A 20nm thin Al_2O_3 gate oxide is formed by atomic layer deposition. From this point subsequent steps are identical to the device in Figure 3c. In Figure 5c,d we plot the electric transfer I_d-V_g and output characteristic I_d-V_d, respectively. We observe ambipolar device behavior with good sub-threshold swing (ca. 200mV/dec) and current saturation at moderate bias voltages. This integration scheme further demonstrates the versatility and strength of the presented deposition method

not possible with conventional metallic placement electrodes.

3 SUMMARY AND CONCLUSION

In summary, we developed a method for electric-field assisted placement of solution-processed carbon nanotubes by using patterned, sacrificial graphene layers. This method is compatible with conventional semiconductor processing and can be applied to various device concepts and substrates used in industry. It allows for further device scaling and complex integration processes with possible extension to wafer-scale device manufacturing. Ultimately, this presents a method applicable to a wide range of nanomaterials as a route to bottom-up integration.

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