CarrICool – the Innovative 3D Interposer Platform for HPC Systems: Analysis, Simulations, Optimization, Practice for Reliability Improvement and Performance Increase

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ABSTRACT

This paper presents specific solutions dedicated for HPC computer systems to extend critical capabilities of integrated circuits performance by application of the innovative interposer module with special attention paying on signal integrity issues. Research efforts [2][4] performed by European FP7 project CarrICool [1] consortium are focused on several fields like Integrated Circuits (IC) cooling efficiency improvement to reach the level of 600W/cm^2 by development of embedded microfluidic structures. Optical communication by dedicated IC interconnects, optimized power delivery by distributed buck converters and electrical communication up to 10GHz assured by optimized 3D interconnecting structures are also in scope of CarrICool R&D activities.

Keywords: 3D interposer, 3D integration, TSV, signal integrity, CarrICool, cooling, modeling, simulation, RF.

1 TECHNOLOGY CHALLENGES

The CarrICool ("Modular Interposer System Architecture providing scalable Heat Removal, Power Delivery and Optical Signaling") project [1] focuses on development of the multifunctional interposer (Fig. 1) for 3D system packaging and integration with respect to key issues from the heat removal, power delivery, optical signaling and signal integrity. The interposer fabrication technology development covers innovative design rules formulation, modeling, simulations and the fabrication followed by the real measurements of the CarrICool demonstrators along with results evaluation. The research activity on technology covers development on corrosion resistant cooling microfluidic channels, on sealings, on 3D interconnects, on bulk inductances, buck converters etc. The research is focused on integration of stacked HPC chips in thermal, electrical and mechanical domains. Therefore, the CarrICool project team pursues on development of the new, modular, multi-functional and scalable platform providing granular, interposer-level (embedded) local power delivery system, scalable highly efficient cooling technology integrated with innovative (or adapted) vertical signal transmission and optical signaling solutions. The IC technology pursuit to fit increasing number of transistors in a single chip forces cutting edge technologies to dive with feature size (now below 20nm) facing subsequent hardware issues (mismatch, stability, leakages, etc.) signal transmission problems and heat dissipation constrains.

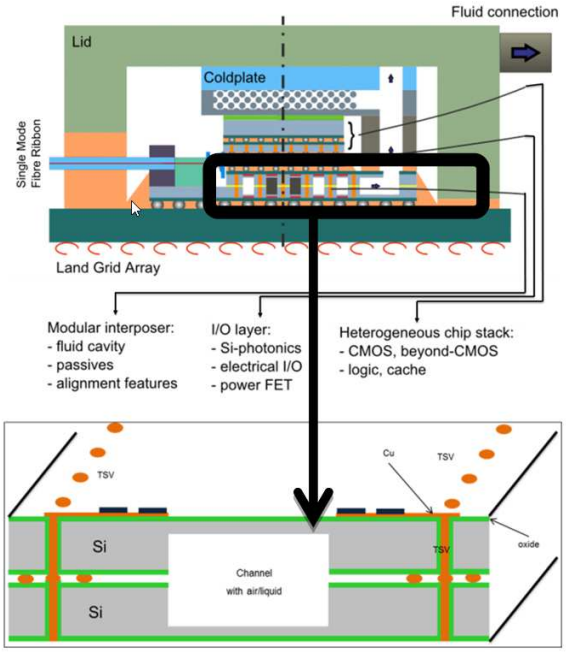


Fig. 1. The CarrICool interposer concept capable to encapsulate in a single stacked structure the microprocessor (the heater and signaling device), heat removal interposer with liquid connectors and liquid cooling media, distributed power supplies, optical and electrical signaling internal connectors and interfaces [1].

Local power dissipation in a single chip scale pushes designers to develop more power efficient solutions to handle with increasing power densities and to develop solutions capable to cool down powerful microprocessors, memories etc.

2 SIGNAL INTEGRITY

The CarrICool project research was focused on the technology made available for project partners (like ITE) to select the most universal structures of electrical routes (coplanar, coaxial etc.), routes geometry, mechanical layers specification (material thickness, resistivity), vertical routing layout components (profiting from TSV availability) to achieve internal compatibility of the interposer with cooling systems (cooling liquid proximity to TSV, metal lines), electrical shielding options, power delivery etc. to push it forward beyond the constrains faced

by HPC designers to satisfy their visionary demands. As it has emerged from the simulations performed, losses related to the redistribution layer (RDL) thickness stabilize for RDL thickness over 1µm (Fig. 2a) copper layer. Therefore 3µm-thick copper RDL technology variant has been selected as offered by the FhG IZM-ASSID partner [3][5].

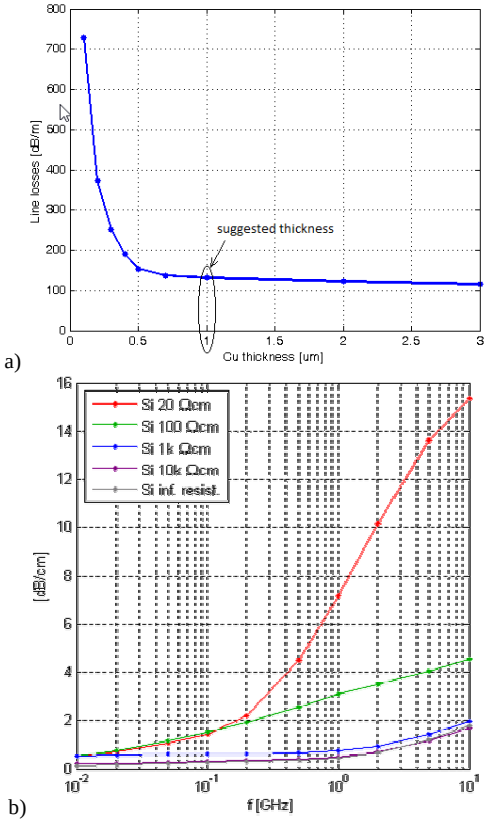


Fig. 2. Simulation results on optimization of CarrICool interposer on: a) RDL metallization thickness for: a) signal integrity losses criteria b) Substrate resistivity optimization for signal integrity modeling purposes. Losses [dB/cm] up to 10GHz for various substrate resistivities. Simulations of coplanar lines GSG type 20/15/20 (20µm width, 15µm spacing).

Similarly, high resistivity substrates (not below 1kΩcm) are necessary to lower transmission losses for signals over 1GHz down to acceptable (lowest level) criteria (Fig. 2b).

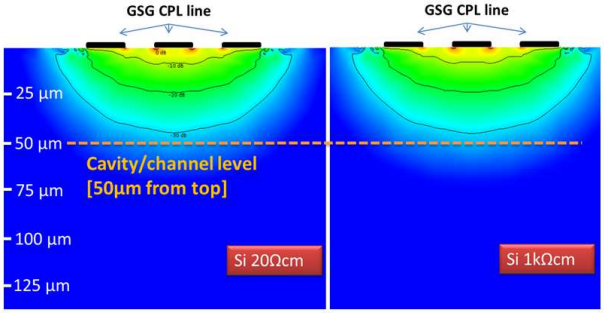


Fig. 3. The depth of EM field penetration into the substrate for 20/15/20µm CPL geometry @10GHz for low (20Ωcm) and high (1kΩcm) resistivity of the silicon substrate.

Another set of simulations performed (Fig. 3) revealed that the depth of EM field penetration saturates. For both: high and low resistivity substrates the penetration depth does not exceed 50µm. The research on signal integrity focused on coplanar line structures (Fig. 4) with respect on neighboring configurations inside the substrate. The CPL is a solution chosen for planar transmission of the signals up to 10GHz. The basic transmission structure has been developed and optimized.

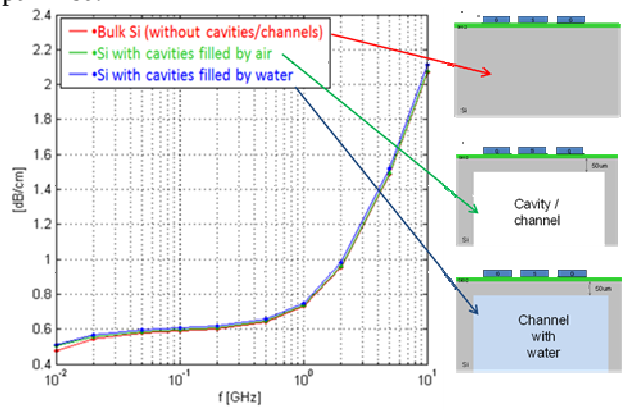


Fig. 4. Simulation results of losses [dB/cm] for various frequencies up to 10GHz for all three neighborhood variants for high resistivity Si substrate (1kΩcm). Three neighborhood variants: no channel (bulk Si), with channel cavities filled with air or filled with water.

Two geometries have been selected for the test vehicle development: 20/15/20 – the narrow one, with the copper strips 20µm wide, with 15µm spacing and 40/30/40 - the wide one, with copper strips 40µm wide with 30µm spacing.

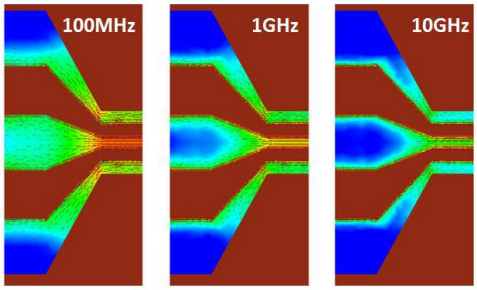
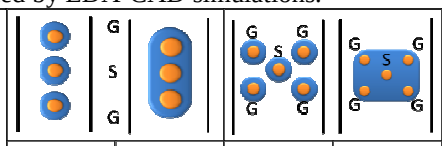


Fig. 5. Analysis of surface current [dB*A/m] flow for 0.1/1/10GHz signal frequency for transition patch from wide GSG line to the narrow one. Strong skin effect for GHz range signals

Such a configuration emerged from TSV geometry simulation and technology features and parameters supported by the FhG IZM-ASSID [9] technology developed, made available for project partners. Several design issues had to be resolved during the coplanar line development in transition area between wide and narrow geometry configurations. Current density for various frequencies has been optimized by CPL transition area geometry using lowest losses optimization criteria (Fig. 5). The set of detailed CPL simulations has been concluded and specific technology guidelines for CarrICool interposer design have been formulated like one that the cooling channel (Fig. 4) should be formed at least 50µm below the CPL deposition level to make neglectable the negative influence of proximity of the channel filled with cooling water. As the signal propagates not only through CPL but also within vertical transition areas (such as TSV) all

interlayer transmission media interconnects have to meet 50Ω impedance matching conditions fixed (standard for measurement equipment). Various configurations have been examined by EDA-CAD simulations.



	TSV on separate Si islands	TSV on common Si islands	TSV on separate Si islands	TSV on common Si islands
Air	0.5-0.6	2	0.8	1.9
Water	>10	2.5-4	>10	2

Fig. 6. Average losses values at 50GHz [dB/cm] for various TSV configurations in CarrICool interposer cooling channel proximity for internal RDL transition area formed by TSV configurations on separate and common islands.

Average loss values for signals up to 50GHz [dB/cm] have been evaluated and generalized (Fig. 6) for various TSV formation configurations: TSVs on common and on separate islands (or within pillars), surrounded by air or surrounded water; for high resistivity (1kΩcm) silicon substrates and for various shielding configurations (GSG and GGSGG).

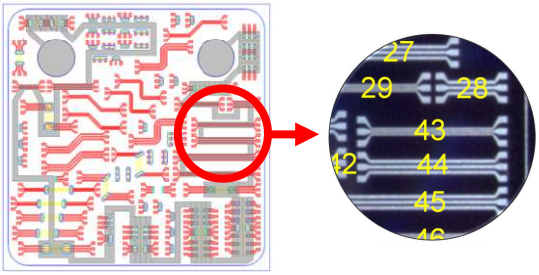


Fig. 7. Test chip layout by ITE for FhG technology (left), with several test structures intentionally with and without TSVs, channels etc., for SI investigations and especially for investigation influence of presents of water for signal transmissions performance. Sample structures enumeration for Fig. 9.

For validation of the interposer technology, design, rules and interposer components profiting from the project practice a set of dedicated test structures has been successfully developed. The CarrICool test chip has been fabricated in FhG IZM-ASSID technology and it combines several test vehicles developed by project partners and embarrasses broad range of interposer reliability, performance, power supply and cooling design issues. In case of the ITE contribution, the test vehicle by ITE integrates over 70 various CPL test structures with optionally with TSV, with channels, contact pads. It has been designed to validate majority of known signal integrity design issues and vulnerabilities with respect for design for testability requirement.

3 THE EXPERIMENT

The CarrICool test chip was fabricated by FhG IZM-ASSID in 2016. The set of technology run versions was selected with care on validation requirements. The 2016' test chips by FhG IZM-ASSID (Fig. 7) used low resistivity substrates, whereas ITE fabricated in parallel similar chips using low (5-7Ωcm) and high (>2kΩcm) resistivity substrates on its own technology, using the internal microfabrication facility in ITE (Fig. 8). Test chips by FhG using high resistivity substrates (1kΩcm) are under production now (III 2017).

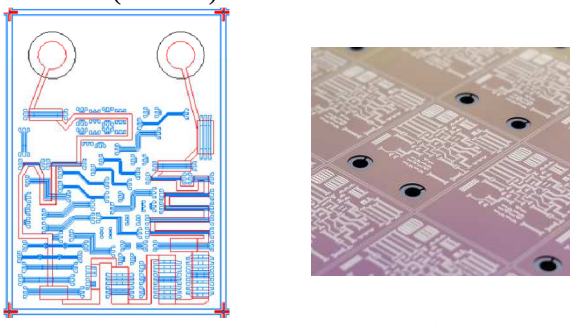
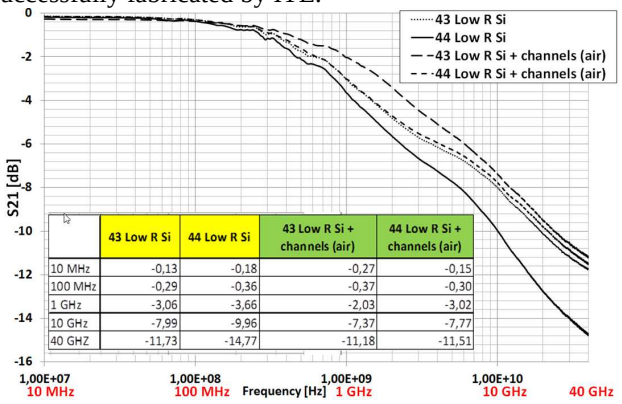


Fig. 8. Test chip layouts by ITE – design layout (left) and the real chip (right.

The FhG 2016 chips cover variety technology aspects of 3D interposer integration apart the signal integrity issues where high resistivity substrates are a must. Therefore backup solution chips by ITE are on high resistivity wafers, however TSV interconnects are not implemented in chip by ITE due to technology constrains. All other interposer issues related to signaling and cooling like channels, liquid ports, coplanar lines, contact pads have been addressed and successfully fabricated by ITE.



	43 Low R Si	44 Low R Si	43 Low R Si + channels (air)	44 Low R Si + channels (air)
10 MHz	-0,13	-0,18	-0,27	-0,15
100 MHz	-0,29	-0,36	-0,37	-0,30
1 GHz	-3,06	-3,66	-2,03	-3,02
10 GHz	-7,99	-9,96	-7,37	-7,77
40 GHZ	-11,73	-14,77	-11,18	-11,51

Fig. 9. Sample planar CPL structure S21 measurement results for no-channel and air-filled channels for two variants of the CPL configuration: 20/15/20 (narrow CPL structure #43) and 40/30/40 (wide CPL structure #44).

The CPL measurements successfully validated simulation results. Narrow CPLs on low resistivity substrates characterize with lower losses than wide CPLs (Fig. 9). Empty channel neighborhood (the channel is filled by air) below the CPL improves its performance (e.g. for #44 14.7[dB] vs. 11.5[dB]). For high resistivity Si substrates an opposite behavior is expected: presence of air-filled channels below the CPL worsens the CPL performance by increased losses. Several S-matrix simulations have been performed for high and low resistivity substrates along with real measurements of test structures developed using ITE design for FhG IZM-ASSID technology on low resistivity

substrates. The S21 measurement results have been achieved for various setups.

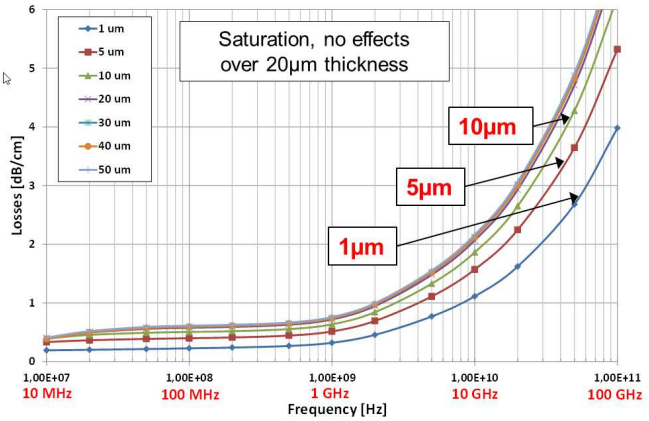


Fig. 10. Simulation results for various channel depths (membrane thicknesses) for air filled channels for high resistivity Si substrate (1kΩcm).

Water influence has been estimated and predicted on simulation basis only yet and achieved results confirm that water proximity worsens losses which become noticeable if channel membrane it thinner than 10um (Fig. 10Fig. 11).

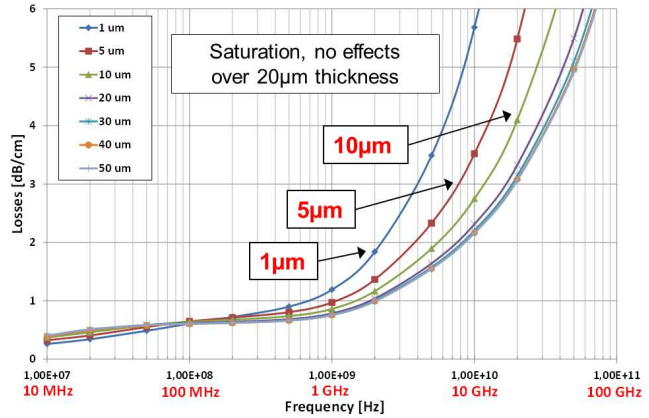


Fig. 11. Simulation results for various channel depths (membrane thicknesses) for water filled channels for high resistivity Si substrate (1kΩcm).

4 CONCLUSIONS

The GHz scale the signal integrity plays very important and critical role. The first major conclusion is that in case of SI the silicon resistivity is most critical due to losses level which are dependent on the geometry of transmission structure but sensitive for presence of water/air which affect achieved performance in opposite styles. High-resistivity substrates lower the coplanar interconnect losses. The spectacular difference is visible between standard, typical, low (few Ωcm) and high (>1kΩcm) resistivity Si wafers. Above 1kΩcm the performance improvement is still observable but not significant. Hence further resistivity increase over 1kΩ may not be financially reasonable. Influence of presence of water is not critical where the water or other fluidic is more than 50µm distant from transmission lines. Signal transmission trough TSV is sensitive for water presence or air proximity. Measurements and more detailed analysis are ongoing and will be continued for high resistivity substrates after fabrication by FhG IZM-ASSID as well as by ITE.

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