Quartz MEMS Oscillators for High-Performance Navigation and Wireless Communications Systems

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ABSTRACT

Quartz MEMS resonators are attractive for use in oscillators for stable frequency control applications in navigation and wireless communication systems by virtue of their reduced cost, size, weight, and power (CSWaP), combined with the potential for integration with electronics. Low phase noise oscillators enable rapid GPS signal acquisition and efficient use of wireless communication frequency spectrum. We present a UHF fundamental-mode oscillator based on a miniature thickness shear mode piezoelectric quartz resonating element fabricated via wafer scale MEMS fabrication. This stable low phase noise oscillator was used to acquire and track the GPS signal in a commercial avionics system, the first demonstration of its kind for MEMS oscillators. An oscillator sustaining ASIC capable of operating in tandem with the quartz MEMS resonator is also described.

Keywords: quartz, MEMS, resonator, oscillator

1 BACKGROUND/STATE OF THE ART

High performance UHF oscillators in most navigation and communication systems are typically fabricated using HF or VHF resonators with frequency multiplying sustaining circuits. Consequently, they operate with high power consumption (usually >100 mW) and have sizable volume (usually >100 mm^3) [1] because of use of larger, low-frequency crystals. Quartz MEMS resonator technology has been developed at HRL Laboratories for UHF oscillators with reduced CSWaP. The MEMS fabrication process enables mass production of UHF resonators on a single wafer. The resonators can then be integrated with their sustaining electronics by either direct wafer bonding or hybrid packaging.

In general, SiGe integrated sustaining circuits have the potential for low 1/f noise, low power consumption, and compact size while maintaining high gain. In addition, advanced quartz packaging technology will enable the future mounting of quartz resonators directly on to a silicon IC [1]. Typical SiGe processes are BiCMOS, with the CMOS technology being used for current sources, bias circuitry, and other control circuitry. Thus, future designs may also include on-chip circuits for temperature and vibration compensation [2].

A challenge in designing oscillator circuits at UHF is the need for large inductors as part of the resonant circuit and RF chokes. These inductors greatly increase the die size and can be difficult to model. Use of a quartz resonator eliminates the need for an inductor to form the resonator and using a push-pull topology eliminates the need for an RF choke. We have designed and measured the results from two pushpull oscillators both utilizing quartz resonators operating above 700 MHz. To our knowledge, this is the highest frequency quartz oscillator that has utilized a SiGe integrated circuit process for the sustaining circuit.

2 UHF RESONATOR DESIGN AND FABRICATION

UHF quartz resonator thickness shear mode devices are designed using COMSOL finite element analysis (FEA). The UHF fundamental thickness shear mode resonators fabricated at HRL consist of an AT-cut quartz plate with a cut angle of 35º15', and top and bottom side rectangular aluminum electrodes. 3-D FEA simulations are performed to evaluate stress profile, modal energy confinement, frequency and Q-factor stability over temperature and also the motional resistance, capacitance and inductance of the resonator.

In quartz resonator design, it is important to optimize modal energy trapping and to minimize spurious or unwanted modes which can interfere with the fundamental thickness shear more and result in undesirable activity dips. Activity dips are discontinuities in the frequency variation over temperature. The corresponding simulated thermal stability of frequency and Q, shown in Fig.1, indicates a stable UHF AT-cut thickness shear device without any unwanted activity dips.

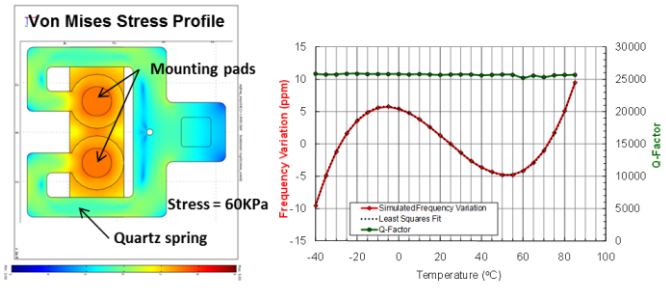

Fig. 1. COMSOL simulated frequency and Q versus temperature of an AT-cut resonator under low mounting stress and without any activity dips.

To achieve fundamental mode resonance in the UHF frequency range, one has to employ wafer-scale micromachining techniques used in MEMS device fabrication. Miniaturization of quartz resonators using key processing enablers such as high aspect-ratio plasma quartz etching and wafer bonding allows the creation of novel piezoelectric structures that are impossible to achieve with the traditional quartz resonator manufacturing process. The wafer-level fabrication process is described in detail in an earlier publication. [1] The starting materials for this process are: 1) a double-side polished AT-cut single crystal quartz wafer, 2) a silicon handle wafer, and 3) a host substrate such as a *GaAs* or a high resistivity silicon wafer. The process begins with a plasma cavity etch into the silicon handle wafer to later accommodate the top metal electrodes of the quartz wafer. The quartz wafer is metallized with electrodes (*Al* or *Au*) and then aligned and directly bonded to the silicon handle wafer using plasma-assisted room temperature bonding in a wafer aligner and bonder. The bonded quartz is subsequently thinned to a thickness of approximately 10 µ*m* using wafer grinding and chemical mechanical polishing techniques. The final target thickness is achieved to less than 5 µ*m* with a combination of argon ion milling and hydrofluoric acid-based wet etching. A deep reactive ion etching (DRIE) with CF_4 chemistry creates the through-wafer vias. Bottom side metallization deposits electrodes matching the previous top side electrode metal (*Al* or *Au*), and also the metal interconnects to bridge the top-side metallization to bottom-side bonding pads. The thin sheet of quartz on the silicon handle is then patterned and etched using a second DRIE step to delineate the resonators. The host substrate is first patterned and etched to form protrusions on its surface, creating a spac-ing underneath the quartz resonator for when it is bonded to the host. *Au* and *In* metals are then deposited on the protrusions to form the bond pads for the subsequent thermal compression bond. In the bonding step, the silicon/quartz pair is aligned to the host substrate using a wafer aligner and then bonded at 100ºC in a wafer bonder using a compression pressure of approximately 10 MPa. Finally, the silicon handle wafer is removed using either an SF_6 plasma etch or a wet TMAH process to release the individual quartz resonators on the host substrate. A completed resonator is shown in comparison with its CAD layout in Fig. 2.

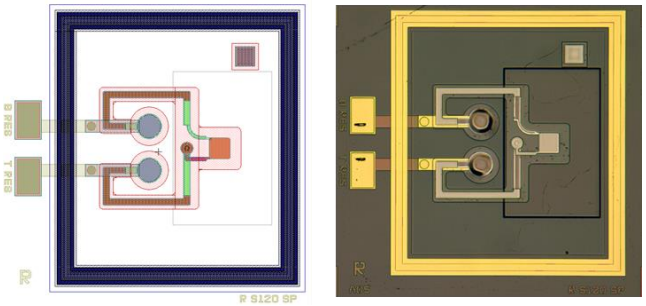

Fig. 2. UHF quartz MEMS resonator design (left) and as fabricated (right).

Fig. 3 illustrates a Van Dyke model representation of a resonator in combinations with an amplifier used to simulate an oscillator. The resonator can be described as a combination of static and motional passive circuit elements. Cs corresponds to the static parasitic capacitance of the resonator. Motional inductance, L1, and motional resistance, R1, correspond to the effective modal mass, m, and damping, the analogous mass-spring system. For the typical linear case, motional capacitance, C1, is analogous to spring stiffness, k. As an example, a 708 MHz quartz resonator, vacuum sealed with a silicon cap, has an unloaded of Q ~ 9.2K and an f*Q product 6.5×10^{12} Hz. It also has a Cs value of 0.699 pF, C1 value of 0.479fF, L1 value of 105 µH and R1 value of 53.442 Ω.

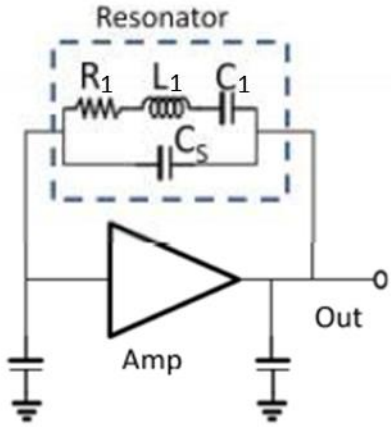

Fig. 3. The Van Dyke circuit model of a quartz resonator in a Pierce Oscillator configuration.

3 HYBRID UHF OSCILLATOR AND SYSTEM INSERTION

We built a hybrid UHF voltage controlled oscillator (VCO) using the quartz MEMS resonator and the printed circuit board technology to perform the initial evaluation of the device. Fig. 4 shows the 663 MHz hybrid oscillator and its phase noise performance measured by an Agilent E5052B signal source analyzer.

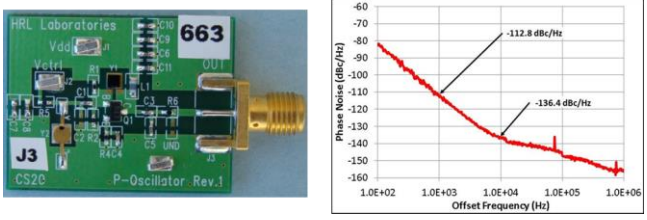

Fig. 4. Photograph and phase noise measurement of the HRL 663 MHz VCO with phase noise of -113 dBc/Hz at 1 kHz offset.

Rockwell Collins, a leading GPS receiver manufacturer, inserted the HRL VCO into its GPS-4000 commercial avionics satellite receiver. The oscillator was able to help lock and track GPS signals, which we believe is

the first demonstration of its kind for MEMS oscillators. Rockwell Collins reported that the HRL effort funded by the DARPA DEFYS program has produced microscale oscillators that are nearly 30 times smaller than what is currently used on GPS receivers. They also consume 320 times less power, and are 30 times more stable under extreme vibration. These oscillators have value beyond GPS systems including precision munitions, ultra small unmanned aerial systems and numerous other applications that require reduced size, weight, power and cost. [3]

4 UHF OSCILLATOR SILICON IC TECHNOLOGY AND CIRCUIT DESIGN

To take full advantage of the small size of the MEMS resonator for UHF oscillator applications, we initiated efforts on the miniaturization of the sustaining circuit electronics – moving from printed circuits to application specific integrated circuits (ASIC). We designed and fabricated through the IBM/GlobalFoundries 7WL 0.18 micron process a SiGe BiCMOS Pierce oscillator sustaining ASIC to be integrated with the resonator.

The IBM/GlobalFoundries 7WL BiCMOS process includes 0.18 μm CMOS for biasing and control circuitry and an HBT process with maximum unity gain frequencies (f_T) of approximately 60 GHz. The key to implementing a push-pull technology is to employ an IC technology that has a well modeled complimentary device that has good RF performance. The IBM 7WL process includes a vertical p-n-p RF device model which is essential to simulate push-pull operation at UHF. Fig. 5 shows a schematic of the push-pull sustaining circuitry and includes the external quartz resonator.

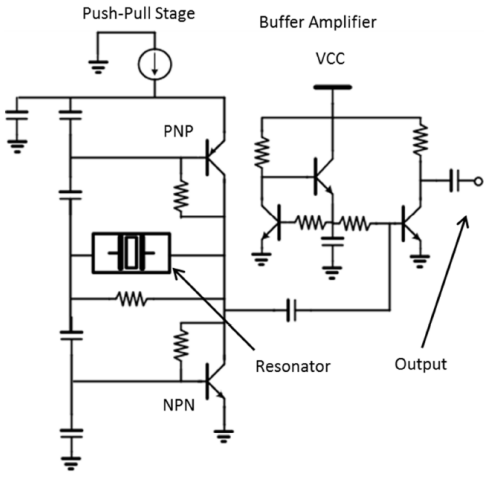

Fig. 5. Schematic of the Push-Pull Pierce oscillator with a buffer amplifier.

The push-pull stage is used to create the oscillation and consists of each transistor (n-p-n and p-n-p) in a Pierce configuration. The n-p-n transistor has a base width of 240nm, an emitter width of 800nm, and an emitter length of 12μm while the vertical p-n-p transistor has base and emitter widths of 800 nm and an emitter length of 10 μm. Capacitors connected from the base and collector to ground (or the emitter for the p-n-p transistor) form the Pierce configuration with the remaining capacitors being used for DC blocking or RF filtering. The buffer amplifier consists of a single stage common emitter amplifier with the device being the same size as the aforementioned n-p-n device. A 184 Ω output bias resistor transforms the output impedance towards 50 Ω and the amplifier adds approximately 10 dB of gain. The remaining two transistors form the current source with the mirror transistor being the same size as the amplifier transistor. The collector voltage, Vcc, is set to 2 V and each leg of the current source draws ~2.3 mA.

Fig. 6 details the current source at the top of Fig. 5 (with one lead attached to ground) biasing the push-pull stage. The device bias conditions were chosen to minimize power consumption while maintaining enough gain to sustain an oscillation. Under these conditions, the f_T of the devices is close to 20 GHz which is sufficient for high gain at UHF. For this design, a "top" current source was selected over a "tail" current source. This current source utilizes the process' 0.18 μm CMOS technology and the theory behind this topology is detailed in [3]. To realize the DC bias, the NMOS devices used for the reference mirror have gate lengths of 400 nm and widths of 10 μm. The PMOS devices directly above the push-pull stage have gate lengths of 400 nm and widths of 20.5 μm and are sized to provide the ~2 mA of current necessary to bias the stage when Vdd is set to 2 V. The associated width to length ratio (W/L) of two leads to a current multiplication of two which is very conservative and selected for ease of design.

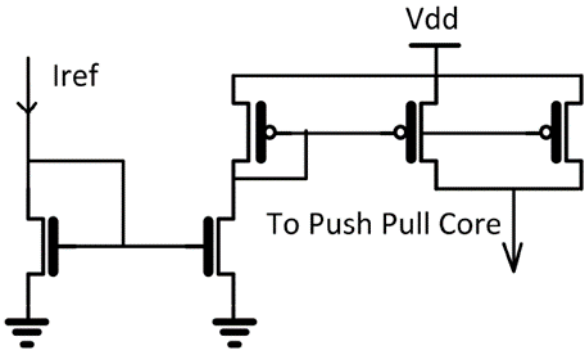

Fig. 6. Schematic of the current source used to bias the push-pull oscillator core.

5 UHF OSCILLATOR WITH SUSTAINING ASIC RESULTS AND FUTURE WORK

The singulated ASIC (Fig. 7) and the packaged MEMS resonator were die attached to a printed circuit board and wire bonded together for ease of testing (Fig. 8). This integrated device has a volume of <2 mm^3 and oscillates at a fundamental mode of 815 MHz with an output power of -9.5 dBm (Fig. 9). This oscillator operates at 1.8 to 2.5 VDC and draws <10 mA for a total power consumption of <25

mW. We tested the phase noise of this oscillator and measured -102 dBc/Hz at 1 kHz offset and noise floor of < -140 dBc/Hz.

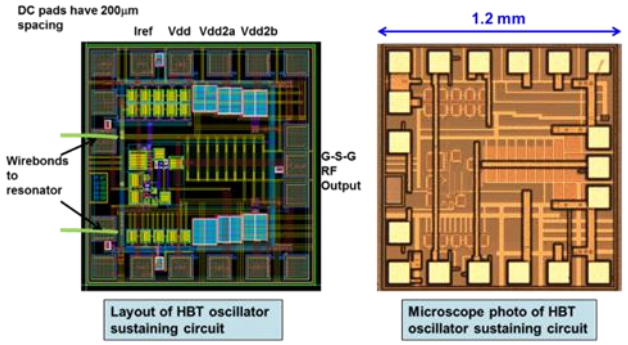

Fig. 7. UHF oscillator sustaining ASIC design (left) and fabricated chip (right).

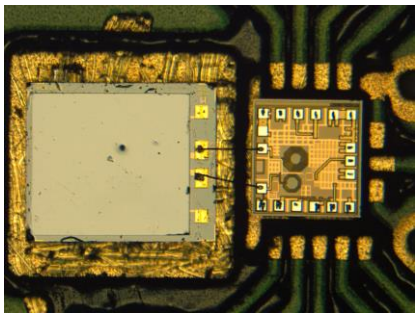

Fig. 8. Integrated UHF oscillator consisted of a vacuum-packaged resonator (left) and a sustaining ASIC (right). The ASIC has a footprint of ~1.4 mm^2 and a chip thickness of < 300 microns.

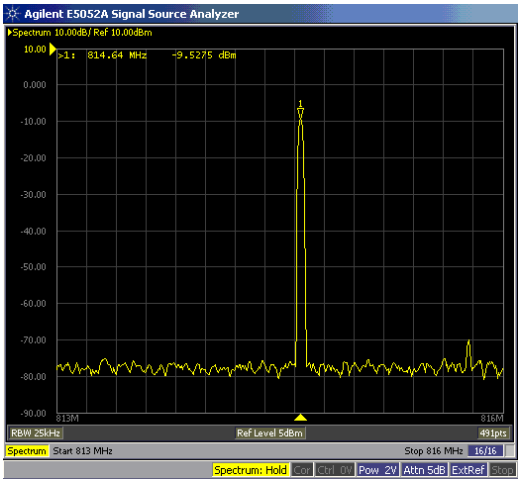

Fig. 9. Oscillation spectrum of the 815 MHz integrated ASIC oscillator.

Phase noise performance of the UHF oscillator based on IC sustaining circuitry is approaching results obtained from hybrid circuitry. Prior quartz oscillators using hybrid technology consume between 30-90 mW of DC power depending the choice of active device. Thus, using established SiGe IC processes leads to lower power consumption in addition to adding the capability for integration of the control circuitry. We anticipate improvement in phase noise as the resonator operating point is more accurately controlled. Future work will focus on developing tunable oscillators (VCXOs) such that the sustaining circuit can be adjusted to operate at an optimal resonator operating point. In addition, adding control circuitry for temperature and vibration compensation will enable higher levels of integration and enhance performance.

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