Characteristic Fluctuation of Gate-All-Around Silicon Nanowire MOSFETs Induced by Random Discrete Dopants from Source/Drain Extensions

Wen-Li Sung[1,2] and Yiming Li[1,2,3,*]

[1] Parallel and Scientific Computing Laboratory, National Chiao Tung University, Hsinchu, Taiwan
[2] Institute of Communications Engineering, National Chiao Tung University, Hsinchu, Taiwan
[3] Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan
Tel: +886-3-5712121 Ext. 52974; Fax: +886-3-5726639; *E-mail: ymli@faculty.nctu.edu.tw

ABSTRACT

In this work, characteristic fluctuation of undoped gate-all-around silicon nanowire MOSFETs induced by random discrete dopants (RDDs) penetrating from the source/drain (S/D) extensions is explored. Compared with the results of RDDs penetrating from the S extension, asymmetric variations of characteristics induced by RDDs penetrating from the D extension are suppressed owing to the different extent of screening effect on the surface of channel; in particular, the fluctuations of voltage gain and cut-off frequency are reduced from 24% and 21% to 7% and 10%, respectively, because of the effective fluctuation reduction of maximum transconductance near the D extension.

Keywords: Gate-all-around, nanowire, MOSFET, random discrete dopants, undoped channel, penetration, source / drain extensions, characteristic fluctuation,.

1 INTRODUCTION

Gate-all-around (GAA) nanowire (NW) MOSFET is a promising device for sub-7-nm technology nodes [1-2]. Many reports of random dopant fluctuation (RDF) focused on DC characteristic variability [3-6]; and various channel doping processes were proposed to suppress characteristic fluctuations induced by random discrete dopants (RDDs) of planar MOSFETs [7]. For production yield improvement and optimization, it is important to consider manufacturing tolerances, model uncertainties, and variations for robust circuit design [8]-[12]. Notably, although the V_{th} variation of WKF and PVE is more significant than that of RDF in DC characteristic fluctuation for GAA Si NW MOSFET [6], the dynamic operation and high-frequency characteristic fluctuation induced by various RDDs sources penetrating from S/D extensions have not been clearly investigated by using a unified simulation methodology. Thus, assessing characteristic fluctuation induced by RDDs penetrating from S/D extensions is important for us to explore sub-7-nm GAA Si NW MOSFETs.

In this work, we study characteristic fluctuation of 7 nm GAA Si NW MOSFETs with undoped channel induced by RDDs penetrating from the source extension and its penetration into channel (denoted as RDs_Sext_pe) and by RDDs from drain side (denoted as RDs_Dext_pe), similarly.

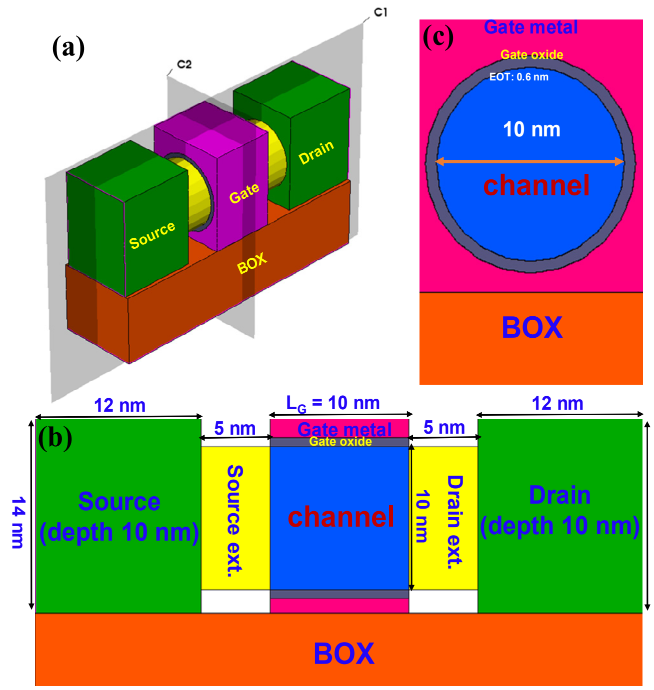

Fig. 1. (a) 3D GAA NW MOSFET structure. (b) Cross-sectional view along C1 cut-plane. (c) Cross-sectional view along C2 cut-plane.

For the 7 nm device, we assume its effective gate length (L_G) is equal to 10 nm, as shwon in Fig. 1, according to the ITRS projection. Characteristic fluctuation of the explored devices induced by different source of RDDs is observed and discussed for the device at 7-nm technology node.

2 COMPUTATIONAL STRUCTURE AND METHODOLOGY

The accuracy of device simulation by solving 3D quantum-mechanically corrected transport model has been validated with the results of non-equilibrium Green's function (NEGF) [6]. Before performing statistical device simulation, our approach has also been calibrated with measured drain current-gate voltage (I_D-V_G) curves of the fabricated devices [6]. Figs. 1(a), (b) and (c) show the 3D plot, transverse and lognitudial cross-sections of simulated structure. The effect of parasitic capacitances resulting from the spacer region is neglected to simplify the calculation.

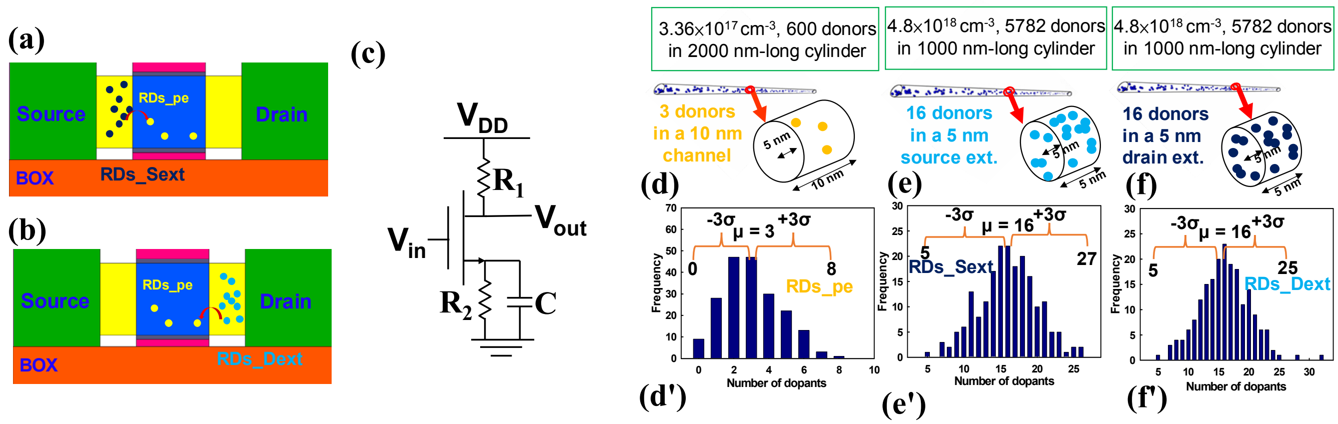

Fig. 2. Device simulation illustration for the fluctuations induced by (a) RDs_Sext_pe and (b) RDs_Dext_pe. (c) The tested common source amplified circuit, where the value of R_1 is $5x10^4$ Ω, R_2 is 10^4 Ω and C is 10^{-6} F, respectively. (d) 2000 nm-long cylinder containing penetrating dopant's concentration with $1.1x10^{19}$ cm^{-3} which is divided into 200 sub-cylinder (10-nm-long channel with various penetrations) and the distribution is shown in (d'). (e) 1000 nm-long cylinder where the equivalent source extension doping concentration is $4.8x10^{18}$ cm^{-3} and is divided into 200 sub-cylinder (5-nm long for the S extension). Its distribution is shown in (e'). (f) Similar to the source extension, we generate statistical patterns for the drain extension. Its distribution is shown in (f').

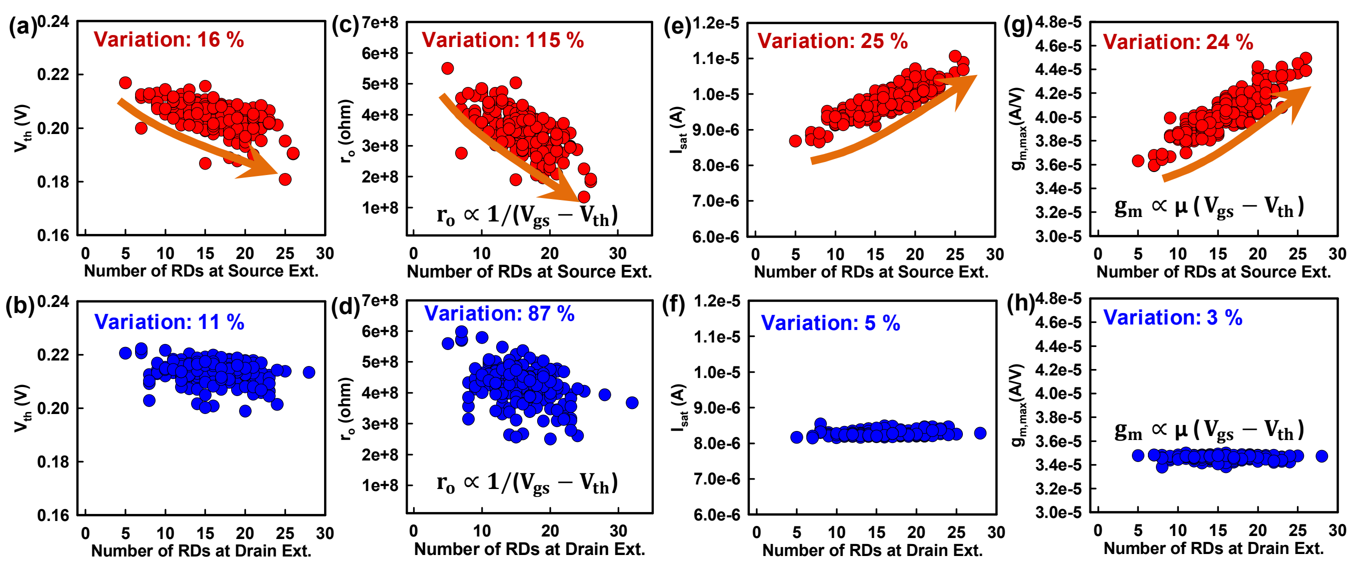

Fig. 3. (a) V_{th} versus the number of RDs at the source extension for RDs_Sext_pe. (b) V_{th} versus the number of RDs at the drain extension for RDs_Dext_pe. (c) r_o versus the number of RDs at the source extension for RDs_Sext_pe. (d) r_o versus the number of RDs at the drain extension for RDs_Dext_pe. (e) I_{sat} versus the number of RDs at the source extension for RDs_Sext_pe. (f) I_{sat} versus the number of RDs at the drain extension for RDs_Dext_pe. (g) $g_{m,max}$ versus the number of RDs at the source extension for RDs_Sext_pe. (h) $g_{m,max}$ versus the number of RDs at the drain extension for RDs_Dext_pe.

The simulated structure consists of amorphous-based titanium nitride, hafnium dioxide gate stack, and 0.6 nm effective oxide thickness and work-function of 4.483 eV. The device is with undoped channel and all RDDs inside the channel are penetrating from S/D extensions including RDDs induced by S/D extensions. The magnitude of V_{th} is extracted by using constant current method.

Figs. 2(a) and (b) illustrate the simulated devices with RDs_Sext_pe and RDs_Dext_pe, respectively. Fig. 2(c) is the tested common-source circuit with sinusoid input wave (offset is equal to 0.5 V) [7]. The equivalent channel resulting from the penetration from S/D extensions and the S/D extensions doping concentration of long cylinder are equal to $5x10^{17}$ and $4.8x10^{18}$ cm^{-3}, respectively. As shown in Figs. 2(d), (e), and (f), they are statistically generated (i.e., totally random) and partitioned into 200 sub-cylinders with 10 and 5 nm, respectively. Fig. 2(d) shows the RDs penetration from the source/drain extensions (denoted as RDs_pe) with an equivalent doping concentration of $1.1x10^{19}$ cm^{-3}, and its distribution shows in Fig. 2(d'). Fig. 2(e) shows the RDDs source extension (denoted as RDs_Sext) with an equivalent doping concentration of

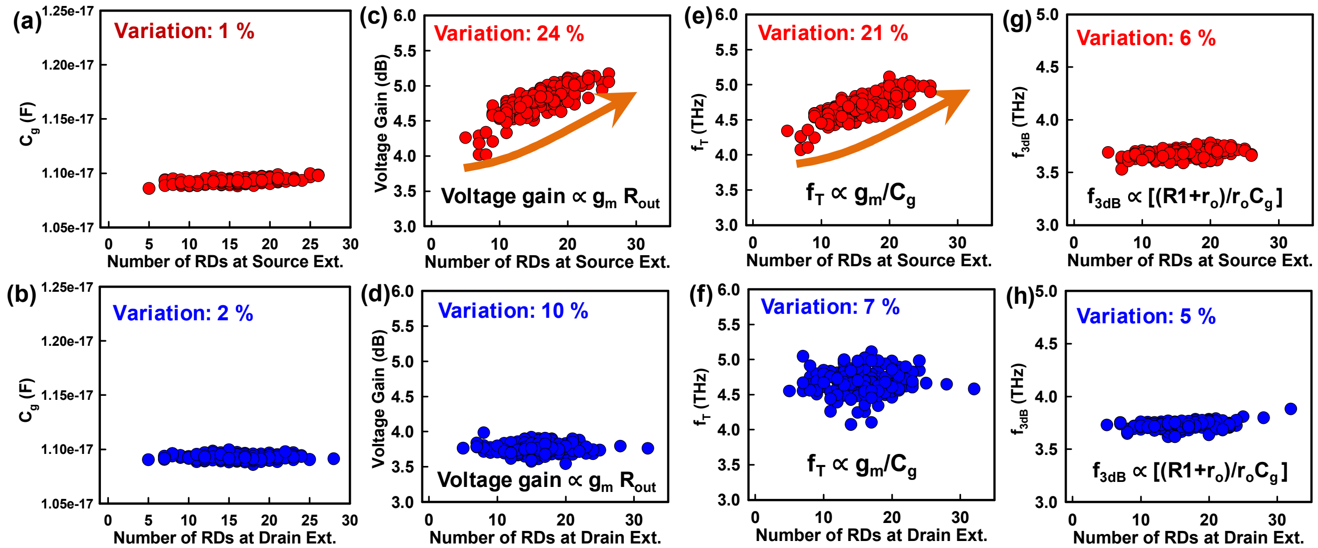

Fig. 4. (a) C_g versus the number of RDs at the source extension for RDs_Sext_pe. (b) C_g versus the number of RDs at the drain extension for RDs_Dext_pe. (c) Voltage gain versus the number of RDs at the source extension for RDs_Sext_pe. (d) Voltage gain versus the number of RDs at the drain extension for RDs_Dext_pe. (e) f_T versus the number of RDs at the source extension for RDs_Sext_pe. (f) f_T versus the number of RDs at the drain extension for RDs_Dext_pe. (g) f_{3dB} versus the number of RDs at the source extension for RDs_Sext_pe. (h) f_{3dB} versus the number of RDs at the drain extension for RDs_Dext_pe.

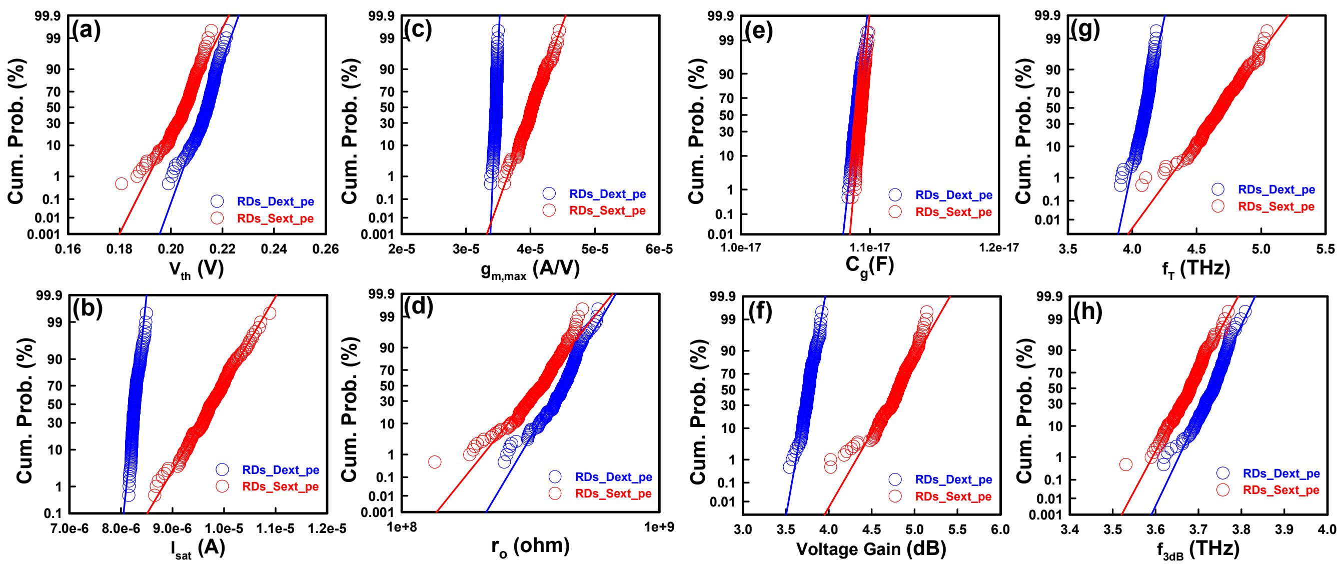

Fig. 5. The cumulative probability of (a) V_{th}, (b) I_{sat}, (c) $g_{m,max}$, (d) I_{off}, (e) C_g, (f) Voltage gain, (g) f_T, and (h) f_{3dB} for RDs_Sext_pe and RDs_Dext_pe.

$4.8x10^{18}$ cm^{-3}, and its distribution shows in Fig. 2(e'). Fig. 2(f) shows the RDs drain extension (denoted as RDs_Dext) with an equivalent doping concentration of $4.8x10^{18}$ cm^{-3}, and its distribution shows in Fig. 2(f'). Notably, instead of traditional circuit simulation with compact model, device-and-circuit coupled simulation approach is performed for the 7-nm GAA Si NW MOSFET CS amplifier. The nodal equations of the tested circuit of Fig. 2(c) are formulated and then directly coupled to the device transport equations, which are solved simultaneously to obtain the circuit AC and high-frequency characteristics. The device terminal characteristics obtained by device simulation are input in the circuit simulation through circuit nodal equations. The effect of RDDs resulting from the penetration of S/D extensions inside the channel and the S/D extensions themselves on the tested circuit behaviors is thus properly estimated from device physics point of view.

3 RESULTS AND DISCUSSION

Fig. 3 compares the variations of threshold voltage (V_{th}), output resistance of transitor (r_o), on-state current (I_{sat}), and the maximum transconductance ($g_{m,max}$) induced by different two sources of RDDs: RDs_Sext_pe and RDs_Dext_pe, respectively. For the case of RDs_Sext_pe, as the number of RDs at source extension increases, the trend of V_{th}, r_o decrease and I_{sat}, $g_{m,max}$ increases, as shown in Figs. 3(a), (c), (e) and (g), respectively. However, for the case of RDs_Dext_pe, as shown in Figs. 3(b), (d), (f), and (h), their trends are insignificant. It could be attributed to the different extent of screening effect on the channel surface. The variation of gate capacitance (C_g) is small due to overall control gate, as shown in Fig. 4(a) and (b). The variations of voltage gain and cut-off frequency (f_T) induced by RDs_Dext_pe is smaller than that of RDs_Sext_pe, as shown in Figs. 4(c) and (e). The dependencies of voltage gain and f_T on the number of RDDs from source extension are clear; however, the variations of voltage gain (10%) and f_T (7%) are small for the case of RDs_Dext_pe, as shown in Fig. 4(d) and (f).

As shown in Fig. 5, we further estimate the cumulative probabilities of V_{th}, r_o, I_{sat}, $g_{m,max}$, C_g, voltage gain, f_T, and f_{3dB} for RDs_Dext_pe and RDs_Sext_pe, respectively. The findings of our study show that the slope of $g_{m,max}$ and I_{sat} for RDs_Dext_pe is smaller than that of RDs_Sext_pe. It indicates that the distribution of $g_{m,max}$ and I_{sat} can be improved by RDs_Dext_pe. For the variation of C_g, there are no significant differences between the cases of source extension and drain extension due to optimal electrostatic control. Thus, the variation of C_g will not be a dominated factor for the variation of f_T and voltage gain which is different from our earlier work [7] that the variation of C_g dominates the fluctuation of high-frequency parameters for planar MOSFETs. The variations of voltage gain, f_T can be effectively suppressed because the variation of $g_{m,max}$ is reduced dramatically by RDs_Dext_pe.

4 CONCLUSIONS

In summary, characteristic fluctuation of GAA Si NW MOSFETs induced by RDs_Dext_pe and RDs_Sext_pe has been estimated for 7-nm technology node. Different characteristic fluctuation induced by S/D extensions and its penetration were observed and explored, where RDDs resulting from the source extension largely complicate variability. The engineering findings of this study indictae asymmetric variability which can be applied to design robust devices and benefit fabrication.

ACKNOWLEDGEMENTS

This work was supported in part by Ministry of Science and Technology of Taiwan under Contracts No. MOST-105-2221-E-009-132 and MOST-105-2218-E-009-019, and by tsmc 2016-2017 grant, Hsinchu, Taiwan.

REFERENCES

[1] N. Mori, G. Mil'nikov, H. Minari, Y. Kamakura, T. Zushi, T. Watanabe, M. Uematsu, K. M. Itoh, S. Uno, and H. Tsuchiya, "Nano-device simulation from an atomistic view," in IEDM, Washington, DC, p. 116, Dec. 2013.

[2] M. Uematsu1, K. M. Itoh, G. Mil'nikov, H. Minari, and N. Mori, "Simulation of the effect of arsenic discrete distribution on device characteristics in silicon nanowire transistors," in IEDM, San Francisco, CA, p. 709, Dec. 2012.

[3] H.-T. Chang and Y. Li, "Random Dopant Fluctuation in 10-nm-Gate Multi-Channel Gate-All-Around Nanowire Field Effect Transistors," NSTI Nanotech. Conf., Washington, DC, vol. 3, p. 5, June 2014.

[4] K. Nayak, S. Agarwal, M. Bajaj, K. V. R. M. Murali, and V. R. Rao, "Random Dopant Fluctuation Induced Variability in Undoped Channel Si Gate All Around Nanowire n-MOSFET," IEEE Trans. Electron Devices, vol. 62, no. 2, p. 685, Feb. 2015.

[5] A. Majumdar, S. Bangsaruntip, G. M. Cohen, L. M. Gignac, M. Guillorn, M. M. Frank, J. W. Sleight, and D. A. Antoniadis, "Room-temperature carrier transport in high-performance short-channel Silicon nanowire MOSFETs," in IEDM, San Francisco, p. 179, Dec. 2012.

[6] Y. Li, H.-T. Chang, C.-N. Lai, P.-J. Chao, and C.-Y. Chen, "Process Variation Effect, Metal-Gate Work-Function Fluctuation and Random Dopant Fluctuation of 10-nm Gate-All-Around Silicon Nanowire MOSFET Devices," in IEDM, Washington, DC, p. 887, Dec. 7-9, 2015.

[7] Y. Li and C.-H. Hwang, "High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants," IEEE Trans. Microw. Theory Tech., vol. 56, no. 12, p. 2726, Dec. 2008.

[8] J. W. Bandler, R. M. Biemacki, Q. Cai, S. H. Chen, S. Ye, and Q. J. Zhang, "Integrated physics-oriented statistical modeling, simulation fluctuations and optimization," IEEE Trans. Microw. Theory Tech., vol. 40, no. 7, p. 1374, Jul. 1992.

[9] D. E. Stoneking, G. L. Bilbro, P. A. Gilmore, R. J. Trew, and C. T. Kelley, "Yield optimization using a GaAs process simulator coupled to a physical model," IEEE Trans. Microw. Theory Tech., vol. 40, no. 7, p. 1353, Jul. 1992.

[10] A. H. Zaabab, Q.-J. Zhang, and M. Nakhla, "A neural network modeling approach to circuit optimization and statistical design," IEEE Trans. Microw. Theory Tech., vol. 43, no. 6, p. 1349, Jun. 1995.

[11] J. Purviance and M. Meehan, "CAD for statistical analysis and design of microwave circuits," Int. J. Microw. Millimeter-Wave Comput. Aided Eng., vol. I, no. 1, p. 59, Jan. 1991.

[12] Q. Li, J. Zhang, Li Wei, J. S. Yuan, Y. Chen, and A. S. Oates, "RF circuit performance degradation due to soft breakdown and hot-carrier effect in deep-submicrometer CMOS technology," IEEE Trans. Microw. Theory Tech., vol. 49, no. 9, p. 1546, Sep. 2001.