A Hybrid Process Design Kit: Towards Integrating CMOS and III-V Devices

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Abstract

A hybrid process design kit (PDK) for novel integrated circuits incorporating high performance compound semiconductor (CS) materials and devices into existing production Si-CMOS compatible foundry process is presented. The hybrid PDK permits direct integration of Au-free III-V devices into CMOS circuits on a common Si-CMOS platform for high performance analog/RF, mixed-signal, digital or optoelectronic interconnect designs. It facilitates electrical information sharing between CMOS and III-V devices on a schematic design with foundry-proven back-end multi-layer metal interconnects in a single chip fabrication. It provides a new path in fabricating integrated CMOS and III-V devices with commonly used CMOS libraries and III-V parameterized cell libraries within shorter design circle times for high-frequency, high-voltage, and high-power applications.

Keywords: Process design kit (PDK), compact model, parameterized cell (PCell), standard cells, CMOS, III-V, design rule check (DRC), layout versus schematic (LVS).

1. INTRODUCTION

Process Design Kit (PDK) is a comprehensive set of foundry-verified data files and device–layout–technology information. It provides schematic symbols, parameterized database, and model cards for circuit simulations, a parasitic extraction deck for post-layout simulations, a set of design-rule check (DRC) and layout-versus-schematic (LVS) verification deck for design verification. A PDK package consists of parameterized cell (PCell) and pad libraries, a set of device verification rule files and associated initialization scripts and characterization files to enable a design with EDA toolset to generate a set of tape-out files for device fabrication. PDK becomes a crucial link to bridge the connection between IC design and fabrication process within shorter design cycle times.

Nowadays, in the microelectronics industry, silicon complementary metal-oxide-semiconductor transistors (Si-CMOS) are still the dominant components in the foundry proven technology nodes. The main-stream in analog/RF and mixed-signal/digital designs is still driven by Si-CMOS PDK [1]. Besides addressing the downscaling of CMOS technologies to meet the requirements on speed, packing circuit density, and power consumption, CMOS designs face challenges in device matching characteristics as a result of scanning device images from the reticle, no longer having a one-to-one correspondence with the layout due to lithographic quantum limits. Furthermore, high leakage currents resulting from lower thresholds and thinner gate oxide in the CMOS process, and its limitations for high-frequency, high-voltage, and high-power applications, force design alternatives in CS materials to meet the demands and requirements. However, in order to achieve cost-effective fabrication with silicon-based substrate in CMOS foundry-proven process within shorter design cycle times together with high-performance III-V devices, the solutions may not be as simple as to bond multiple modules together by flip-chip packaged [2], [3] or die-wafer bonded [4] in opto-electronic interconnect, which may introduce unforeseen parasitic and increase the delay in the actual fabricated circuits. A more attractive approach is the direct integration of CMOS and III-V devices on a common silicon-substrate. To facilitate this approach, the incorporation of CS materials process data into a Si-CMOS PDK to fabricate III-V and CMOS devices on a common platform becomes a necessity.

In this paper, we present the development of a hybrid CMOS/III-V PDK using III-V low-temperature Au-free contact metallurgy [5] under the Singapore-MIT Alliance Research and Technology Low Energy Electronic Systems (SMART-LEES) program. The challenges in merging GaN HEMTs, GaN LEDs, InGaP LEDs, and InGaAs HEMTs process data into an existing Si-CMOS foundry PDK to fabricate the devices on the same Si-substrate are addressed in the following sections. The developed hybrid PDK has been implemented in EDA toolset, which designers are already familiar with. Designers will not need to differentiate between CMOS and hybrid CMOS/III-V PDKs in performing pre/post-layout simulations, design-rule checks, and even generating GDS-II files for tape-out submission. However, designers will have access to the same properties in their designs as those III-V devices in large-signal RF and high-speed analog/mixed-signal

designs on a cost-saving production-proven Si-CMOS compatible foundry process.

2. The Merger Between Compound And Si-CMOS Semiconductor Materials

Double-layer bond-and-transfer (DL-BaT) process has been demonstrated successfully to bond both CS materials and Si-CMOS on a common SOI substrate [6]. The same procedure has been carried out to bond Si-CMOS layer, in which CMOS devices have been fabricated, as shown in Fig. 1(a), on either III-V HEMT or photonic layers [7], as shown in Fig. 1(b), into a single engineered substrate. The engineered substrate contains both the Si-CMOS layer and the CS material layers in which III-V devices can be formed [8].

The developed hybrid PDK offers GaN HEMTs, GaN LEDs, InGaP LEDs, and InGaAs HEMTs to designers. Each of these devices requires different type of CS materials to bond with CMOS layers before forming the chosen III-V device on an engineered substrate. In order to facilitate designers to correctly choose the appropriate bonding materials for their designs, designers are provided with a flag in the PDK to select the correct type of CS materials to be used in the DL-BaT process. This flag also provides the information of the correct set of design rules to be performed on their design for any process violations and device matching between the layout and the schematic.

With the DL-BaT process approach, and the implementation of a flag in the hybrid PDK, these ensure a correct type of CS materials to be bonded with a CMOS layer to form a chosen III-V device with the correct verification rules to be performed on a hybrid design.

3. The Merger Between III-V and CMOS Devices into a Hybrid PDK

A PDK package is the collection of foundry-specific data and script files using EDA tools as a platform for chip designs and fabrication. It provides a complete set of PDK libraries with symbols for schematic designs, component models for circuit simulations, and layout information with process-specific parameters for tape-out and fabrication.

An existing Si-CMOS PDK provides a set of CMOS PCells and a complete multi-layer interconnect scheme to connect devices on a CMOS design. The design can be fabricated on a Si-substrate wafer. Figs. 3(a) and 3(b) show, respectively, two separate hybrid designs using GaN and InGaAs/InP CS materials as the substrate. Symbols for CMOS and III-V devices can be selected from PCell libraries in the developed hybrid PDK.

Layer and technology information of CMOS and III-V processes is available in the hybrid PDK. This information provides a complete set of GDS layer numbers, which are referenced to photolithography masks used in CMOS and III-V lithography processes.

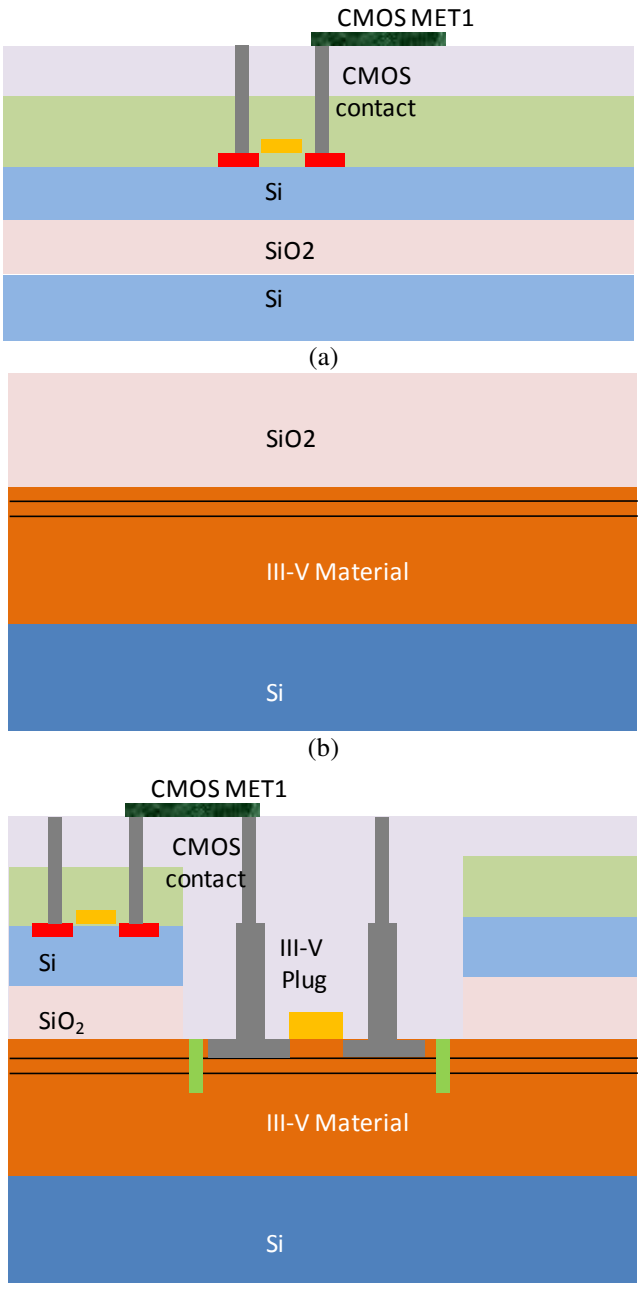


Figure 1: Cross sectional views of (a) CMOS with CMOS back-end metal, (b) III-V CS material layers, and (c) CMOS/III-V devices on Si-substrate with CMOS back-end interconnects.

With these GDS layers, it allows designers to view and create CMOS and III-V devices on the same layout. Each of the lithography process steps uses drawn or/and generated layers to complete a lithography process. It is important that the developed hybrid PDK captures the entire set of lithography processes with the set of GDS layers stored in the technology files.

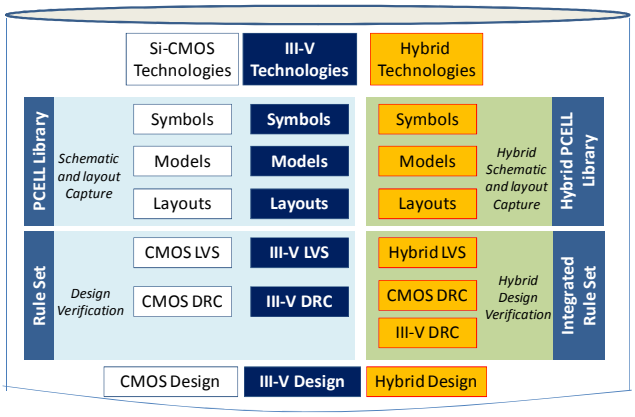
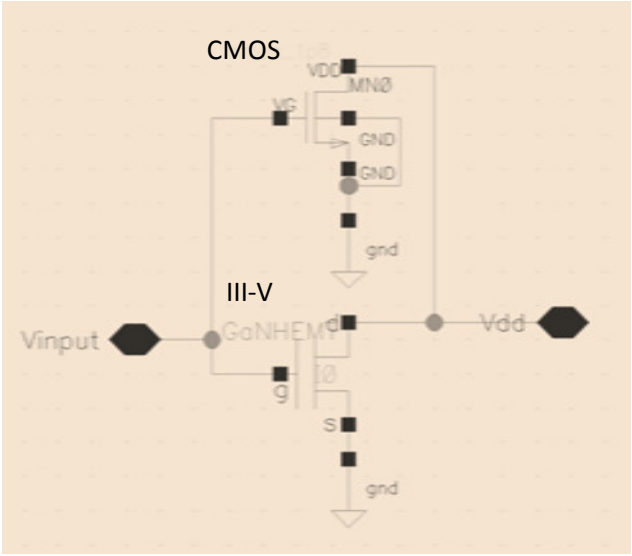


Figure 2: Hybrid CMOS/III-V PDK, a merger between Si-CMOS and III-V technologies.

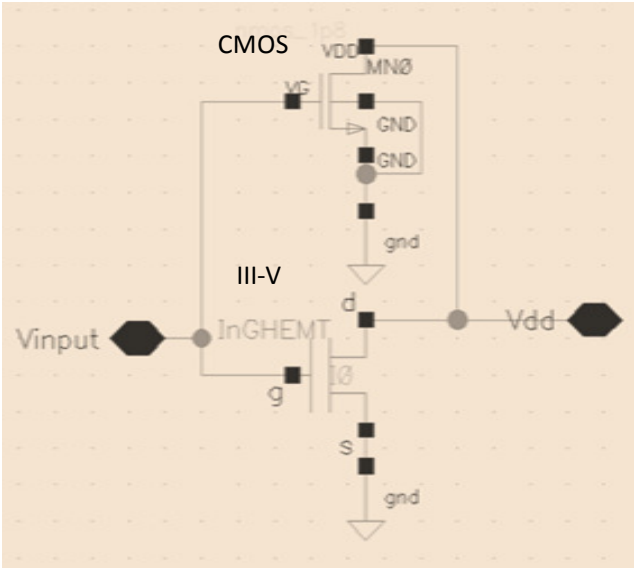
A hybrid schematic is provided with a wire tool to connect CMOS and III-V device symbols together for circuit simulations. A hybrid layout is provided with multi-layer metal interconnects to make the connections between devices. The developed hybrid PDK has chosen foundry-proven CMOS metallization processes to establish physical connectivity between devices, as shown in Fig. 1(c). It provides a common metallization platform, which is the most efficient interconnection scheme and, importantly, it reduces the risk in back-end fabrication processes for a hybrid design. The developed hybrid PDK provides a set of III-V connectivity rules to verify the electrical connection between CMOS and III-V devices. It can also perform the standard CMOS back-end interconnects verification on a hybrid design.

Design verification in design and fabrication flow plays a very important role to match a translated layout to a schematic design (using LVS). It performs design checks on possible process violations, which can be detected with a set of design rules (using DRC) on the layout. It also provides a consistency check on the devices drawn on a layout against the symbols used in a schematic. The developed hybrid PDK has integrated III-V device information in DRC and LVS rules set to perform hybrid design verification. This verification is very important when a hybrid layout is used to generate a set of GDS layer information, which is one of the tape-out requirements for device fabrication.

A hybrid design uses CMOS process to fabricate CMOS devices and III-V process for III-V devices. Thus, the hybrid PDK provides two sets of DRC rules to check on a hybrid design for any layout design-rule violations. It can use one set of standard CMOS DRC rules and another set of III-V DRC rules to perform DRC checks separately on a hybrid design. The information that the CMOS DRC checks can provide includes the CMOS device fabrication process and its back-end metallization process violations. The checks include physical back-end CMOS metal layers and CMOS contact on III-V devices. III-V DRC checks can only provide the information of any III-V device fabrication process violations. This is sufficient for a complete DRC to check on a hybrid design for any design violations on both technologies.



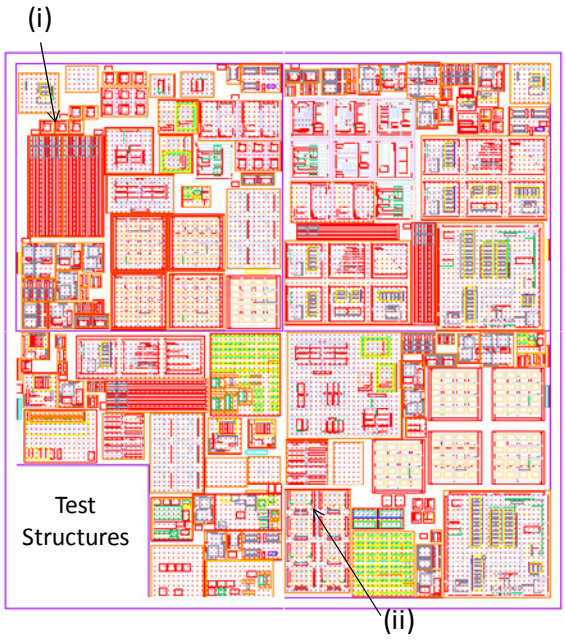
(a)



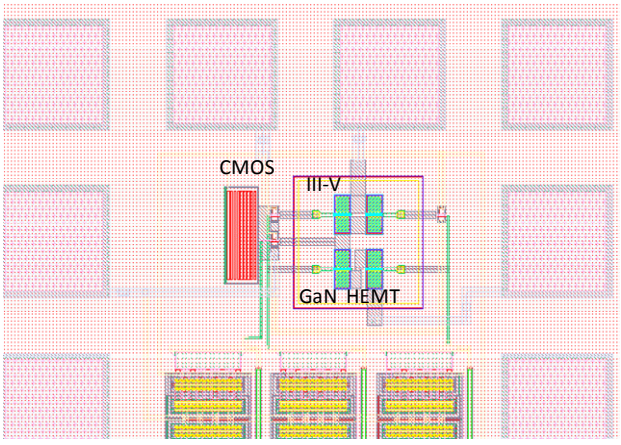
(b)

Figure 3: The schematic diagrams of (a) CMOS + GaN HEMT and (b) CMOS + InGaAs HEMT circuits on different CS materials with the same hybrid CMOS/III-V PDK.

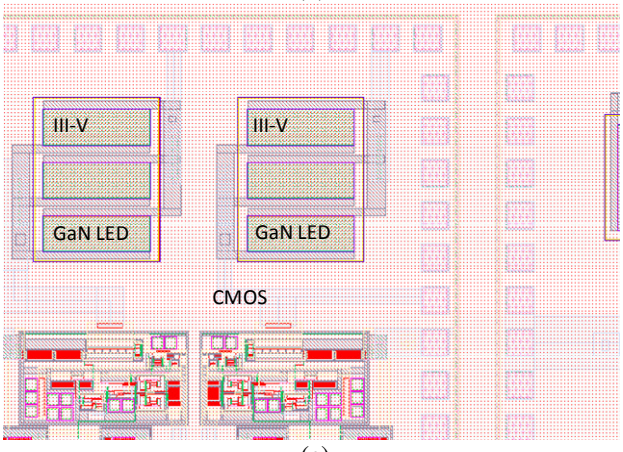
Furthermore, the hybrid PDK presented here uses the existing CMOS library without modification. This allows designers to reuse their pre-designed CMOS circuit libraries. Hybrid designs become simpler with minor modifications to replace a few key components in the existing CMOS designs with III-V devices to boost up the overall design performance in a single chip.



(a)



(b)



(c)

Figure 4: A cost-saving approach to facilitate integrated designs from various teams on (a) a multi-project chip, (b) the integrated CMOS-HEMT circuit at location (i), and (c) the integrated CMOS-LED circuit at location (ii) on the same multi-project chip.

4. Hybrid Design with Hybrid PDK

The hybrid PDK presented here allows designers to choose from a variety of III-V HEMT and LED devices to integrate with CMOS. The current iteration of our integration process flow only allows a single III-V device platform to be integrated with CMOS. Thus, the CMOS + GaN HEMT platform, as shown in Fig. 3(a), can allow circuits that comprise only GaN HEMT (on GaN CS material substrate) and CMOS devices. Similarly the CMOS + InGaAs HEMT platform, as shown in Fig. 3(b), can enable circuits that comprise only InGaAs HEMT (on InP-capped formula using self-aligned gate-first process [8]) and CMOS devices. Both hybrid circuits have to be designed and processed separately because of different CS materials used in the processes. The hybrid PDK has been developed with a flag, as described in section 2, for choosing the correct type of CS materials in the DL-BaT process to grow the desired III-V devices on an engineered substrate. It is also used in the PDK to perform LVS and DRC checks. It becomes an important process indicator to integrate III-V devices with the correct type of CS materials into CMOS circuits with the correct setting for LVS and DRC checks on a hybrid design in which to be fabricated on an engineered substrate.

The value for the flag can be easily set in the PDK under the EDA environment setting. This information is important for a hybrid design to synchronize the devices used in a design with the correct materials used before the actual fabrication process. The hybrid verification rules have been designed in such a way that the DRC and LVS rule checks can only be successful when the selected III-V device in a hybrid design matches the chosen III-V layer for the DL-BaT process. Further process development that is underway in LEES will potentially enable to the integration of two, or more, III-V device platforms together with Si CMOS.

5. A Cost-Saving Shared Mask Multi-Project Chip

A multi-project chip (MPC) is a platform to share the IC fabrication resources to fabricate different integrated circuit designs from various teams into a single chip on a wafer. The presented hybrid PDK has been distributed to various research teams. A MPC has been proposed to the teams to share resources on the mask area and the cost of the integration processes. Fig. 4(a) shows a recent tape-out using the MPC platform to fabricate various circuits, such as CMOS transmitter and GaN PA [9], class D audio Amplifiers with InGaAs HEMTs, GaN and InGaP LEDs with CMOS drivers, which were designed with the developed hybrid PDK.

Designers can access CMOS and III-V devices from PCell libraries in the PDK. Designers provided their hybrid circuits with the flag to indicate the type of III-V devices used in the circuits. Their hybrid designs have been

consolidated and tiled on a die. One of the hybrid designs can be the integrated GaN HEMTs into a CMOS circuit, as shown in Fig. 4(b), and another integrated circuit with GaN LEDs into CMOS circuits, as shown in Fig. 4(c). Since the PDK libraries provide all III-V components and CMOS devices, their hybrid layouts on different CS materials can be easily tiled onto a MPC layout.

It depends on the type of CS materials used in the DL-BaT process, the hybrid circuits on the MPC are expected to function fully only with the chosen III-V devices grown on the correct III-V layers. In order to provide sufficient working hybrid circuits to designers, the same MPC can be fabricated on different type of engineered substrate, in which the CS materials layer in the engineered substrate can be from different types of CS material layers. It provides an adequate area and space for low-quantity integrated hybrid circuits with low fabrication cost.

6. Summary

The developed hybrid CMOS/III-V PDK for direct integration of CMOS and III-V devices on a common silicon substrate is presented. It provides shorter design circle times to design high-frequency and high-voltage circuits, in which the circuit performance can be optimized by the strategic placement of III-V devices with CMOS transistors in a single chip, utilizing the foundry-proven back-end multi-layer interconnects to have direct access to the electrical information between the devices.

The PDK has been distributed to designers for designing integrated hybrid CMOS/III-V circuits. Designers utilized a cost-saving MPC platform to fabricate their circuits with the CMOS/III-V devices from the PCell libraries. The PDK is able to support real applications under the industry-standard EDA environment.

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