Fabrication and modeling of resistance switching cells for ReRAM applications

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ABSTRACT

This paper presents the technology, fabrication process, measurements and modeling of resistance switching devices, that were built using nickel oxide (NiO) as for oxide layers between two platinum layers used as metal electrodes. Processing steps were improved to get correct current-voltage characteristics of resistance switching devices. Such devices can be implemented in so called Resistive Random Access Memory (ReRAM). To use it in the ReRAM circuit design the circuit model was created that could be used by commercial simulators. Such model was created based on the Schmitt trigger design with some added modifications. It behaves very similarly to the actual cell under triangular voltage sweep (TVS) excitement and its I-V characteristic resembles the hysteresis. For this reason it could be applied in the ReRAM circuit design.

Keywords: ReRAM, resistance switching, metal-insulator-metal, SPICE model, Schmitt trigger

1 INTRODUCTION

The physical phenomenon of resistance switching has been known for a few decades. It is a conceptually simple event when the oxide which usually behaves like an insulator can change its behavior to a conductor. The structure of the device resembles a sandwich with oxide between top and bottom metal layers, hence its name: metal-insulator-metal (MIM). One type of MIM structure is called binary metal oxide and it is represented by such compounds as TiO_2 and NiO. The insulator between metals is also called Transition Metal Oxide (TMO). When biased with certain type of voltage this structure is able to switch between High Resistance State (HRS) and Low Resistance State (LRS). Such two separate states can be used in a memory cell that would store logical 0 for HRS and logical 1 for LRS. This type of memory has been extensively researched in the last few years and is collectively called Resistive Random Access Memory (ReRAM or RRAM). The binary oxide MIM can be integrated with conventional CMOS process so that different memory structures resembling SRAM or DRAM technologies can be built..

2 RESISTANCE SWITCHING

Structure of MIM cell is shown in Figure 1 together with a voltage source producing a pulse or triangular waveform and the component responsible to limiting current (I_C – compliance current). Also shown is the table with some examples of materials used for top and bottom electrodes and for TMO [1]:

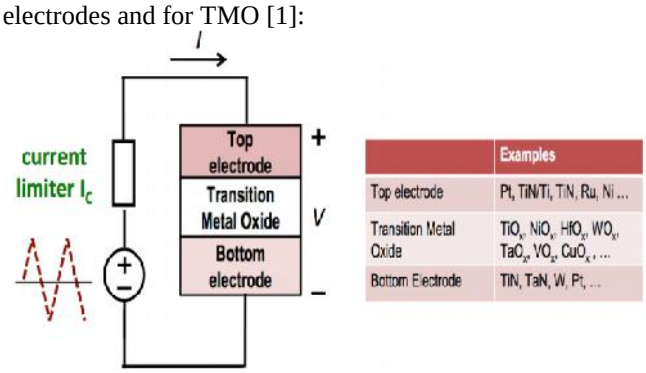


Figure 1: Structure of resistance switching cell [1]

This cell can operate correctly when switching between HRS and LRS occurs. When MIM structure transitions from HRS to LRS it is called 'SET' and when it transitions from LRS to HRS it is called 'RESET'. Often the new sample needs to be electroformed during first application of voltage input – this process is called 'FORMING' and requires the use of voltage that is greater in magnitude than for 'SET' operation. There are two types of 'SET'–'RESET' operations: unipolar and bipolar. For unipolar switching both 'SET' and 'RESET' operations occur for the same polarity of applied voltage (either positive or negative) and the magnitude of this voltage determines switching from HRS to LRS or vice versa. For unipolar switching if both operations occur for both positive and negative voltages it is additionally called 'nonpolar' switching. Bipolar switching occurs when 'SET' operation can only be performed with positive voltage and 'RESET' can be performed with negative voltage (or vice versa). Unipolar switching is preferred due to lower power consumption caused by voltage of unidirectional amplitude. However bipolar switching is usually easier to implement in the circuit because there is no problem with voltage margins as positive voltages cause one type of transition and negative voltages another one. Both types of switching are shown in Figure 2:

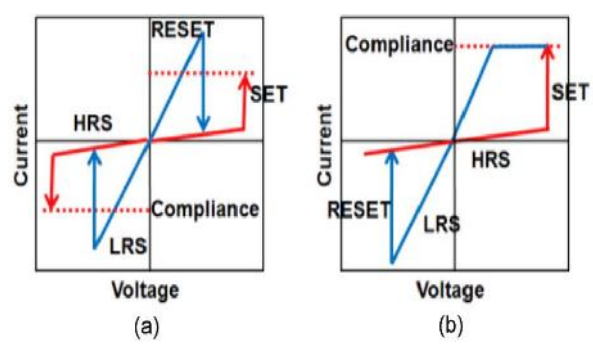


Figure 2: Unipolar and bipolar switching modes [2]

To prevent the cell from breaking down when too much current flows in LRS high current limit is applied – it is compliance current I_C and can be set by the measurement tool as in our setup (for example semiconductor parameter analyzer SPA) or the component controlling I_C can be integrated into the circuit together with MIM structure. Examples of compliance current controlling components include load resistors, diode or transistor [3].

The physics responsible for the resistance switching behavior was explained in a few ways. Majority of approaches show linear (ohmic) relationship in the LRS. However description of the HRS is more complicated. Possible descriptions include: Poole–Frenkel emission ($log(I/V) \sim V^{1/2}$), Schottky emission ($log(I) \sim V^{1/2}$) and Child's square law region relation ($I \sim V^2$) were observed and characterized for different materials. The main conduction behavior depends on different physical phenomena in different MIM structures. They depend on properties of the oxide (bandgap energy, trap energy), fabrication process variations (annealing temperature and atmosphere)) and the properties of metal-oxide boundary (barrier height). All details are still subject of extensive research. Here we will briefly present resistance switching in Nickel Oxide.

Forming (the first time the structure goes from HRS to LRS) and setting (subsequent HRS to LRS transitions) are widely accepted to occur due to dielectric breakdown, where the time of forming and setting depends exponentially on the voltage applied. It is a result of defects caused by stresses in the oxide. Under the influence of electric field the atoms of oxygen in the oxide are removed from the lattice structure and drift in the direction of anode layer. These oxygen vacancies create the conduction filaments responsible for increase of conductivity. For low power efficiency it is better if the forming voltage is as small as possible (ideally equal to set voltage). Such a device is then called forming-free and its application is much easier in the actual circuit structure since no additional voltage is required for first time usage. The thickness of the oxide layer directly influences the magnitude of forming voltage so research focuses on depositing thin oxide layers between metal electrodes. Another factor affecting the forming voltage is the annealing temperature during deposition, because of generation of defects in the oxide that create oxygen deficiencies. We built our samples forming-free taking into account thickness of the NiO layer and annealing temperature. RESET (transition from LRS to HRS) is still not certainly explained by physical phenomenon. In scientific literature it was proposed that thermal dissolution is responsible for switching in the unipolar mode and ionic migration in the bipolar switching mode, at least partially. It was found that the unipolar or bipolar switching mode is determined by both type of oxide and metal used in the MIM structure. Some oxides can be unipolar in combinations with certain metal electrodes and bipolar with others. In our research platinum Pt was used both as top and bottom electrode so we obtained the unipolar switching mode. NiO has been researched as a resistance switching material for a long time and it was found that materials such as Pt, Au, W and Ni can be used as metals. NiO shows unipolar switching with typical reset voltages between 0.5 V and 2 V and set voltages between 1 V and 3 V with reset currents less than 10 µA which was confirmed in our results. Because of unipolar switching in NiO structures, the main problem is to have strictly separated ranges of voltages for set and reset. That can cause failures with reading and writing of potential memory cells.

3 FABRICATION OF NIO CELLS

The fabrication process that we applied to make resistance switching cells is described in this section and the structure of the final MIM NiO cell is shown in Figure 3:

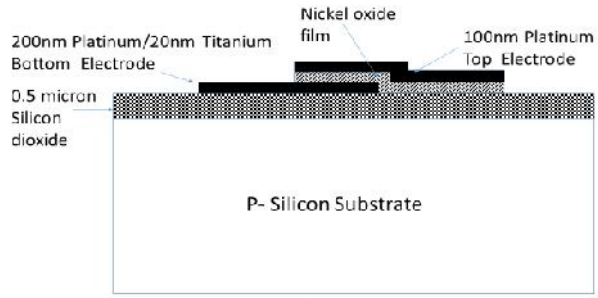


Figure 3: Structure of the resistance switching cell

Metal-insulator-metal structures were built on 4 inch diameter, 500 micron thick silicon substrates with 5000 Å wet thermally grown silicon dioxide (SiO_2). The bottom electrode made of 200 nm of Platinum with 20 nm of titanium adhesion layer was deposited on these wafers by DC magnetron sputtering. This bottom electrode layers were patterned using standard photolithographic technique and ion milling. NiO solution supplied by Kojundo Chemical Laboratory was diluted with n-butyl acetate and spun on these wafers at 2000 rpm for 30 seconds. Each layer resulted in thickness of 12 nm and five layers resulted in thickness of 60nm of NiO film. After the deposition of NiO, each layer was baked at temperature of 150 C for 2 minutes, 280 C for 4 minutes and annealed at 450 C. The sample was finally annealed at a temperature of 450 C for 30 minutes in oxygen. Top electrode platinum of thickness 200 nm was deposited by DC magnetron sputtering. The top electrode was patterned using standard photolithographic technique and ion-milling. Figure 4 shows the micrograph of the fabricated device:

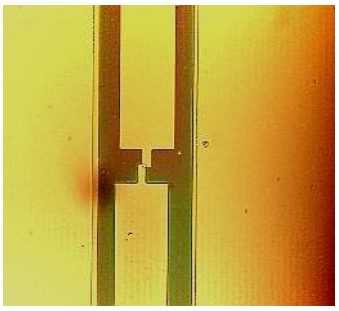


Figure 4: Micrograph of the fabricated switching resistance cell

The actual switching device is placed at the tiny intersection of top and bottom electrodes in the middle of Figure 4. The top and bottom electrodes were big enough to put measurement probes on them but the device was made tiny by mask misalignments during fabrication. Such devices were inspected under the microscope to verify which one could be tested. The wafer was mounted in probe station and devices were analyzed with Semiconductor Parameter Analyzer and Triangular Voltage Sweep (TVS) was applied to them using HP VEE software. Samples were analyzed and voltage sweeping from 0 V to 2 V and back to 0 V with 0.1 V step was applied to each sample. The highest current was set by software to be 10 mA. This was the highest value of current flowing through the cell in the LRS, which was the compliance current. Double sweep from 0 V to 2 V and back to 0 V resulted in 42 values of voltage applied to each sample, and for each of these voltages corresponding current was measured. Figure 5 shows one current-voltage characteristics of NiO resistor under triangular voltage sweep. With increase in voltage, the current increases gradually up to 1.5 Volts. Increase of voltage above 1.5 Volts, results in rapid increases in current confirming switching of resistor to LRS. Since the semiconductor parametric analyzer was set to 10 mA current limiting to avoid melting of device, the current saturates to this value above 1.7Volts. When the applied voltage was decreased from 2V to 0V, at about 1.1V, the current starts decreasing significantly with the applied voltage, confirming the switching to HRS. The memory window or hysteresis in I-V characteristics for this resistor is about 0.4 V for an applied voltage from 0 to 2 V.

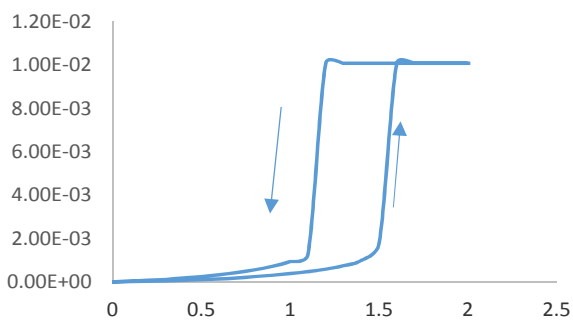


Figure 5: Current-voltage characteristics of a typical NiO switching resistor

4 RESISTANCE SWITCHING MODELING

Models for switching resistance devices already exist. They can be broadly divided into physical models and circuit level models implemented in SPICE. SPICE models can be used in commercial simulators during the design of integrated circuits with switching resistance devices. In our previous paper "Analysis and comparison of memristor models in Verilog-A applied in the design of switching resistance nonvolatile RRAM memories" we presented various Verilog-A models, which are physical models rather than SPICE circuit level models. In these Verilog-A models device behavior is described by physical equations, which are coded in Verilog-A language.

This section presents our approach to resistance switching modeling. We started from the idea that unipolar resistance switching current-voltage characteristics resembles the Schmitt trigger transfer characteristics which looks like hysteresis curve. It has two separate voltages VT+ and VT- and is illustrated in Figure 6:

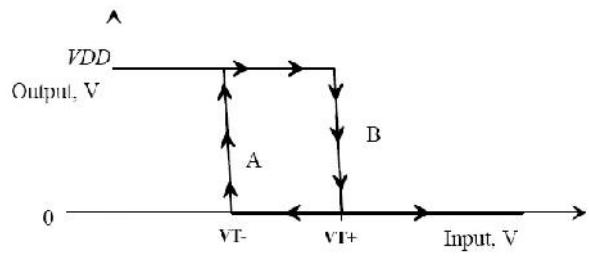


Figure 6: Transfer characteristics of Schmitt trigger.

Current-voltage characteristics from Figure 5 looked like inverted version of Figure 6 with finite resistance in HRS. For the purpose of our analysis we assumed VT+ is set voltage and VT- is reset voltage. We used the alternative version of CMOS Schmitt trigger presented Figure 7:

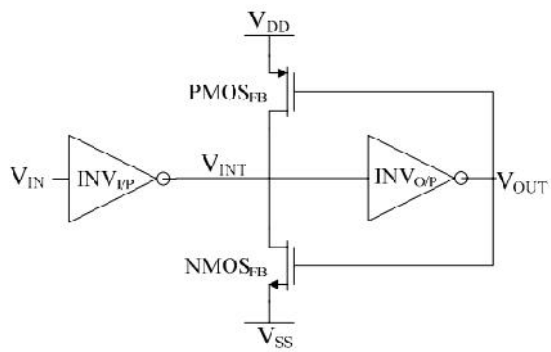


Figure 7: CMOS Schmitt trigger structure

Our goal was to create a circuit that when triangular voltage sweep going from 0 V to 2 V and back to 0 V was applied then the current measured at its output would switch between HRS and LRS and its I-V characteristics would look like Figure 5. Ideal transfer characteristics of Schmitt trigger differed in a few ways from our measured I-V characteristics in Figure 5. A few changes had to be applied to the simple CMOS Schmitt trigger of Figure 7 to make sure its I-V characteristics resembles real measurements

Figure 6 is the transfer characteristics of the Schmitt trigger i.e. it shows output voltage as a function of input voltage. Our resistance switching device had a current-voltage characteristics. For this reason we added resistor R0 in parallel with capacitor C4 to add load to the output voltage and convert it to current. Additionally inverter $INV_{I/P}$ of Figure 7 makes sure the I-V characteristic is of the non-inverting type.

Schmitt trigger transfer characteristic can be thought of as a transfer characteristic of an inverter with two separate

threshold voltages VT+ and VT-, one for falling input and the other for rising input voltage. For the simple CMOS inverter with NMOS pull-down and PMOS pull-up transistors the threshold voltage is given by:

$$V_{th} = \frac{\sqrt{\ _n / \ _p} * V_{Tn} + (V_{DD} - |V_{Tp}|)}{1 + \sqrt{\ _n / \ _p}} \qquad (1)$$

In equation (1) β_n, V_{Tn}, β_p, V_{Tp} are transconductance parameters and threshold voltages of NMOS and PMOS transistor respectively and V_{DD} is a voltage supply. Analyzing the circuit of Figure 7 and assuming $NMOS_{FB}$ and $PMOS_{FB}$ have transconductance parameters β_{n1} and β_{p1} and $INV_{O/P}$ has NMOS and PMOS transistors that have transconductance parameters β_{n2} and β_{p2} one can calculate the effective transconductance ratios for cases when $V_{in} = 0$ and $V_{in} = V_{DD}$. Those two ratios determine VT+ and VT- and are given by equations 2 and 3:

$$_A = \ _{n2} / (\ _{p1} + \ _{p2}) \qquad (2)$$

$$_B = (\ _{n1} + \ _{n2}) / \ _{p2} \qquad (3)$$

With (2) and (3) we can adjust transistors' transconductance ratios and consequently their sizes to make sure we get VT+ and VT- similar to those from Figure 5. We used transistors of length L = 0.18µm and for simulation we used BSIM3v322 models so by adjusting width W of transistors we were able to control VT+ and VT-.

We had to make sure that the transition from HRS to LRS and vice versa is not abrupt but gradual. To make it happen we added PMOS transistor M6 with source at V_{DD} and gate grounded in parallel with capacitor C0. It made the transition smooth.

Another improvement was ensuring that resistance in HRS is of some finite value instead of infinite as in the case of ideal Schmitt trigger. To make sure it is the case we had to make sure NMOS pull-down transistors are slightly on (at the edge of conduction) while PMOS pull-up network is on. We did it by adding voltage source V5 of negative magnitude that would increase V_{GS} of pull-down network.

Figure 8 below presents the circuit based on the Schmitt trigger model with the above-mentioned improvements:

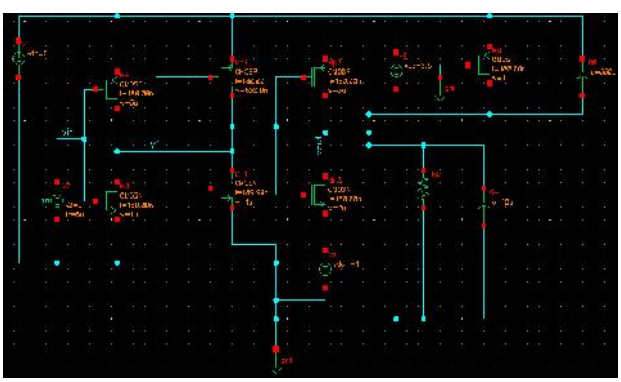
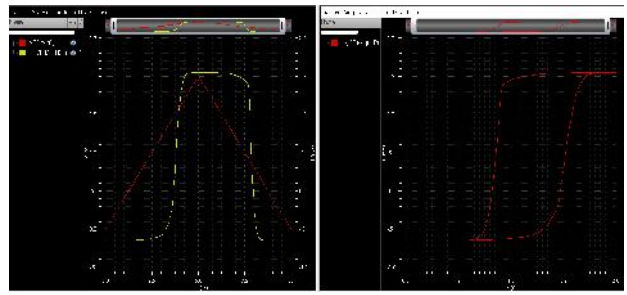


Figure 8: Circuit modeling resistance switching device.

Applying the TVS going from 0 V to 2 V and back to 0 V gives us the following I-V characteristics:



(a) (b)

Figure 9: (a) input voltage (red) and output current (yellow) and (b) I-V characteristic resembling the hysteresis with two visible high resistance and low resistance states

Such a model could be of practical value for SPICE simulations of actual integrated circuit containing resistance switching devices. Setting appropriate value for transistor widths, load resistor and capacitors as well as voltage source connected to sources of NMOS pull-down transistors we can control VT+, VT-, smoothness of HRS to LRS and LRS to HRS transition and resistance of a device in HRS. This model could also be used for transient simulations.

5 CONCLUSIONS

Resistance switching devices can be used in ReRAM types of memory. In this paper we presented physical background behind resistance switching and how they are described. In order to create memory circuits we first had to prove that manufacturing of a single robust and reliable resistance switching cell is possible. We were able to get switching between high resistance state (HRS) and low resistance state (LRS) with different set and reset voltages for 6 different samples. Next step was to create the circuit model that would replicate the same switching behavior. We based our model on CMOS Schmitt trigger and added a few components that would introduce I-V characteristics non-idealities. By changing resistances, capacitances and voltages of added components we can adjust our model's behavior to fit the specific resistance switching cell.

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