Compact Modeling for UTBB-FDSOI Technologies: Main Challenges and Possible Solutions

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ABSTRACT

Fully-Depleted Silicon-On-Insulator technologies featuring Ultra-Thin silicon Body and Buried oxide have now entered into industrial production stage. These technologies present several decisive advantages over other options, such as excellent transistor electrostatic control, very low variability, simple planar process close to conventional bulk one, and very efficient back-bias effect. This latter feature allows dynamic modulation of delay/power trade-off, which is a powerful know at circuit level. To take full advantage of these technologies, circuit designer need compact models able to describe the transistor behavior over wide ranges of back biases, which requires considering FDSOI transistors as real Independent Double Gate MOSFETs. We review here the challenges to address in order to build such compact models and we describe the solutions developed for Leti-UTSOI2, a complete and mature compact model valid and predictive in all bias configurations and in use in industrial design kits.

Keywords: spice, compact model, fdsoi, independent double gate, transistor

1 INTRODUCTION

Transistors with fully-depleted low-doped thin body are now produced industrially for 28nm technology generation and below [1]. These devices are highly scalable thanks to their excellent electrostatic integrity and benefit from reduced variability since they do not suffer from random dopant fluctuations [2]. Among thin body transistor architectures, Fully-Depleted Silicon-On-Insulator (FDSOI) devices designed with Ultra-Thin Body and Buried oxide (UTBB) are very attractive for several reasons. First, they are planar transistor and their process integration is close to that of conventional bulk devices [1]. Second, they exhibit significant threshold voltage dependence with the bias applied to the well located below the buried oxide, and this efficient back-bias effect is preserved down to deca-nanometer transistor gate lengths [3]. At circuit level, this feature provides a way to modulate the speed / power trade-off significantly, which is a powerful knob for circuit performance / consumption optimization (see for example [4-6]). In particular, such flexibility is key for ultra-low power Internet-of-Things applications [7-8]. As a consequence, UTBB-FDSOI compact models have to describe accurately transistor characteristics on the widest possible back bias range, so that circuit designers can eventually take full advantage of the technology versatility.

In this paper, we review the main challenges associated to this need, and we detail possible solutions through the description of Leti-UTSOI2 compact model [9-10]. In section 2, we illustrate the effect of large back biases on fundamental transistor characteristics, and we highlight from this short analysis the basic requirements that must be fulfilled by UTBB-FDSOI compact models. Section 3 details the resulting challenges for surface potential analytical calculation and describes the solution developed three years ago for Leti-UTSOI2 [11]. In section 4, we describe the specificities of UTBB-FDSOI transistors in terms of quantum confinement and back gate depletion and way of modeling these effects. In section 5, we first discuss the challenges associated to the derivation of a drain current closed form equation valid in all operation regimes. Then, we describe some specificity that has to be accounted for FDSOI DC characteristics. Section 6 is dedicated to a brief description of the charge model. Finally, section 7 gives an overview of physical ingredients introduced in Leti-UTSOI2 and illustrates its accuracy against silicon data.

2 FDSOI AS INDEPENDENT DOUBLE GATE TRANSISTOR

After device description, we detail in this section the impact of back bias on long channel transistor electrostatic behavior.

2.1 Device description

In UTBB-FDSOI technology, the doped region located just below the buried oxide, called backplane [1], can be biased through the well and acts as a second transistor gate, with the buried oxide as back gate dielectric. Transistors can then be designed with regular-wells (well type opposite to that of source drain) or with flip-wells (same well type as that of source drain). This provides a simple way to define two device flavors with a unique gate stack [1]. Figure 1, left, shows a schematic of FDSOI transistor. As for conventional bulk devices, four electrodes have to be considered, the thin fully-depleted body of the device being not directly accessible.

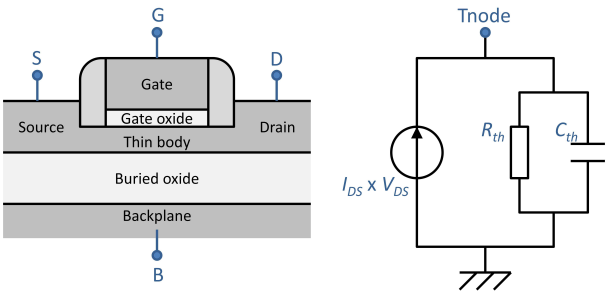

Figure 1: Schematic of UTBB-FDSOI MOSFET (left) and thermal network used to account for self-heating effect (right).

Moreover, it is well known that, because of the presence of the buried oxide, which is about 100x more thermally resistive than silicon, self-heating is an important effect to consider in FDSOI transistor modeling [13]. Therefore, a fifth thermal node, that gives the channel temperature elevation induced by self-heating with respect to ambient temperature, has to be introduced. In Leti-UTSOI2, self-heating effect is considered in a conventional way, with a thermal node connected to the ground through a parallel thermal RC network, in which the dissipated power is supplied (figure 1, right). Thermal resistance and capacitance are scalable with device geometry, and the thermal node can be optionally accessed in the netlist from version 2.1 of the model.

2.2 Impact of back gate bias

When a back gate bias is applied to UTBB-FDSOI transistor, electrostatic behavior is significantly impacted. Since the description of device electrostatics is essential for predictive MOSFET modeling, it is very important that UTBB-FDSOI compact models are able to reproduce the gate to channel capacitance as a function of back gate bias in reverse and forward bias modes. Such capacitance, simulated with self-consistent Poisson-Schrödinger solver, is plotted against gate voltage for back gate biases of -3V, 0V and +3V in fig. 2. While the C(V) characteristic exhibits a somewhat classical shape for negative or null V_{bs}, a double plateau behavior can be observed for positive V_{bs}. This is due to the creation of a strong inversion charge at the back interface of the thin body. On the first plateau, the gate to channel capacitance value corresponds to the gate oxide capacitance in series with the thin body dielectric one. Once strong inversion layer is created at the bottom of the thin body, both interfaces are relatively decoupled and, as V_{gs} is further increasing, a second channel appears at the front interface. The resulting mobile charge concentration profiles in the thin body at V_{gs}=1V are illustrated in fig. 2, inset.

As a consequence, we need to consider the device as an Independent Double Gate device, with possible channel creation at both interfaces of the thin body. If the creation of strong inversion layer at the back interface is neglected, the device electrostatics is correctly described from reverse to null back bias, but the model is less and less accurate as we go towards forward back bias. The need for dual channel operation description impacts significantly not only the surface potential calculation procedure, but also the way of modeling the drain current and intrinsic charges.

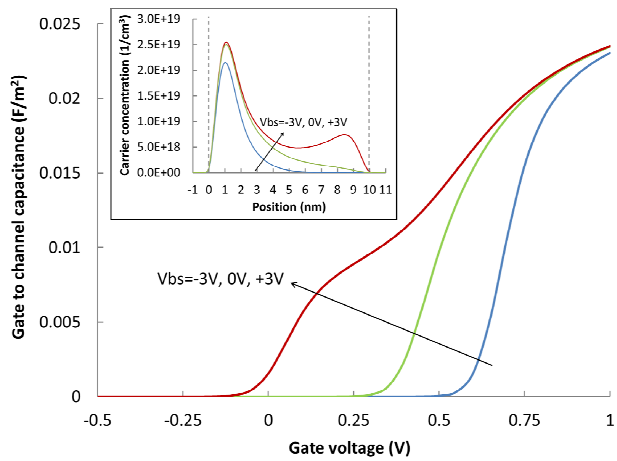

Figure 2: Gate to channel capacitance versus gate voltage obtained from self-consistent Poisson-Schrödinger simulations for UTBB-FDSOI transistor with T_{ox}=1nm, T_{Si}=10nm, T_{box}=25nm. Inset: Carrier concentration vertical profiles in the thin body at V_{gs}=1V.

3 INTERFACE POTENTIAL MODEL

The need for accurate modeling of dual channel operation is actually the main challenge for UTBB-FDSOI compact models. In particular, finding an accurate and computationally efficient resolution procedure for interface potentials, valid in all operation regimes, is a complex problem. While an extensive literature exists on this topic [14-22], the first straightforward solution without approximation and without numerical loop has been proposed in [11]. The mathematical difficulty comes from the fact that, depending on applied biases, integrations of Poisson's equation with boundary conditions leads to a set of equations involving either hyperbolic or trigonometric functions [23]. In this section, we briefly describe the interface potential calculation solution developed for Leti-UTSOI2. More details can be found in [9].

3.1 Initial set of equations

UTBB-FDSOI transistors are generally designed with low-doped channels [1]. Thus, defining the electrostatic potential ψ as the difference between the midgap energy position at a given location (y,z) in the device with respect to the Fermi level in the source, long channel Poisson's equation and boundary conditions write:

$$\frac{\partial^2\psi}{\partial z^2}(y,z) = \frac{qn_i}{\varepsilon_{ch}} e^{(\psi(y,z)-\phi_{im}(y))/\phi_t} \quad (1)$$

$$Q_g(y) = -\varepsilon_{ch}\frac{\partial\psi}{\partial z}(y,0) \quad (2)$$

$$Q_b(y) = \varepsilon_{ch}\frac{\partial\psi}{\partial z}(y,T_{Si}) \quad (3)$$

In (1)-(3), q is the elementary charge, n_i the intrinsic carrier concentration, ε_{ch} the thin body dielectric permittivity, ϕ_t the thermal voltage, ϕ_{im} the quasi-Fermi level, Q_g and Q_b charge densities in front and back gate, respectively.
Integrating Poisson's equation with (2) and (3), and simplifying the writing by removing explicit dependence upon position y along the channel, we obtain three coupled equations (see Appendix A of [9] for calculation details):

$$Q^2 = Q_g{}^2 - 2qn_i\varepsilon_{ch}\phi_t e^{(V_{gs}-\Delta\phi_g-\phi_{im})/\phi_t} e^{-Q_g/(C_{ox}\phi_t)} \quad (4)$$

$$Q^2 = Q_b{}^2 - 2qn_i\varepsilon_{ch}\phi_t e^{(V_{bs}-\Delta\phi_b-\phi_{im})/\phi_t} e^{-Q_b/(C_{box}\phi_t)} \quad (5)$$

$$\frac{Q}{2C_{Si}\phi_t} + \coth^{-1}\left(\frac{Q_g}{Q}\right) - \coth^{-1}\left(-\frac{Q_b}{Q}\right) = 0 \quad (6)$$

In (4) to (6), $\Delta\phi_g$ and $\Delta\phi_b$ are the front and back gate workfunctions, respectively, referenced to silicon midgap level, and C_{ox}, C_{box} and C_{Si} are front gate oxide, buried oxide and thin body dielectric capacitances, respectively. Q is a function of y coming from the first integration of (1). It is homogeneous to a charge density (or to an electrical displacement) but, actually, this quantity can be either real (hyperbolic mode, coupled interfaces), or imaginary (trigonometric mode, decoupled interfaces). Equation (6) has been written here with complex notations. In trigonometric mode, Q is imaginary and (6) involves $\cot^{-1}$ function instead of $\coth^{-1}$.

3.2 Set-up of a unique equation to solve

The dependence of the form of (6) upon applied biases makes it not convenient for analytical calculation of gate charge densities. To tackle this difficulty, (6) can be modified by using well known identity of coth(a-b), to get:

$$Q\coth\left(\frac{Q}{2C_{Si}\phi_t}\right)(Q_g + Q_b) + Q_gQ_b + Q^2 = 0 \quad (7)$$

Equation (7) is much more convenient than (6), because it can be considered as a function of Q^2. Indeed, when plotted as a function of Q^2, the first term of the equation presents a naturally smooth continuity between hyperbolic (positive Q^2 values) and trigonometric (negative Q^2 values) modes. Such natural continuity can be exploited by considering Q_g, Q_b and Q^2 as the three real unknowns to be determined from (4)-(5)-(7).

As shown in [9], we can build a unique equation to solve by choosing Q_g as unique input variable and by combining (4), (5) and (7) in such a way that abrupt dependences upon Q_g are avoided as much as possible:

$$f(Q_g) = 0 = \left(Q_g + Q\coth\left(\frac{Q}{2C_{Si}\phi_t}\right)\right)(Q_g + Q_b) - 2qn_i\varepsilon_{ch}\phi_t e^{(V_{gs}-\Delta\phi_g-\phi_{im})/\phi_t} e^{-Q_g/(C_{ox}\phi_t)} \quad (8)$$

In (8), Q and Q_b are defined as functions of Q_g from (4) and from combination of (4), (5), (7), respectively. Notice that finding Q_g is equivalent to calculating the top surface potential ψ_{sf}, since both quantities are related through the boundary condition at the front interface $Q_g=C_{ox}(V_{gs}-\psi_{sf})$.

During the resolution of (8), a particular attention has to be paid to the fact that it admits infinity of roots in the trigonometric mode. Only the highest of these roots being physical, any underestimation of Q_g has to be avoided during the resolution procedure.

3.3 Analytical model of interface potentials

With (8), we can set-up a straightforward resolution based on an initial guess of Q_g followed by a few error correction steps. Several ways can be followed to build the initial guess. The solution used in Leti-UTSOI2 starts from the calculation of the interface potentials, in absence of mobile charges, from the capacitive divider formed C_{ox}, C_{Si} and C_{box} in series. After a smooth saturation of these interface potentials to their value at the onset of strong inversion, a second calculation is carried out, still neglecting mobile charges, to account for the effect of strong inversion at the opposite interface. After making the obtained potential saturate to their threshold value, we get interface potentials with a good accuracy in the subthreshold regime whatever the back gate bias [9].

From this initial guess, Householder's method can be used with function $f(Q_g)$ given by (8) to compute the front gate charge density. Applying this correction once leads to an excellent accuracy of Q_g in subthreshold and moderate inversion regimes, but also to possible overestimation of Q_g in strong inversion. To avoid ending up with unphysical solution, a correction step is thus applied to Q_g in the strong inversion regime prior to the second Householder correction. This intermediate step is based on an approximation of $Q\coth(Q/(2C_{Si}\phi_t))$ in the trigonometric mode, which allows expressing Q^2 as an explicit function of Q_g and Q_b from (7) [9]. The correction term to add to Q_g is then given by a first order Taylor expansion of (4). This specific strong inversion correction being carried out twice, Householder 2nd order correction based on (8) can be safely applied again. Applying it twice leads to an excellent accuracy on the front interface potential, with a maximal error of a few fV for typical UTBB-FDSOI geometries [9].

This straightforward resolution procedure is very accurate and numerically very robust for large ranges of

transistor geometries, from real Independent Double Gate to thick BOX FDSOI transistors, and for very wide ranges of applied back biases, as shown in [9]. It provides a very solid basis on which DC and AC core models are built to describe device behavior without any back bias limitation.

4 QUANTUM CONFINEMENT AND BACK GATE DEPLETION

We briefly describe in this section the particularities of UTBB-FDSOI transistors in terms of quantum confinement and back gate depletion.

4.1 Quantum confinement effect

In thin body transistors, quantum confinement has two origins: a geometry-related one, since the thin body sandwiched between front and back gate oxides constitutes a quantum well, and a bias-dependent one, corresponding to the well induced and modulated by the transverse electric field. A proper general solution can be obtained by using the variational approach [24].

In Leti-UTSOI2, a simpler yet accurate approach is chosen [10]. Geometry-related confinement is simply taken into account by applying an offset to front and back gate biases, which corresponds to the elevation of the first sub-band in a square-well of thickness T_{Si}.

On the other hand, field-related confinement is considered in two steps. First, bias dependent dark-spaces are computed within triangular well approximation, neglecting the impact of mobile carriers. These dark-spaces are used to modify the effective vertical geometry of the transistor prior to interface potential calculation. A second order correction is applied *a posteriori* on current and charge models to account for the impact of mobile charges on these dark-space thicknesses.

As shown in [10,11,25], this approach leads to an accurate description of transistor electrostatics when compared to self-consistent Poisson-Schrödinger simulation results and to hardware data.

4.2 Back gate depletion modeling

Back gate of UTBB-FDSOI transistors is made of doped silicon. Therefore, it is important to account for possible depletion effect in this gate in order to properly model the back bias dependence of threshold voltage and the gate to substrate capacitance. Leti-UTSOI2 incorporates this effect, modeled through back gate effective voltage calculation carried out prior to interface potential resolution. Illustration of the achieved accuracy on device characteristics can be found in section 7 and in [25].

5 DC MODEL

Since mobile charge is distributed within the thin body, with possible strong inversion layer at front, back or both interfaces, several aspects have to be considered in order to properly model the drain current of UTBB-FDSOI devices:

- Charge sheet approximation cannot be used.
- Front interface potential gradient along the channel is not relevant to describe the drift current in all bias configurations (same statement applies for back interface potential).
- When two channels co-exist, carriers experience different transverse fields at front and back interfaces.

5.1 Drain current and mobility

From interface potential calculation described in section 3, compact expression of inversion charge densities Q_{inv} can be obtained at source and drain sides, without any assumption about the repartition of this charge in the body [9]. Then, since front or back interface potential gradient cannot be used to describe the drift current in the general case, we have defined, from the most general drain current expression, an effective electrostatic potential whose gradient governs the drift current whatever the position of the charge centroid [10]:

$$\psi_{eff} = \phi_{im} + \phi_t \ln\left(Q_{inv}/\left(C_{Si}\phi_t\right)\right) \tag{9}$$

From the analysis of the dependence of the inversion charge density profile along the channel with this effective potential, it turns out that Q_{inv} linearization can be assumed in most cases, except at high drain voltage when two channels co-exist at source side. In this latter case, the $Q_{inv}(\psi_{eff})$ curve presents two distinct slopes, corresponding to two different sections of the channel [11]. At source side, two channels are created and interfaces are completely decoupled. When moving towards the drain, after the pinch-off of the weakest channel, both interfaces are more coupled, which induces a different body factor in that second section. This IDG specificity makes simple current expression obtained from Q_{inv} linearization fail to reproduce the transistor saturation current in forward back bias mode.

In Leti-UTSOI2, inversion charge symmetric linearization has been generalized to account for the different slopes of $Q_{inv}(\psi_{eff})$ at source and drain sides. From a smooth integrable maximum function between two linear dependences, a closed form equation can be obtained for the drain current [10].

In addition, one has to consider that carriers at front and back interface are not submitted to the same transverse electric field, and are possibly confined against interfaces of different natures (e.g. high-k at front interface and thermal oxide at back interface). This must be taken into account in the mobility model. In Leti-UTSOI2, inversion charge is split between front and back one when two channels co-exist. In addition to the fact that appropriate effective field is considered for each channel, Leti-UTSOI2 includes also the possibility to have different mobility values at front and back interfaces.

5.2 Short channel effects

In FDSOI transistors, source/drain can influence the channel by capacitive coupling not only within the body but also through the buried oxide [26]. To account for short channel effects (SCEs) in a physical way, a bi-dimensional capacitance network is used in Leti-UTSOI2, in which source/drain are coupled with both interfaces of the thin body [10]. From this 2D description, an equivalent 1D scheme is derived, so that short channel interface potentials are calculated with the 1D calculation presented in section 3. This provides a consistent modeling of subthreshold slope degradation, DIBL and threshold voltage roll-down, predictive against technological parameters [27]. In addition, a particular care is taken in Leti-UTSOI2 to provide an accurate description of the moderate inversion regime. From version 2.1, the possibility to have a modulation of electrical channel length with V_g and V_b has been introduced, to account for gradual source/drain junctions and to improve further the model accuracy [27].

5.3 Series resistance, velocity saturation, overshoot and channel length modulation

In addition to short channel electrostatic effects, other physical effects such as series resistance, including its dependence with gate voltage, velocity saturation and channel length modulation are introduced in Leti-UTSOI2. The modeling of these effects is close to that of bulk transistor models, except for velocity saturation, for which a particular attention has again to be paid to the case of dual channel operation for $V_{ds,sat}$ calculation [10]. In addition, velocity overshoot effect is captured thanks to the length scaling of saturation velocity parameters, so that drain current and output conductance of short channel transistors in saturation mode are accurately described [25].

6 AC MODEL

Possible dual channel operation has also to be considered for the intrinsic charge model. This requires in particular a consistent model of Ward-Dutton inversion charge partitioning between source and drain. An efficient way to get integrated charges on all terminals, based on an effective gate charge concept, has been proposed in [12]. This approach, adapted in Leti-UTSOI2, provides a very accurate description of all (trans)capacitances [10] and is fully compliant with Gummel symmetry.

Besides this intrinsic charge model, Leti-UTSOI2 incorporates also all required parasitic charges to provide a complete AC model.

7 MODEL OVERVIEW

In this final section, we summarize all the effects accounted for in Leti-UTSOI2 and we briefly illustrate its accuracy against hardware data.

7.1 Summary of included effects

Leti-UTSOI2 includes all the effects required to describe physically and accurately deca-nanometer transistors. Electrostatic device description, based on interface potential calculation valid in all operation regimes, accurately accounts for interface coupling and dual channel operation. As described in section 4, quantum confinement and back gate depletion effects are included, as well as a predictive model of short channel electrostatics. Besides the ingredients of the DC and AC models described in sections 5 and 6, Leti-UTSOI2 includes also parasitic current models (gate current, GIDL/GISL) adapted from bulk ones. A STI-based stress model is also included, and a new stress model dedicated to UTBB-FDSOI specificities has been developed [27] and will be available soon. Leti-UTSOI2 incorporates also noise models, including flicker, thermal, induced gate and shot noise components. Finally, all temperature dependences are described, as well as self-heating effect, as mentioned in section 2.

7.2 Comparison with experimental data

An extensive validation of Leti-UTSOI2 against hardware data from 28nm FDSOI technology developed by STMicroelectronics, including V_{bs} dependence, geometry and temperature scaling, can be found in [25]. Here, we briefly show a few comparisons on key characteristics.

Figure 3 shows a gate to channel capacitance measured on a long transistor with 25nm BOX for various V_{bs} from -10V to +10V. The two plateaus behavior described in section 2 is clearly visible in forward back bias mode and accurately reproduced by Leti-UTSOI2, by adjusting only a few process parameters (T_{ox}, T_{Si}, T_{box}, $\Delta\phi_g$ and backplane doping level).

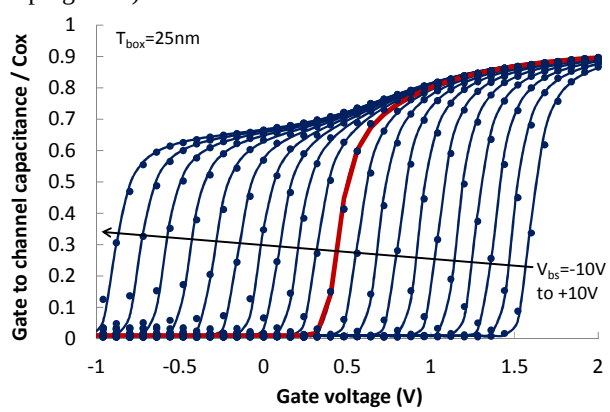

Figure 3: Gate to channel capacitance versus V_{gs} for V_{bs} from -10V to +10V. Measurement results (dots) are accurately reproduced by Leti-UTSOI2 (lines).

Figure 4 evidences that accurate description of transfer and output characteristics can be obtained with Leti-UTSOI2 for transistors as short as 20nm.

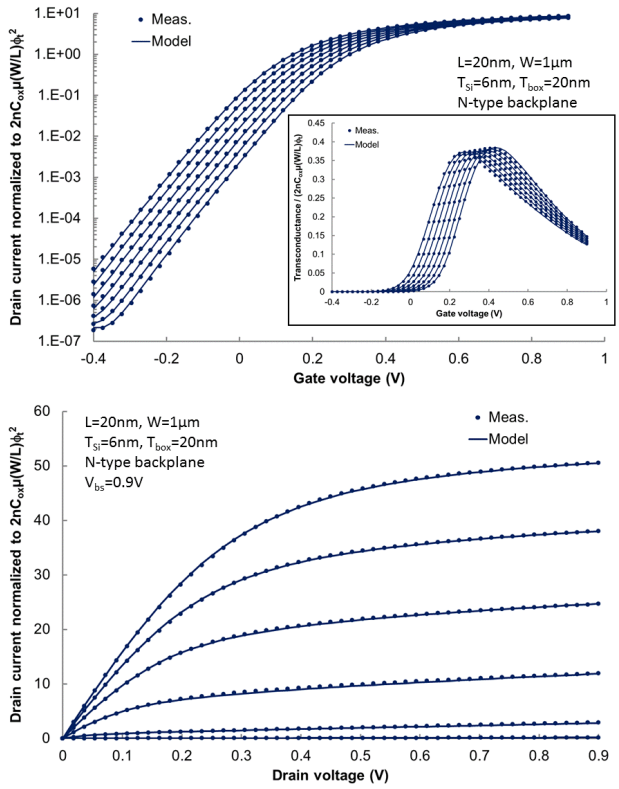

Figure 4: Transfer (top) and output (bottom) characteristics of a 20nm gate length nMOSFET in forward back bias mode. Accurate description of measurements (dots) is achieved with Leti-UTSOI2 (lines).

Thanks to its strong physical background and to its ability to describe device behavior in all bias configurations, Leti-UTSOI2 has also been successfully used to model 28nm FDSOI transistor RF characteristics, including back-gate F_t and F_{max} cut-off frequencies [28].

8 CONCLUSION

UTBB-FDSOI transistors have to be considered as Independent Double Gate MOSFETs with possible conduction at both interfaces of the thin body. Leti-UTSOI2 has been developed to reproduce accurately and predictively such device behavior in all regimes of operation, including strong forward back biases. This model incorporates all the effects required to describe accurately deca-nanometer devices. It features high accuracy and predictability over technological parameters, has been extensively validated against hardware data and is compliant with standard requirements from quality assurance and convergence tests. Leti-UTSOI2 is available in all major commercial SPICE simulators and is successfully used in industrial design kits.

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