Compact Modeling of Long-Term MOSFET Degradation for Predicting Circuits Degradation

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ABSTRACT

We propose a prediction method of long-term metal oxide semiconductor field effect transistors (MOSFETs) degradation to realize CMOS circuit design for reliability. Negative bias temperature instability (NBTI) and hot carrier effect are considered as physical origins of the degradation. During long-term use, CMOS circuit degradation affects the circuit operation. Moreover the circuit operation also affects the CMOS circuit degradation. The develeped method can be utilized for this purpose even after long-term use, and has been verified at different long-term stress conditions by comparison with the actual transient simulation using physical models.

Keywords: negative bias temperature instability, hot carrier, degradation, CMOS, modeling

1 INTRODUCTION

Prediction methods of long-term degradation for both p- and n-type metal oxide semiconductor field effect transistors (MOSFETs) in CMOS circuits are proposed. During CMOS circuit degradation, not all the MOSFETs but only several MOSFETs degrade crucially. Therefore it is required to detect the most degraded MOSFET suffered from given circuit operation condition at given degradation time. The developed long-term degradation methods can be utilized for this purpose and enable the optimization on circuit design for reliability.

In section 2 physical models and long-term degradation methods are shown for negative bias temperature instability (NBTI) and hot carrier. In section 3 CMOS circuit simulation with long-term degradation methods is demonstrated. Finally conclusions are presented in Section 4.

2 METHOD

Different physical phenomena are responsible for the degradation, NBTI in p- and hot carrier effect in n-MOSFETs. Miura-Mattausch et al. has modeled both phenomena for realizing CMOS circuit simulation [1-4] from the physical point of view. To apply the models on a practical circuit, however, not only short-term degradation but also long-term degradation must be predicted. In this study we have developed the long-term NBTI degradation method for p-MOSFETs and the long-term hot carrier degradation method for n-MOSFETs and implemented them into the surface potential based compact model HiSIM [5] for CMOS circuit simulation with long-term degradation effect. An important advantage of the developed methods is the simplicity of the simulation with minimum simulation time while keeping the physically correct concept of the degradation mechanism.

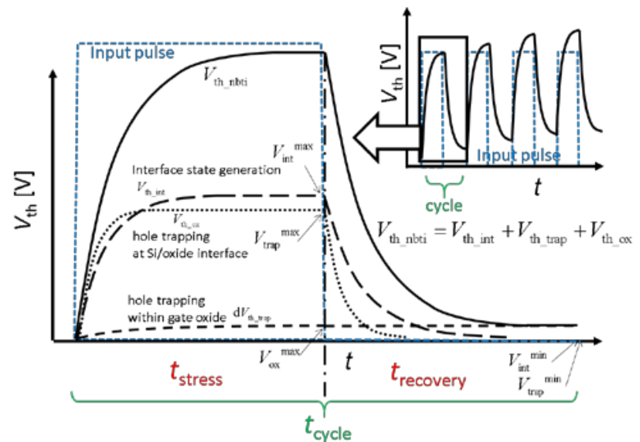

Fig. 1. Schematic of the threshold degradation of NBTI model which consists of three mechanisms, interface state generation, hole trapping at Si/oxide interface, and hole trapping within gate oxide. V_{int}^{max}, V_{trap}^{max}, and V_{ox}^{max} are maximum value of V_{th_int}, V_{th_trap}, and V_{th_ox} for each stress/recovery cycle, respectively.

2.1 Physical Model of NBTI in p-MOSFETs

The NBTI effect is caused by positive charge buildup in the gate oxide and observed as a threshold voltage shift. In this paper, we treat NBTI as uncorrelated contribution from interface-state generation and hole trapping at Si/oxide interface , and hole trapping within gate oxide (Fig.1). Moreover NBTI is modeled as a function of oxide field E_{ox}. [6]

The interface-state generation can be written as

$$V_{\text{th_int}}(t) = \frac{q}{C_{\text{ox}}} R_{\text{str}} \log(1 + \frac{t_{\text{stress}}}{\tau_{\text{s}}}) \quad (1)$$

with

$$\frac{q}{C_{\text{ox}}} R_{\text{str}} = M_{\text{Rstr}} \exp(N_{\text{Rstr}} \cdot E_{\text{ox}})$$

where M_{Rstr}, N_{Rstr}, are model parameters, and τ_{s} is interface generation time constant.

$V_{\text{th_int}}$ recovers as follows.

$$V_{\text{th_int}}(t) = 1 - R_{\text{rec}} \cdot \log(1 + \frac{t_{\text{recovery}}}{\tau_{\text{rec}}}) \quad (2)$$

where R_{rec} is a model parameter.

The hole-trapping in the pre-existing interface traps is described as

$$V_{\text{th_trap}} = \frac{q}{C_{\text{ox}}} N_{\text{trap0}} [1 - \exp(-\frac{t_{\text{stress}}}{\tau_{\text{c}}})] \quad (3)$$

With

$$\frac{q}{C_{\text{ox}}} N_{\text{trap0}} = M_{\text{Ntrap}} \exp(N_{\text{Ntrap}} \cdot E_{\text{ox}})$$

where M_{Ntrap} and N_{Ntrap} are model parameters; and τ_{c} is defined as the hole-capture time.

$V_{\text{th_trap}}$ recovers as follows

$$V_{\text{th_trap}} = \exp(-\frac{t_{\text{recovery}}}{\tau_{e}}) \quad (4)$$

where τ_{e} is hole emission time constant.

Holes tunneling from the substrate into the gate oxide generate traps in the gate oxide. By integrating the trap distribution along the vertical direction, the oxide trap density is derived. The density is described as power-law function of stress time with time exponent [7]. The hole-trapping within gate oxide degradation is written as

$$V_{\text{th_ox}} = \frac{q}{C_{\text{ox}}} N_{\text{ox}} t^{\text{SITA}} \quad (5)$$

with

$$\frac{q}{C_{\text{ox}}} N_{\text{ox}} = GL_1 \cdot \exp(-\frac{GL_2}{E_{\text{ox}}})$$

where SITA, GL_1 and CL_2 are model parameters.

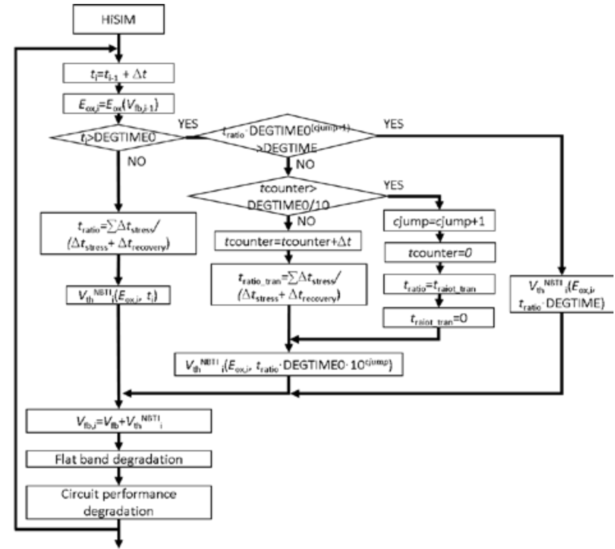

Fig. 2. Flow chart of the NBTI model implementation into the compact model HiSIM.

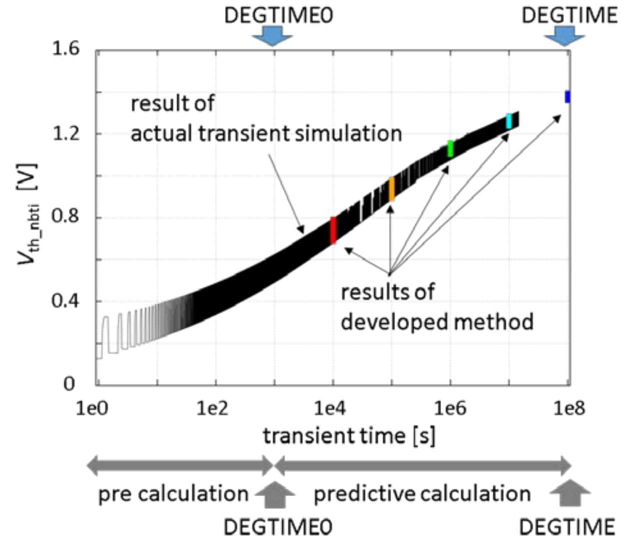

Fig. 3. AC (sine wave, -1.8V@1Hz) transient simulation results with long-term NBTI degradation method at different degradation times. The actual transient simulation with physical NBTI models is dipicted together for confirmation of prediction capability of the developed method.

Table 1. Comparison of NBTI degradation voltages for 3 methods: actual transient simulation with physical NBTI models, long-term degradation method (constant t_{ratio}), and long-term degradation method (re-calculated t_{ratio}).

degradation time [sec.]		1e4	1e5	1e6	1e7	1e8
Actual. tran. simulation		0.679	0.887	1.076	1.217	—
Long-term deg. method	constant t_{ratio}	0.688	0.900	1.090	1.252	1.407
	Re-cal. t_{ratio}	0.688	0.892	1.085	1.225	1.332

2.2 Long-term NBTI Degradation Method for p-MOSFETs

In the NBTI model of long-term AC simulation, hole-trapping within gate oxide dagradateion becomes dominant factor because there is no recovery (5). Hence hole-trapping within gate oxide degradation is re-written as

$$V_{\mathrm{th_ox}} = N_{\mathrm{ox}} \cdot (t_{\mathrm{ratio}} \cdot \mathrm{DEGTIME})^{\mathrm{SITA}} \tag{6}$$

where DEGTIME is degradation time of long-term degradation method and t_{ratio} is a ratio of stress time to simulation time. The t_{ratio} is described as

$$t_{\mathrm{ratio}} = \frac{\sum_{i=0}^{\mathrm{DEGTIME0}} t_{\mathrm{stress}}}{\sum_{i=0}^{\mathrm{DEGTIME0}} (t_{\mathrm{stress}} + t_{\mathrm{recovery}})} \tag{7}$$

where DEGTIME0 is simulation time of pre calculation to determine the t_{ratio}. The t_{ratio} should vary even after pre-calculation. Therefore it is re-calculated during predictive calculation from DEGTIME0 to DEGTIME (Fig. 2, 3). In Fig. 3 (note that DEGTIME0: 1e3 and DEGTIME: 1e8 seconds), the $V_{\mathrm{th_nbit}}$ is calculated with long-term degradation method by following procedure:

1. Perform the simulation until 1e3 sec. as pre calculation to obtain t_{ratio}.
2. Perform the simulation at 1e4 sec. using the t_{ratio} which is calculated during pre-calculation. In this step the t_{ratio} is re-calculated for next simulation at 1e5 sec.
3. Perform the simulation at 1e5 sec. using the t_{ratio} calculated at 1e4 sec. In this step the t_{ratio} is re-calculated for next simulation at 1e6 sec.
4. Goto step3 for next time step.

In Fig. 3, a sine wave of -1.8@1 Hz V is applied during the simulation. The black line is an actual transient calculation result with physical NBTI models (depicted for a reference), which is calculated until 1.5e7 sec. of transient time. The colored vertical bars are transient calculation results with the long-term NBTI degradation method. The red, yellow, green, cyan, and blue vertical bars correspond to results at 1e4, 1e5, 1e6, 1e7, and 1e8 sec., respectively. As shown, good agreement is achieved. The effectivity of adjusting the t_{ratio} of long-term degradation method during the simulation is confirmed by comparison with actual simulation (Table 1).

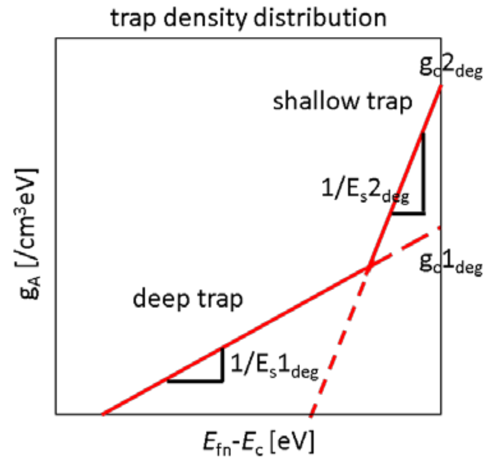

Fig. 4. Schematic of the acceptor-type trap density of states distribution used for this study. g_cs are the density at E_{fn}-E_c=0. The inverses of E_ss are the slopes of the density of states. In this study we consider two independent trap-density distributions: the shallow trap density distribution and the deep trap density distribution.

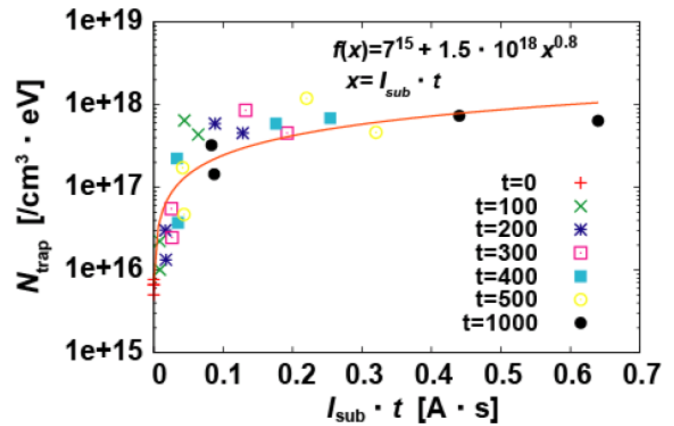

Fig. 5. Observed universal relationship [3] between normalized trap density N_{trap} and substrate current I_{sub} multiplied by stress duration time t, which is independent of stress bias conditions and duration. Thanks to this universal relationship N_{trap} can be written as a function of $I_{\mathrm{sub}} \cdot t$ for accurate modeling of degradation.

2.3 Pysical Model of Hot Carrier Effect in n-MOSFETs

In the n-MOSFETs, hot-channel-carrier trapping is dominant for the degradation [8]. In contrast to p-MOSFETs degradation, n-MOSFETs degradation has not only threshold voltage shift but also obvious degradation of subthreshold slope. Therefore, we have developed a compact model by considering the energy-dependent trap density, which is included in the Poisson equation so that all effects caused by trapped charges are self-consistently calculated with respect to all device characteristics.

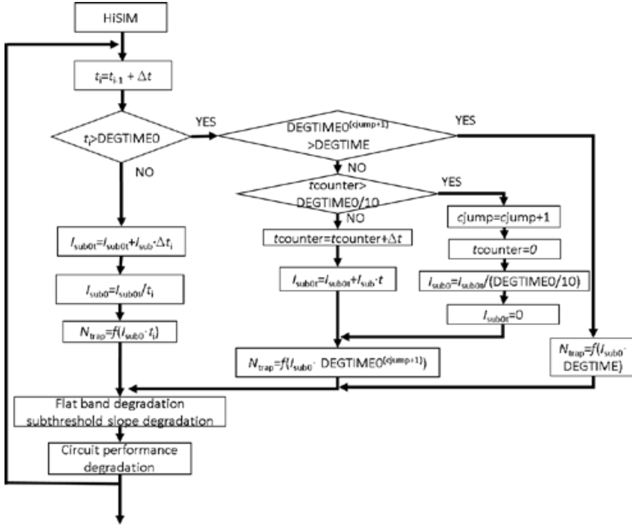

Fig. 6. Flow chart of the hot carrier model implementation into the compact model HiSIM.

The trap density distribution is written by

$$g_{\rm A}(E) = g_{\rm c}\exp(\frac{E-E_{\rm c}}{E_{\rm s}}) \tag{10}$$

where the g_c is the density of states at E_{fn}-E_c=0, and the inverse of E_s is the slope of the density of states. In this study we considered two independent trap-density distributions, the shallow trap density distribution and the deep trap density distribution, as schematically shown in Fig. 4. Since circuit simulations need only node potential, N_{trap_A} is integrated with regard to the energy as a function of E_{fn}- E_c.

$$N_{\rm trap_A} = N_0\exp(\frac{E_{\rm f}-E_{\rm c}}{E_{\rm s}}) \tag{8}$$

with

$$N_0 = g_{\rm cdeg}\cdot E_{\rm sdeg}\frac{\frac{kT}{E_{\rm sdeg}}}{\sin(\frac{kT}{E_{\rm sdeg}})} \tag{9}$$

where g_{cdeg}, E_{sdeg}, k, and T are the density of states at E_{fn}-E_c=0, the slope of the density of states, the Boltzmann constant, temperature, respectively.

The trap density is included in the Poisson equation as follows.

$$\nabla^2\phi = -\frac{q}{\varepsilon_{\rm s}}\left(p-n+N_{\rm D}-N_{\rm A}+N_{\rm trap_D}-N_{\rm trap_A}\right) \tag{10}$$

In this hot carrier model we consider only n-MOSFETs. Hence the donor-like trap density is neglected in this paper and only acceptor-like trap is considered. The Poisson equation is solved iteratively together with the Gauss's law [5].

2.4 Long-Term Hot Carrier Degradation method for n-MOSFETs

We consider two independent trap-density. One is the shallow trap density $N_0 1$ and the other is the deep trap density $N_0 2$.

$$N_{\rm trap_A} = (N_0 1 + N_0 2) \tag{11}$$

In the case of deep trap density, trapped carriers cannot be removed easily. As a result deep trap density is modeled as a function of time.

$$N_0 1 = g_c 1_{\rm deg}(t)\cdot E_s 1_{\rm deg}(t)\frac{\frac{kT}{E_s 1_{\rm deg}(t)}}{\sin(\frac{kT}{E_s 1_{\rm deg}(t)})}. \tag{12}$$

The $g_c 1_{deg}(t)$ and $E_s 1_{deg}(t)$ are able to be described as a power function of I_{sub0t} [3, 9]. Therefore resulting $N_0 1$ is also a function of I_{sub0t} (Fig. 5).

The $g_c 1_{deg}$ and $E_s 1_{deg}$ of (12) are function of I_{sub0t}. The I_{sub0t} is written as

$$I_{\rm sub0}\cdot t = (\frac{I_{\rm sub0t}}{\rm DEGTIME0})\cdot{\rm DEGTIME} \tag{13}$$

where

$$I_{\rm sub0t} = \sum_{i=0}^{i=\frac{\rm DEGTIME0}{t_{\rm i}-t_{\rm i-1}}} I_{\rm sub0}(V_{\rm gs}(t),V_{\rm ds}(t),V_{\rm bs}(t))\cdot(t_{\rm i}-t_{\rm i-1}) \tag{14}$$

The DEGTIME0 and DEGTIME are model parameters. The DEGTIME0 is simulation time for pre calculation to determine I_{sub0t}. (Fig. 6)The I_{sub0t} is recalculated during predictive calculation. The procedure is same as that of t_{ratio} in p-MOSFETs. DEGTIME is degradation time of long-term degradation model such as 10^8 seconds.

In the case of shallow trap density, only pre-existing trap is considered.

$$N_0 2 = g_{\rm c}20\cdot E_{\rm s}2\cdot\frac{\frac{kT}{E_{\rm s}2}}{\sin(\frac{kT}{E_{\rm s}2})} \tag{15}$$

where $g_c 20$ and $E_s 2$ are fresh device values.

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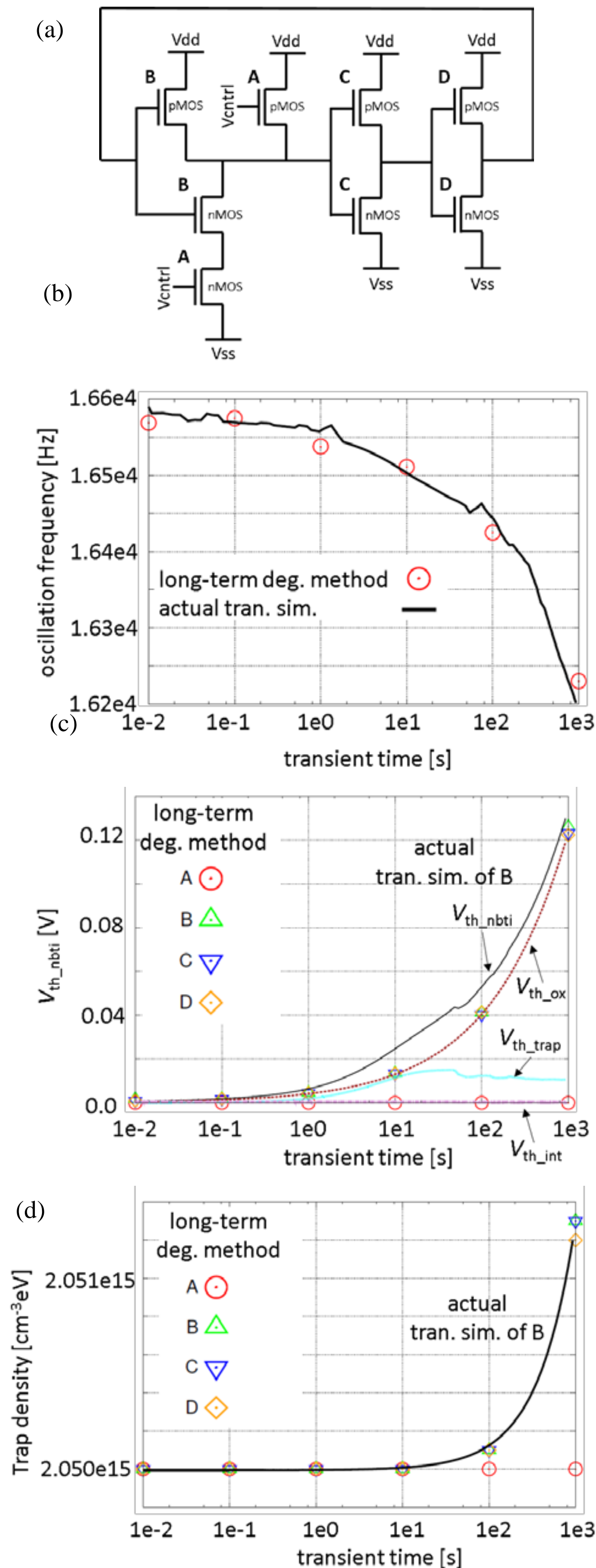

Fig. 7. The comparison of developed methods and actual transient simulation with physical models. (a) Illustration of 3-stage ring oscillator (1 NAND gate, and 2 inverters) used for the comparison. The drain voltage is fixed to 5.0V and model parameters are fixed to L=30 μm, W=2 μm, TOX=30nm, NSUBC=1e16 cm^{-3}. (b)Oscillation frequency degradation. (c) NBTI degradation of p-MOSFETs (d) hot carrier degradaton of n-MOSFETs. In (c) and (d) results of actual transient simulation with physical models of MOSFET B are depicted together.

Table 2. Caculation cost of actual transient simulation with physical models and long-term degradation method.

Degradation time [seconds]	The numberof applied pulse cycle (1Hz)	
	Actual .transient simulation	Long-term deg. method
1e4	1e4	1.1e3
1e5	1e5	1.2e3
1e6	1e6	1.3e3
1e7	1e7	1.4e3
1e8	1e8	1.5e3

2.5 Calculation Cost

An important advantage of the developed method provides simple simulation with minimum simulation time while keeping the physical concept of the degradation. The simulation cost of the developed long-term degradation method is alomost constant. However, the simulation cost of the actual transient simulation with pyhisal models is proportional to the degradation time (Table. 2).

3 RESULTS AND DISCUSSIONS

The developed long-term degradation methods are investigated with the 3-stage ring oscillator circuit(Fig. 7). To confirm the predictivity of the methods, we compared the result of actual transient simulation with the result of long-term degradation method. As shown, good agreement was achieved. Fig. 7 (c) shows that hole-trapping within gate oxide becomes dominant and hole-trapping at gate surface suturates in the long-term use of the MOSFET. This confirms our approximation of (6) and (7). Fig. 7 (b) and (c) show that the circuit A is less degrated and the circuits B, C, D are degrated equally. Each value of MOSFET degradations is calculated.

4 CONCLUSION

The develeped method can be utilized for predicting long-term degradation after long-term use, and has been verified at different long-term stress conditions by comparison with the actual transient simulation using physical models. The developed model is applicable to detect MOSFET degradation critical for a circuit performance at given degradation time and condition.

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