A New Method to Fin-width Line Edge Roughness Effect of FinFET Performance

Yu Zhu[1], Wei Zhao[1], Wenping Wang[1], Wen Wu[1], Zhuqing Feng[2], Caixia Du[1], Jin He[1*], Ping He[3], and Lei Song[4]

[1]*Peking University Shenzhen SOC Key Laboratory, PKU-HKUST Shenzhen-Honkong Institutios, Shenzhen, P. R. China*

[2]*Shenzhen Huayue terascale chip Co., Ltd, Shenzhen, P. R. China*

[3] Shenzhen Emperor Electronic Technology Co., Ltd, Nanshan District, Shenzhen,518108, China

[4] Shenzhen SuperD Co. Ltd, Huaqiaocheng, Nanshan District, Shenzhen 518053, China

Abstract

This paper developed a full three-dimensional (3-D) statistical simulation method to investigate Fin-width Line Edge Roughness (LER) effect on the FinFETs performance. The line edge roughness is introduced by Matlab program, and then the intrinsic parameter fluctuations at fixed LER parameters are studied in carefully designed simulation experiments. The result shows that Fin-width LER causes a dramatic shift and fluctuations in threshold voltage. The simulation results also imply that the velocity saturation effect may come into effect even under low drain voltage due to LER effect.

Keywords: Fin-width, LER, intrinsic parameter fluctuation, FinFET, 3-D numerical simulation.

1 Introduction

In recent years, the mainstream of the CMOS integrated circuits is arriving at 32 nanometer size and beyond. According to the SIA national technology roadmap, devices built at this scale are required to control gate length within approximately 8 nm [1]. However, with the process of lithography and etching, random deviation of the line edge from its ideal pattern, which is called line edge roughness (LER), does not scale with the critical dimension. As a result, intrinsic parameters fluctuations in deep nanometer dimensions caused by LER deserve adequately attentions. Numerous simulations and experiments on the impact of line edge roughness [2-4] have been reported.

FinFET [5] exhibit its strong control of lightly doped channels and good immunity of short channel effect [6]. However, as mentioned above, LER plays a significant role on the transistor operation of nanoscale FinFETs.

A Fourier synthesis technique base on the power spectrum of a Gaussian autocorrelation function was used for LER analysis in planar bulk MOSFETs, and the geometrical variation effects was also systemically studied [4].

In this paper, the LER issue in FinFETs is investigated through a full 3-D statistical simulation approach. The Fin-width roughness is first generated using Matlab program. Then, the variation of on-current Ion, off-current Ioff, voltage threshold VT, transconductance (gm) and subthreshold slope SS are studied in a series of simulation experiments. Finally we analyze the performances of synchronic technological parameter devices under different work conditions.

2 Simulation approach

In this paper, TCAD 3-D numerical simulator is applied for FinFET performance simulation. The structure of double-gate n-channel FinFETs studied here is shown in Fig. 1. The Fin-width roughness modeling approach is based on a sequence of fixed root-mean-square amplitude by Matlab. The parameters used to generate the edges are

root-mean-square amplitude Δ and a cut-off frequency f_H, which reflects the nature of LER in the simulation. Experimentally, Δ is relative to the standard deviation of Fin-width and f_H is determined by suiting a particular Fourier transformation of the fin edges.

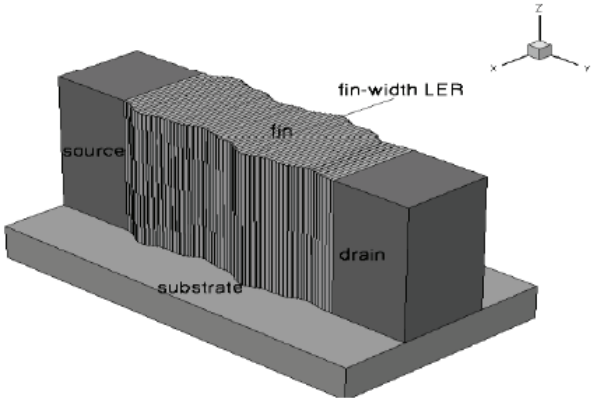

Figure 1: Three-dimension schematic of simulated DG FinFETs with Fin-width LER (Omit the gate).

In the process of Fin-width generation, a premier sequence S is first produced as follow:

S = average-value-of-Fin-width + Δ × randn(1,N)

The Fourier transformation of S is consequently obtained. Then, a frequency, which is higher than cut-off frequency fH as zero in S, is set to fit a specific fin edges for real. After obtaining a new sequence S1 by Fourier transformation, a series of adjustments are applied to equal the average value as well as the standard deviation of S1 to those of the premiere S. To be specific, Fig. 2 set an example of a particular resist-defined fin following that method.

Nominal geometry and correlation parameters are listed in Table 1. To compare with the practical parameters, data used in this work is referred to [4] and [6]. Linearity threshold voltage $V_{T,lin}$ and saturation threshold voltage V_T, sat have been calculated through a constant current method at V_{ds} = 50mV and V_{ds} = 1V, respectively. In addition, I_{on} and I_{off} have been extracted in the saturation regime (V_{ds} = 1V) at V_{gs} = 1V and V_{gs} = 0V, respectively. Subthreshold slope is detected based on device characteristic curve. With respect to the dramatic quantum effects due to the small dimension, we apply the density gradient method. As for most analog applications operate in saturation regime, high drain bias conditions is focused for the mismatch estimation.

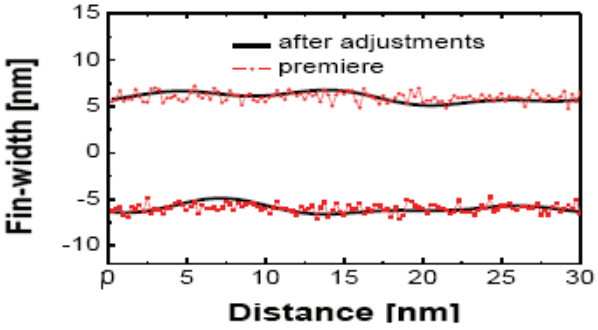

Figure 2: Example of resist defined fin generation. The LER parameters used to define the fin edges are Δ = 0.71nm and fH=6.

Table 1: Simulated double-gate FinFETs' parameters.

Parameter	Value	Parameter	Value
W_{fin}	12nm	length of	10nm
H_{fin}	20nm	channel	p-type 10^{17}
L_{gate}	30nm	S/D doping	n-type 10^{20}
t_{ox}	1.5nm		

3 Simulation results

We assume the root-mean-square amplitude Δ of Fin-width LER 0.71nm, which means variation fluctuations to be 10% of its critical dimension.

Fig. 3 compares the average value of $V_{T,lin}$, $V_{T,sat}$, SS,g_m due to Fin-width LER to the ideal values without LER effects. As shown in Fig. 3 (a), the threshold voltage increases with Fin-width LER due to enhanced short channel effect. Meanwhile, the increase of drain voltage results in severe threshold voltage fluctuations, which is comparable to those resulting from similar 30nm FinFETs in [6]. Observed from Fig. 3 (c), SS almost remains constant with the increased drain voltage. Moreover, SS turns out to be smaller with Fin-width LER, which indicates a better device performance in subthreshold region. This result is owing to the dramatic decrease of I_{off} when considering only Fin-width roughness.

Table 2: Average value of Ion and Ioff on different drain voltages.

Average	V_{ds}=50mV	V_{ds}=1.0V

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I_{on}(A/um)	3.029×10^{-5}	3.117×10^{-5}
I_{off}(A/um)	2.147×10^{-14}	3.491×10^{-14}

From Table 2, it can be seen that drive current I_{on} as well as leakage current I_{off} of V_{ds} = 1V and V_{ds} = 50mV remain surprisingly close to each other. Combining the close result of V_{ds} = 1V and V_{ds} = 50mV in Fig. 3, it seems those two conditions similar to each other. This is because of the velocity saturation effect in the channel. Since the fin is ultra thin, the electric-field intensity is extraordinarily high. Considering this electric-field intensity to be 10^5V/cm, we confirm velocity saturation happening.

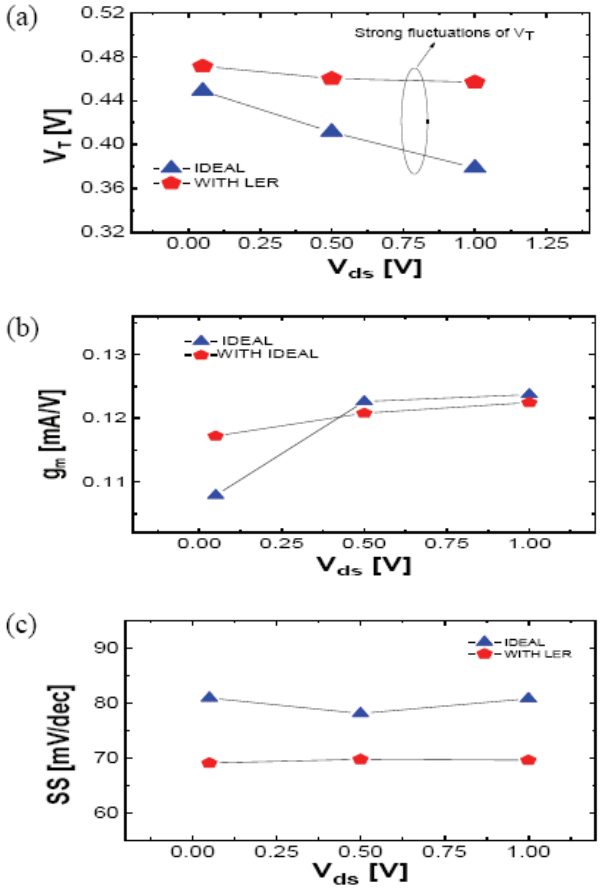

Figure 3: Comparison of ideal FinFETs' performance with those of Fin-width LER on average value of (a) VT,sat, (b) gm, (c) SS. The LER parameters used to define the fin edges are Δ = 0.71nm and fH=6.

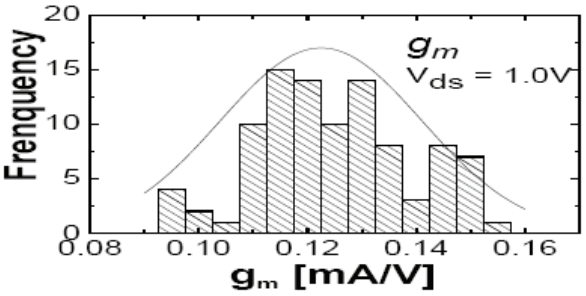

Figure 4: Distributions of the g_m under high drain voltage with Δ = 0.71nm and f_H=6.

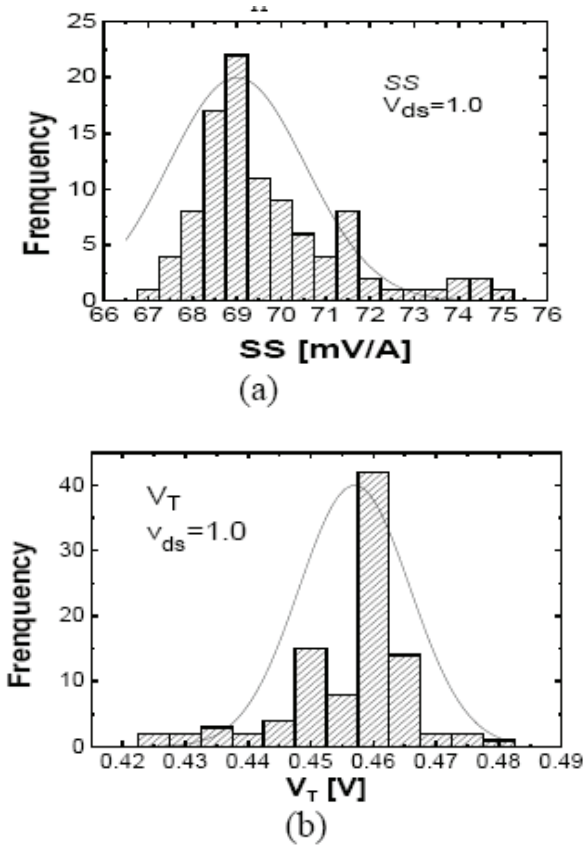

Figure 5: Distributions of the (a) SS and (b) V_T under high drain voltage with Δ = 0.71nm and f_H=6.

Fig. 4 and Fig. 5 shows typical distributions of transconductance, threshold voltage and subthreshold slope in 30 nm FinFETs corresponding to Fin-width LER under high drain voltage (V_{ds} = 1V). These are almost close to a Gaussian distribution. Combining the fact that threshold voltage does show a dramatic shift compared with an ideal on, which is illustrated in Fig. 3(a), it infers that the threshold voltage in saturation region is largely affected by LER. Typical distributions of threshold voltage and

subthreshold slope at low drain voltage (V_{ds} = 50mV) are illustrated in Fig. 6, subthreshold slope and the threshold voltage distribution in subthreshold region shows highly concentration. This difference is owing to two facts. One is that Fin-width LER mainly influences the channel direction. The other is the extreme low voltage of V_{ds}, which is along the channel direction. With respect to those two facts, the device characteristic in subthreshold region is affected relatively to a small extent by Fin-width LER.

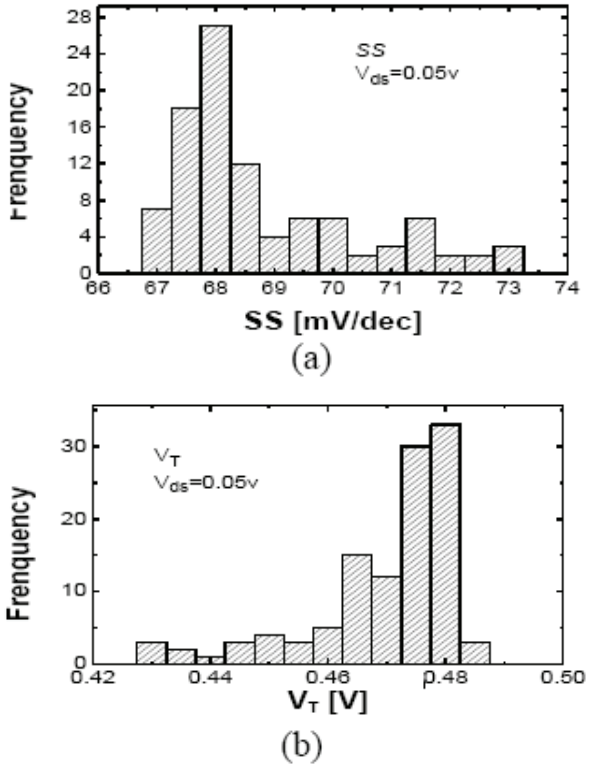

Figure 6: Distributions of the (a) SS and (b) VT under low drain voltage with Δ = 0.71nm and fH=6.

4 Conclusion

The LER effect is investigated using Matlab in this paper for the first time. The Fin-width LER is demonstrated to be a critical source of intrinsic parameter fluctuations in nanometer FinFETs, especially for the threshold voltage. Velocity saturation effect has been proved to occur even under low drain voltage. As under high drain voltage, the distributions of VT, SS and gm match a Gaussian distribution, which indicating the influence of Fin-width LER along the channel direction.

Acknowledgment

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