A Full Differential Charge Pump Based on Symmetrical Complementary
Half-Current Circuit Architecture

Qixiang Huang\(^1\), Wei Zhao\(^1\), Wenping Wang\(^1\), Wen Wu\(^1\), Caixia Du\(^1\), Zhuqing Feng\(^2\), Jin He\(^1\), Ping He\(^3\), and Lei Song\(^4\)

\(^1\) Peking University Shenzhen SOC Key Laboratory, PKU-HKUST Shenzhen-Hongkong Institution, P. R. China
\(^2\) Shenzhen Huayue terascale chip Co., Ltd, Shenzhen, P. R. China
\(^3\) Shenzhen Emperor Electronic Technology Co., Ltd, Nanshan District, Shenzhen, 518108, China
\(^4\) Shenzhen SuperD Co. Ltd, Huaqiaocheng, Nanshan District, Shenzhen 518053, China

Abstract

A full differential charge pump with low current mismatch and deviation is designed in this paper based on the symmetric complementary half-current circuit architecture. It adopts two symmetrical complementary P-N replica circuits with half value of the reference current source to remove the current mismatch and deviation. The charging and discharging current are matched very well over a wide output range. The maximum output current mismatch and deviation of the proposed charge pump are 0.78% and 0.97% over the output voltage range from 0.2V to 1.5V, respectively. The good current matching characteristics and low deviation effectively reduce the reference spur of charge pump phase locked loops. The proposed charge pump is implemented in 0.18\(\mu\)m CMOS technology with 1.8V supply.

Keywords: Charge pump; differential charge pump; mismatch; deviation; symmetrical complementary replica circuits;

1 Introduction

Phase-locked loops (PLLs) are very popular in the modern mixed signal systems, such as distribution networks and frequency synthesizers [1-2]. Among the different PLL topologies, charge pump (CP) PLL is preferred because of the good phase-lock performance. Fig. 1 shows the key modules of CP PLLs. Traditional charge pumps consist of two switched current sources driving the loop filter and make use of MOS switches. However, the two sources have mismatch which is induced by channel-length modulation effect [3], nonideal switch effects [4] and process variation. What’s more, the output current deviation occurs when the output voltage varies. Both the current mismatch and deviation introduce phase noise and spurious tones in the VCO output, and then the loop band width of the PLL. A cascode structure is introduced to enhance the output impedance of the charge pump so as to obtain good current matching characteristics in [5]. Opamp is included in [6-7] to remove the current mismatch, but the output current deviation and difference between the replica and the main current source still exists. Compensation circuits is added to suppress the current deviation in [8], however, due to the bias circuit the PMOS-NMOS (P-N) current difference is not completely compensated and the inherent coefficient difference of P-N channel length modulation effect is remained.

![Figure 1: Block diagram of charge pump PLL](image)

In this paper, a fully differential charge pump circuit with low current mismatch and deviation is proposed. It adopts two symmetrical complementary P-N replica circuits with half value of the reference current source to remove the current mismatch and deviation. Rail to rail amplifier and common mode feed back circuit (CMFB) is also included to ensure large voltage swing.

2 Current mismatch and deviation of charge pumps

The conceptual diagram of a conventional fully differential charge pump is shown in Fig. 2. When the output voltage varies the current match characteristics and deviation of the charging and discharging current becomes worse due to the channel length modulation effect.

We defined that \(\Delta V > 0\) is the voltage variation. Then the output current deviations due to channel length modulation effect by \(\Delta V\) at both sides are

\[
\Delta I_{\text{up}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda_p (\Delta V) = k_p \lambda_p (\Delta V)
\]

(1)

\[
\Delta I_{\text{down}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda_n (\Delta V) = k_n \lambda_n (\Delta V)
\]

(2)
Where \( \mu \) and \( \lambda \) are the mobility and channel length modulation coefficient of PMOS or NMOS.

The output deviation at the differential side is

\[
\Delta I_{up} = k_p \lambda_p (\Delta V)
\]

\[
\Delta I_{dn} = k_n \lambda_n (-\Delta V)
\]

Eqns (1)-(4) indicate that the higher \( \Delta V \) varies, the larger \( \Delta I \) becomes. The output voltage variation affects the charge pump current mismatch and deviation significantly.

Figure 2: Conceptual diagram of conventional fully differential charge pump

### 3 Proposed charge pump

To overcome the drawbacks analyzed above, a fully differential charge pump is proposed as shown in Fig. 3. The op1 and op2 branches are symmetrical complementary replica circuits each with half current value of the reference current source to ensure high current matching characteristics and low output current deviation due to the channel length modulation effect. The op3 eliminate the switches charge sharing effect and stabilize the circuits. The CMFB block [7] in Fig. 4 is designed as a rail-to-rail structure by three rail-to-rail opamps [9] shown in Fig. 5 so as to get large voltage swing of the charge pump. The opamps are designed to have enough DC gain to ensure the outputs of the charge pump to be equal. From the proposed circuits low current mismatch and deviation are achieved.

The difference among P-N current is converted to NMOS-NMOS (N-N) current. Because of the symmetry of the circuits, the op2 replica circuit has the same specific functions as op1, but the diversity is that the difference between P-N current is converted to PMOS-PMOS (P-P) current.

It’s obviously that the output charging and discharging current are both sum of PMOS and NMOS current, which are matched well.

The current flows through the op1 and op2 replica branch are:

\[
I_{up} = \frac{1}{2} I_{ref} = \frac{1}{2} \times \frac{1}{2} \mu_n C_m W (V_{ref} - V_{in})^2 \left(1 + \frac{g_{m}}{g_{ds}} V_{ds} + \left(V_{gs} - V_{th}\right)\right) = \frac{1}{2} k_n (1 + \lambda_n V_{in})
\]

\[
I_{dn} = \frac{1}{2} I_{ref} = \frac{1}{2} \times \frac{1}{2} \mu_p C_m W (V_{ref} - V_{in})^2 \left(1 + \frac{g_{m}}{g_{ds}} V_{ds} + \left(V_{gs} - V_{th}\right)\right) = \frac{1}{2} k_p (1 + \lambda_p V_{in})
\]

The output current deviations of the charge pump are

\[
\Delta I_{up} = \Delta I_{dn} = \Delta I_{ph1} + \Delta I_{ph2} = \Delta I_{p1} + \Delta I_{p2} = \frac{1}{2} (k_p \lambda_p \Delta V - k_n \lambda_n \Delta V)
\]

Where \( \Delta V > 0 \) is the voltage variation.

The output current deviations at the differential side are

\[
\Delta I_{up} = \Delta I_{dn} = \frac{1}{2} (k_p \lambda_p \Delta V - k_n \lambda_n \Delta V)
\]

Eqns (7)-(8) show clearly that the output current deviations of the charge pump are greatly suppressed by the symmetrical complementary half-current circuits.

Figure 3:  Proposed fully differential charge pump

Figure 4: Rail-to-Rail CMFB
4 Simulation Results

The proposed charge pump is implemented in 0.18μm CMOS technology, and its simulation results are shown in Fig. 6. The charging and discharging current are matched very well. The current deviation is very low too. The maximum output current mismatch of the proposed charge pump is 0.78% over the output voltage range from 0.2V to 1.5V. Even for a wider output voltage range from 0.1V to 1.7V the maximum output current mismatch is less than 1.1%. The maximum output current deviation is only 0.97% when the corresponding output voltage ranges from 0.2V to 1.5V which covers more than 72% of the power supply. The maximum current deviation of the charge pump in [8] is 1.7% when the output voltage covers only 67% of the power supply. Both the cascade structure charge pump and the charge pump with only P or N replica circuits which have the same transistor size used in this paper are also designed for comparison. Both the current mismatch and deviation in paper are much less than that of the aforementioned three charge pumps topologies.

5 Conclusion

Based on the analysis of current mismatch and deviation of charge pumps, a fully differential charge pump circuit with low current mismatch and deviation is proposed in this paper. It adopts two symmetrical complementary P-N replica circuits with half value of the reference current source to remove the current mismatch and deviation. The simulation results show good current mismatch characteristics and the low deviations are achieved by the proposed structure. Both the current mismatch and deviation are less than 1% over the output voltage range for 0.2V to 1.5V which reduce the phase noise and spurious tones in the PPLs. The proposed charge pump is very appropriate for high performance PLLs for the low current mismatch and deviation.

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