

# Fabrication of Capacitive Micromachined Ultrasonic Transducer Arrays Using Glass Reflow Process and Anodic Bonding

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## ABSTRACT

This paper presents a process for the fabrication of vacuum-sealed capacitive micromachined ultrasonic transducer (CMUT) arrays using glass reflow and anodic bonding techniques. The silicon through-wafer interconnects have been investigated by glass reflow process. Then, the patterned silicon-glass reflow wafer is anodically bonded to an SOI (silicon-on-insulator) wafer for the fabrication of CMUT devices. The CMUT 5 x 5 array has been successfully fabricated. The resonant frequency of the CMUT array with a one-cell radius of 100  $\mu$ m and sensing gap of 3.2  $\mu$ m (distance between top and bottom electrodes) is observed at 2.83 MHz. The  $Q$  factor is approximately 1300 at vacuum chamber pressure of 0.01 Pa.

**Keywords:** Capacitive micromachined ultrasonic transducer, glass reflow process, anodic bonding, medical imaging, non-destructive measurement, chemical sensing.

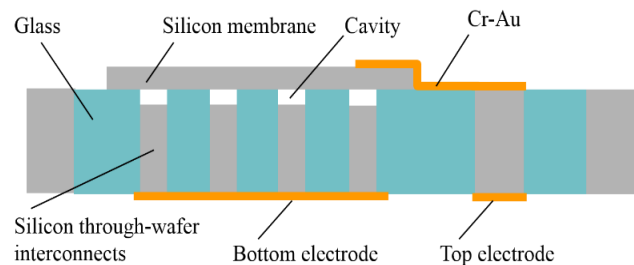
## 1 INTRODUCTION

CMUTs have wide-range promising applications for making ultrasound transducer such as medical imaging [1], non-destructive measurement [2], and chemical sensing [3]. Generally, CMUTs were fabricated using a sacrificial release method [4], in which the sensing gaps are formed by the selective removal of the sacrificial layer using an appropriate etchant. However, this method requires well control over the uniformity, thickness and mechanical properties of deposited films that may effects on CMUT parameters such as sensing gap height, the membrane thickness, and the residual stress. Moreover, the removal of the sacrificial layer induces the stiction of the top and bottom electrodes, especially when the sensing gap is small. To improve the process controllability and repeatability limiting the sacrificial release process, and also to reduce the process complexity, a fusion bonding technique is investigated [5]. Nevertheless, this process requires the very flat surfaces and high temperature process (over 1100°C). Additionally, the minimum sensing gap height is limited by the thickness of the initial oxide layer. As a result, this structure is traded-off by reduced breakdown voltage and increased parasitic capacitance in the area between the cells of the CMUT array. The recent process using SOI wafer and anodic bonding to Pyrex glass has been reported in [6]. A

single-cell as well as 1D and 2D arrays with isolation-trenches has been successfully demonstrated, but its cavity is not vacuum-sealed and co-CMUT devices and integrated circuits are difficult due to without through-wafer interconnects.

In this work, CMUT arrays have been fabricated by using glass reflow [7] and anodic bonding techniques. The silicon through-glass wafer interconnects have been done by glass reflow. The anodic bonding between silicon-glass reflow wafer and SOI wafer is performed. Then, the handle and buried oxide layers are removed to release CMUT membranes. Finally, the electrical connections and pads are formed.

## 2 DEVICE CONCEPT



**Figure 1.** Device Structure.

A schematic diagram of the CMUT array is shown in Fig. 1. It consists of silicon through-wafer interconnects (bottom electrode) and thin movable membranes (top electrode) suspended over a vacuum gap. The CMUT cells are isolated by the Tempax glass and Cr-Au layers are used for electrical connections and pads. The summarized parameters of CMUT array are shown in Table 1.

The CMUT works as a capacitor cell. When a DC voltage is applied to two electrodes, the silicon membranes is attracted toward the bottom electrode by the electrostatic force. If the AC voltage is superimposed over the DC voltage, the silicon membrane will vibrate in the response to the RF (radio frequency) signal and generates ultrasound. It acts as a transmitter in this case. Otherwise, if the membrane is subjected to ultrasound pressure, the electrical current is created due to the capacitance changes, in this mode it works as a receiver.

### 3 EXPERIMENTS

#### 3.1 Fabrication process

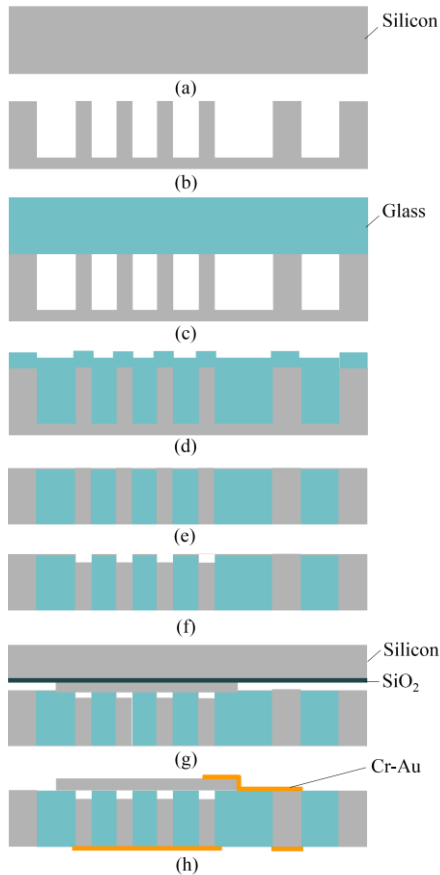


Figure 2. Fabrication process. (a) Silicon wafer. (b) Photolithography and deep RIE. (c) Anodic bonding in vacuum chamber. (d) Glass reflow process. (e) Lapping and polishing. (f) Photolithography and deep RIE. (g) Anodic bonding in vacuum chamber. (h) Silicon and SiO<sub>2</sub> removal, electrical connection and contact pads.

The fabrication process is given in Fig. 2. It starts with a 300  $\mu\text{m}$ -thick silicon wafer (Fig. 2 (a)). The silicon structures (silicon mold) are formed by deep RIE based on Bosch process using SF<sub>6</sub> and C<sub>4</sub>F<sub>8</sub> with an SiO<sub>2</sub> mask (Fig. 2 (b)). The silicon structure with an etching depth of 230  $\mu\text{m}$  has been achieved.

Anodic bonding of the silicon wafer and the Tempax glass is carried out in a high vacuum chamber with an applied voltage of 800 V at 400°C for 15 min (Fig. 2 (c)). The vacuum applies a force on the Tempax glass within the vacuum cavities, pulling it into the cavities during the high temperature glass reflow process. The glass reflow process is performed in an atmospheric furnace with a high temperature of 750°C for 10 hours (Fig. 2 (d)). Both of the Tempax glass and the silicon sides of the wafer are lapped and polished as shown in Figs. 2 (e). The complete filling process into cavities has been achieved as shown in Fig. 3.

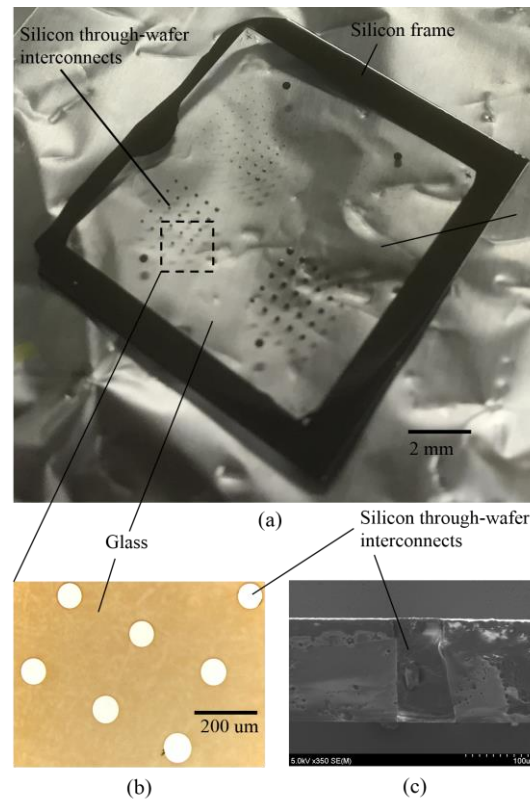


Figure 3. (a) 2 x 2 cm<sup>2</sup> silicon-in-glass wafer. (b) Top view. (c) Cross section view.

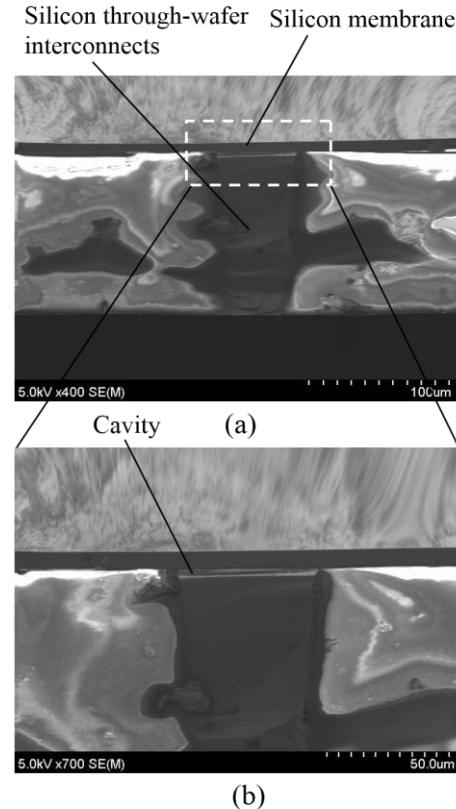


Figure 4. (a) Vacuum cavity. (b) Close-up image.

Thus, the silicon through-wafer interconnects have been successfully fabricated. Next, silicon through-wafer interconnects have been etched in the depth of about 3  $\mu\text{m}$  for the sensing gaps (Fig. 2 (e)). Anodic bonding of reflow wafer and SOI wafer is performed in vacuum chamber at same condition as above (Fig. 2 (g)). The handle and buried oxide layers are removed by deep RIE and RIE methods, respectively. The vacuum-sealed cavity is successfully demonstrated as shown in Fig. 4. Finally, the electrical connections and pads are formed by using stencil masks and a sputtering technique (Fig. 2 (h)).

### 3.2 Measurement setup

Measurement setup for the resonant characterization of CMUTs is shown in Fig. 5. A network analyzer (Anritsu MS4630B) in range from 10 Hz to 300 MHz has been employed for this evaluation. A DC voltage is applied to the bottom electrode of CMUTs against the grounded top electrode through 100 k $\Omega$  resistor, which decoupled from the RF output of the network analyzer using 100 nF. The output of device is obtained by capacitive detection between the top and the bottom electrodes. Small changes in the capacitive gap generate a voltage on the RF input of the network analyzer. The CMUTs is placed inside a vacuum chamber with coaxial feed-through.

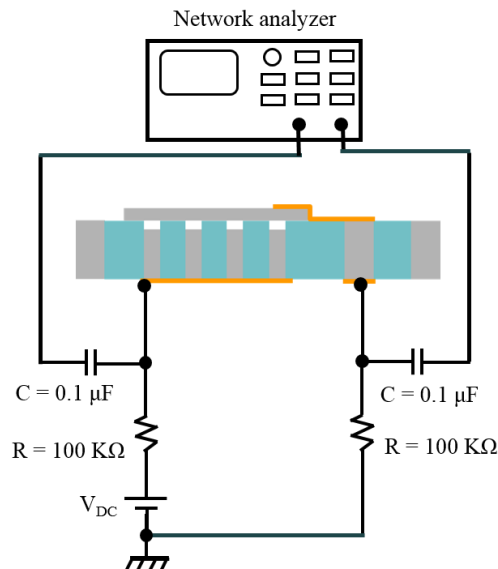


Figure 5. Measurement setup.

### 3.3 Measurement results

The resonant characteristic of the fabricated device is evaluated, as the specification is summarized in Table 1. Transmission  $S_{21}$  is indicated for CMUT array in Fig. 6. A resonant peak, which is observed under  $V_{DC}$  of 120 V,  $V_{AC}$  of 0 dBm, is found at 2.83 MHz with the  $Q$  factor of approximately 1300 in vacuum environment of 0.01 Pa. Additionally, the simulation result (FEM – finite element

method) is in good agreement with experiment result as shown in Fig. 6.

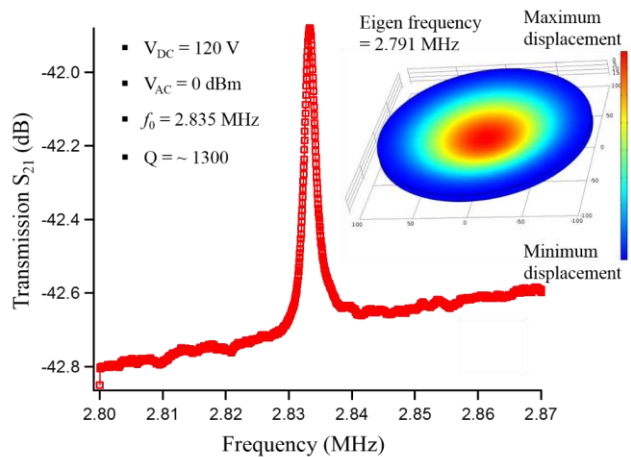


Figure 6. Simulation and measurement results.

Table 1. Summarized parameters of CMUT array.

<b>Parameters:</b>	
Membrane size (circular)	100 $\mu\text{m}$
Membrane thickness	7 $\mu\text{m}$
Array	5 x 5
Sensing gap	3.2 $\mu\text{m}$
<b>Applied conditions:</b>	
$V_{dc}$	120 V
$V_{ac}$	0 dBm
Pressure level of chamber	0.01 Pa
<b>Resonant frequency (Calculation)</b>	
Resonant frequency	2.88 MHz
<b>FEM simulation:</b>	
Resonant frequency	2.79 MHz
<b>Measurement results:</b>	
Resonant frequency	2.83 MHz
$Q$ factor	1300

### ACKNOWLEDGMENTS

Part of this work was performed in the Micro/Nanomachining Research Education Center (MNC) of Tohoku University. This work was supported by Special Coordination Funds for Promoting Science and Technology, Formation of Innovation Center for Fusion of Advanced Technologies

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