Simulation of Lags and Current Collapse in Field-Plate AlGaN/GaN HEMTs with Different Types of Buffer Layers

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ABSTRACT

We make 2-D transient simulations of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer, where a deep acceptor above the midgap is considered. It is studied how the deep acceptor and the field plate affect lag phenomena and current collapse. It is shown that the drain lag and current collapse could be reduced by introducing a field plate, as in a case with a deep acceptor compensated by a deep donor in the buffer layer. This reduction occurs because electron trapping by the deep acceptors is weakened by the field plate. The dependence on the field-plate length and the insulator thickness under the field plate is also studied, showing that the rates of lags and current collapse are quantitatively similar between the two cases with different types of buffer layers when the deep-acceptor density in the buffer layer is the same.

Keywords: GaN, HEMT, deep acceptor, current collapse, field plate

1 INTRODUCTION

In AlGaN/GaN HEMTs, slow current transients are often observed even if the gate voltage or the drain voltage is changed abruptly [1]. This is called gate lag or drain lag, and is problematic for circuit applications. The slow transients mean that dc *I-V* curves and RF *I-V* curves become quite different, resulting in lower RF power available than that expected from the dc operation [2]. This is called current collapse. These are serious problems, and many experimental works are reported [1-5], and several theoretical works are made [5-10]. In previous theoretical works, the semi-insulating buffer is treated as undoped, and a deep donor and a deep acceptor are considered in it [6, 7], and the effects of a field plate on buffer-related lags and current collapse are also studied [9, 10]. Recently, a Fe-doped semi-insulating buffer layer is often adopted, and Fe acts as a deep acceptor [11]. Therefore, in this work, we have made simulations of field-plate AlGaN/GaN HEMTs with a buffer layer including only deep acceptors, and found that the buffer-related lags and current collapse are quite similar between the two cases.

2 PHYSICAL MODEL

Figure 1 shows a modeled device structure analyzed in this study. The gate length L_G and the field-plate length L_{FP} are typically set to 0.3 μm and 1μm, respectively. As a buffer layer, we consider a Fe-doped semi-insulating buffer layer. The Fe-level (E_{DA}) is set to 0.5 eV below the bottom of conduction band, and it is assumed to act as a deep acceptor. Here the deep acceptor acts as an electron trap. The deep-acceptor density N_{DA} is set to 10^{17} cm^{-3} here.

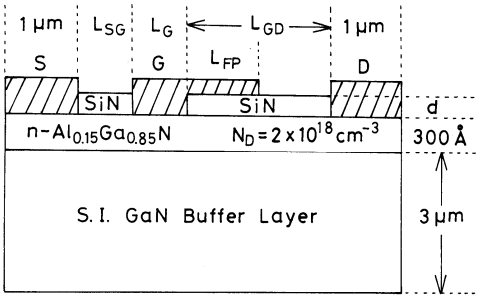

Figure 1: Device structures simulated in this study.

Basic equations to be solved are Poisson's equation including ionized deep-acceptor terms, continuity equations for electrons and holes which include carrier loss rates via the deep acceptor and rate equations for the deep acceptor [7, 12-16].

1) Poisson's equation

$$\nabla \bullet (\varepsilon \nabla \psi) = -q(p - n + N_D - N_{DA}^-) \quad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - R_{n,DA} \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - R_{p,DA} \quad (3)$$

where

$$R_{n,DA} = C_{n,DA}(N_{DA} - N_{DA}^-)n - e_{n,DA}N_{DA}^- \quad (4)$$

$$R_{p,DA} = C_{p,DA}N_{DA}^- p - e_{p,DA}(N_{DA} - N_{DA}^-) \quad (5)$$

3) Rate equation for the deep acceptor

$$\frac{\partial}{\partial t}N_{DA}^- = R_{n,DA} - R_{p,DA} \quad (6)$$

where N_{DA}^- represents the ionized deep-acceptor density. $C_{n,DA}$ and $C_{p,DA}$ are the electron and hole capture coefficients of the deep acceptor, respectively, $e_{n,DA}$ and $e_{p,DA}$ are the electron and hole emission rates of the deep acceptor, respectively. These are given as functions of the

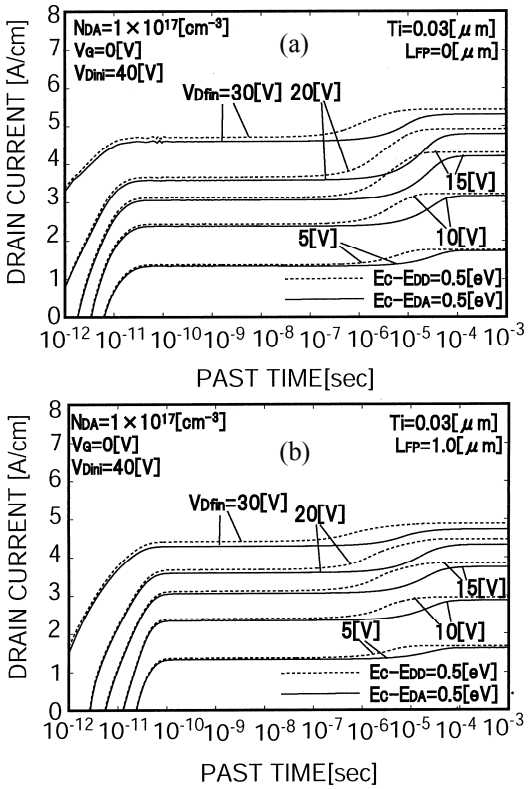

Figure 2: Calculated drain-current responses of AlGaN/GaN HEMTs when V_D is changed abruptly from 40 V to V_{Dfin}, while V_G is kept constant at 0 V. d = 0.03 μm. $N_{DA} = 10^{17}$ cm^{-3}. (a) Without field plate, (b) with field plate (L_{FP} = 1μm).

deep acceptor's energy level and the capture cross sections.

These basic equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

3 DRAIN LAG

Figure 2 shows calculated drain-current responses of AlGaN/GaN HEMTs when V_D is lowered abruptly from 40 V to V_{Dfin}, where V_G is kept constant at 0 V. The dashed lines show the case with an undoped buffer layer with N_{DA} = 10^{17} cm^{-3} and E_C - E_{DD} = 0.5 eV, where E_{DD} is the deep donor's energy level. Figure 2(a) shows the case without a field plate (L_{FP} = 0) and Fig.2(b) shows the case with a field plate (L_{FP} = 1 μm). Here the thickness of SiN passivation layer d is 0.03 μm. In both cases, the drain currents remain at low values for some periods and begin to increase slowly, showing drain-lag behavior. It is understood that the drain currents begin to increase when the deep acceptors in the buffer layer begin to emit electrons, because the state of higher V_D is a state where more electrons are captured by the deep acceptors. It is seen that the change of drain current is smaller for the case with a field plate, indicating that the drain lag is smaller for the field-plate structure.

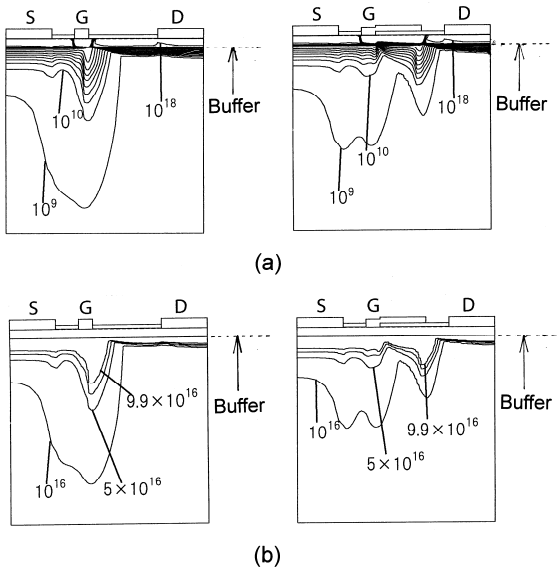

Figure 3: (a) Electron density profiles and (b) ionized deep-acceptor density N_{DA}^- profiles at V_G = 0 V and V_D = 40 V. d = 0.03 μm. $N_{DA} = 10^{17}$ cm^{-3} and $E_C - E_{DA}$ = 0.5 eV. The left is for the case without a field plate, and the right is for the field-plate structure (L_{FP} = 1μm).

Comparing the solid and dashed lines, the response is a little faster for the case with the undoped buffer (and the current change is almost the same), but the reason of the faster response is not clear now. We will discuss below why the reduction in drain lag due to the field plate arises.

Figure 3 shows (a) electron density profiles and (b) ionized deep-acceptor density N_{DA}^- profiles at V_G = 0 V and V_D = 40 V. The left shows the case without a field plate, and the right shows the case of field-plate structure. In Fig.3(a), it is seen that without a field plate, electrons are injected deeper into the buffer layer under the gate, particularly under the drain edge of the gate region. These electrons are captured by the deep acceptors, and hence N_{DA}^- increases there as seen in Fig.3(b). As mentioned before, when V_D is lowered abruptly, the drain current remains at a low value for some periods and begins to increase slowly as the deep acceptors begin to emit electrons (and N_{DA}^- decreases), showing drain lag. In the case of field-plate structure, as seen in Fig.3(a), electrons are injected into the buffer layer under the drain edge of field plate as well as under the gate. But the injection depth is not so deep as compared to the case without a field plate. This is because the electric field at the drain edge of the gate becomes weaker by introducing a field plate. Hence, the change of N_{DA}^- by capturing electrons is smaller for the field-plate structure as seen in Fig.3(b). Therefore, the drain lag becomes smaller for the structure with a field plate.

4 CURRENT COLLAPSE

Next, we have calculated a case when V_G is also changed from an off point. V_G is changed from threshold

voltage V_{th} to 0 V, and V_D is changed from 40 V to V_{Don} (on-state drain voltage). The characteristics become similar to those in Fig.2, although some transients arise when only V_G is changed (gate lag). From these turn-on characteristics, we obtain a quasi-pulsed *I-V* curve.

In Fig.4, we plot by (□) the drain current at $t = 10^{-9}$ s after V_G is switched on. Figure 4(a) shows the case without a field plate, and Fig.4(b) shows the case of field-plate structure (L_{FP} = 1 μm). These curves are regarded as quasi-pulsed *I-V* curves with pulse width of 10^{-9} s. They stay rather lower than the steady-state *I-V* curves (solid lines), indicating gate lag and current collapse behavior. Note that the gate lag is rather large [17]. In Fig.4, we also plot another pulsed *I-V* curve (○), which is obtained from Fig.2 (where only V_D is changed), indicating drain-lag behavior. From Fig.4, we can definitely say that the lag phenomena (drain lag, gate lag) and current collapse become smaller for the structure with a field plate.

5 FIELD-PLATE PARAMETER DEPENDENCE

We have next studied dependence of lag phenomena and current collapse on the field-plate length L_{FP} and the SiN thickness *d*.

Figure 5 shows drain-current reduction rate $\Delta I_D/I_D$ (ΔI_D : current reduction, I_D : steady-state current) due to current collapse, drain lag or gate lag as a function of L_{FP}. As L_{FP} becomes longer, the current collapse and the lag phenomena becomes weaker. This is because the electric field at the drain edge of the gate is more reduced and the electron injection into the buffer layer becomes weaker. It is also seen that the characteristics are quite similar between the two cases with different types of buffer layers. Note that the acceptor density is the same for the two cases (N_{DA} = 10^{17} cm^{-3}).

Figure 6 shows drain-current reduction rate $\Delta I_D/I_D$ due to current collapse, drain lag or gate lag, with *d* as a parameter. When *d* is thick, the current collapse and lag phenomena are relatively large because the field plate does not almost affect the characteristics. As *d* becomes thinner, the current collapse and lag phenomena become smaller. This is because the buffer-trapping effects are reduced as described before. However, the rates of current collapse and drain lag increase for very thin *d*. This is understood that for very thin *d*, the electric field at the drain edge of the field plate becomes very strong, and electrons are injected deeper into the buffer layer under the field-plate region, contributing to the current collapse and drain lag. From this figure, we can say that there is an optimum thickness of SiN to minimize the buffer-related current collapse and drain lag in AlGaN/GaN HEMTs. As in Fig.5, It is also seen that the characteristics are quite similar between the two cases with different types of buffer layers. Note that the acceptor density is the same for the two cases (N_{DA} = 10^{17} cm^{-3}).

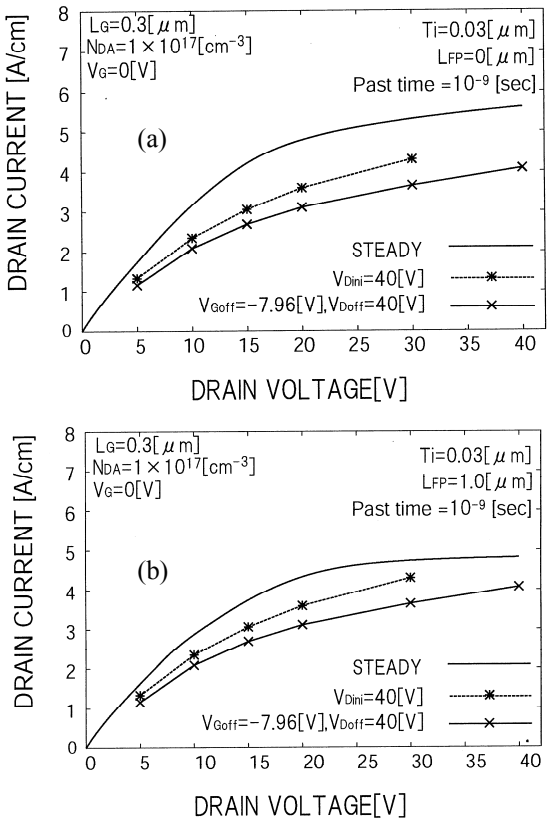

Figure 4: Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (x, ∗) of AlGaN/GaN HEMTs. (a) Without a field plate, (b) with 1 μm-length field plate. (∗): Only V_D is changed from 40V ($t = 10^{-9}$ s), (x): V_D is lowered from 40 V and V_G is changed from V_{th} to 0 V (t = 10^{-9} s).

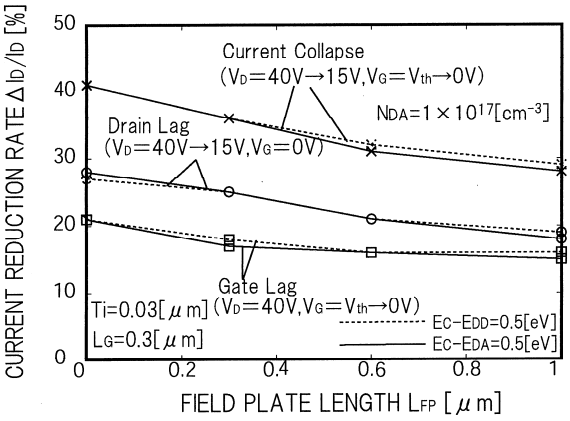

Figure 5: Current reduction rate $\Delta I_D/I_D$ due to current collapse, drain lag or gate lag for AlGaN/GaN HEMTs, with the field-plate length L_{FP} as a parameter.

6 CONCLUSION

Two-dimensional transient simulations of field-plate AlGaN/GaN HEMTs with a semi-insulating buffer layer have been performed, where a deep acceptor above the

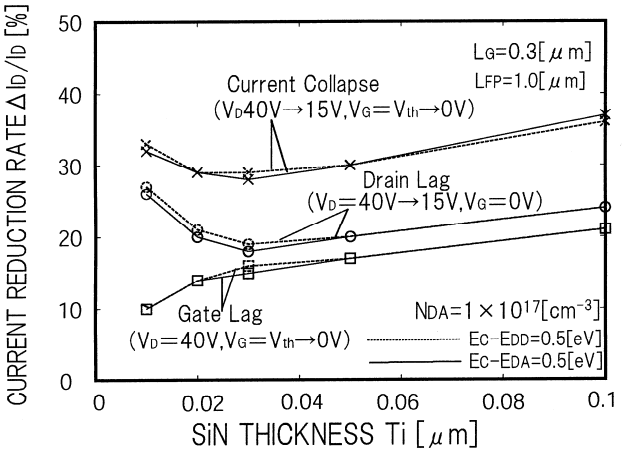

Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current collapse, drain lag or gate lag for AlGaN/GaN HEMTs, with SiN thickness d as a parameter. $N_{DA} = 10^{17}$ cm^{-3}.

midgap is considered. The results are compared with the case where a deep acceptor located below the midgap is compensated by a deep donor located above the midgap. It has been shown that the drain lag and current collapse could be reduced by introducing a field plate, as in the case with the deep acceptor compensated by the deep donor. This reduction occurs because electron trapping by the deep acceptors is weakened by the field plate because the electric fiield at the drain edge of the gate is reduced. The dependence on the field-plate length and the insulator thickness under the field plate is also studied, showing that the rates of lags and current collapse are quantitatively similar between the two cases with different types of buffer layers when the deep-acceptor density in the buffer layer is the same.

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