Simulation of Current Slump Removal in Field-Plate GaAs MESFETs with a Thin Passivation Layer

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ABSTRACT

Two-dimensional transient analysis of field-plate GaAs MESFETs is performed by considering surface states in the region from the gate toward the drain. The field-plate length L_{FP} and the thickness of SiO_2 passivation layer T_i are varied as parameters. It is shown that the drain lag is not removed when T_i is thick even if L_{FP} is longer than the length of surface-state region L_S. But when T_i becomes thinner than 0.02 μm, the drain lag, gate lag and current slump are completely removed by introducing a field plate longer than L_S because the surface-state effects may be masked. By carefully examining the L_{FP} dependence of lags and current collapse for T_i = 0.02 μm, they are found to be completely removed even if L_{FP} is alittle shorter than L_S.

Keywords: GaAs FET, current slump, surface state, drain lag, gate lag

1 INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [1,2]. This is called drain lag or gate lag, and undesirable for circuit applications. Slow transients indicate that dc and RF current-voltage (*I-V*) curves become quite different, resulting in lower RF power available than that expected from dc operation [3]. This is called current slump. These phenomena occur due to surface states and/or bulk traps [1-5]. Experimentally, the introduction of field plate like Fig.1 is shown to reduce the lags and current slump [3,6,7]. However, few simulation studies on field-plate structures have been made, although GaN-based FETs with bulk traps or surface states are studied [8,9]. In previous works [10,11], we made two-dimensional analysis of field-plate GaAs MESFETs including surface states, and showed that surface-related lags and current slump could be reduced by introducing a field plate and that in some cases, they were completely removed. In this work, we have further studied the field-plate effects and studied the condition when the lags and current collapse are completely removed.

2 PHYSICAL MODELS

Figure 1 shows a device structure analyzed in this study.

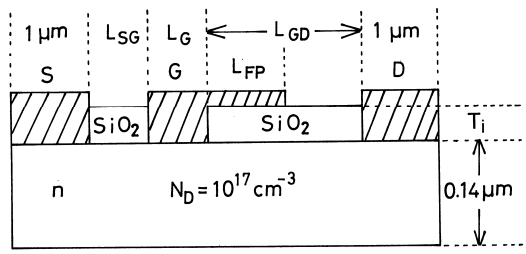

Figure 1: Device structure analyzed in this study.

The gate length L_G is typically set to 0.3 μm. The gate electrode extends on to SiO_2 passivation layer. This is called a field plate. The field-plate length L_{FP} is varied as a parameter. The thickness of SiO_2 layer T_i is also varied. Relatively high densities of surface states are considered only at the drain edge of the gate region. This situation can occur after the device has been stressed or due to device degradation. Here the length of surface-state region L_S is set to 0.4 μm from the gate edge toward the drain. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities (N_{SD}, N_{DA}) are typically set to $6x10^{19}$ cm^{-3} ($3x10^{12}$ cm^{-2}). As for their energy levels, the following case based on experiments is considered as in a previous work [10,11]: E_{SD} = 0.87 eV, E_{SA} = 0.7 eV, where E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. In this case, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap.

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels [12-15]. These are expressed as follows.

1) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D + N_{Di} + N_{SD}^{+} - N_{SA}^{-}) \qquad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - (R_{n,\mathrm{SD}} + R_{n,\mathrm{SA}}) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - (R_{p,\mathrm{SD}} + R_{p,\mathrm{SA}}) \quad (3)$$

where

$$R_{n,\mathrm{SD}} = C_{n,\mathrm{SD}} N_{\mathrm{SD}}^{+} n - e_{n,\mathrm{SD}}(N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) \quad (4)$$

$$R_{n,\mathrm{SA}} = C_{n,\mathrm{SA}}(N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) n - e_{n,\mathrm{SA}} N_{\mathrm{SA}}^{-} \quad (5)$$

$$R_{p,\mathrm{SD}} = C_{p,\mathrm{SD}}(N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) p - e_{p,\mathrm{SD}} N_{\mathrm{SD}}^{+} \quad (6)$$

$$R_{p,\mathrm{SA}} = C_{p,\mathrm{SA}} N_{\mathrm{SA}}^{-} p - e_{p,\mathrm{SA}}(N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) \quad (7)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) = R_{n,\mathrm{SD}} - R_{p,\mathrm{SD}} \quad (8)$$

$$\frac{\partial}{\partial t} N_{\mathrm{SA}}^{-} = R_{n,\mathrm{SA}} - R_{p,\mathrm{SA}} \quad (9)$$

where N_{SD}^{+} and N_{SA}^{-} are ionized densities of surface deep donors and surface deep acceptors, respectively. C_n and C_p are electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are electron and hole emission rates of the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level.

These equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_{D} and/or the gate voltage V_{G} are changed abruptly.

3 SLOW CURRENT TRANSIENTS (DRAIN LAG)

Figure 2 shows calculated drain-current responses of GaAs MESFETs when V_{D} is lowered abruptly from 10 V to V_{Dfin}, where V_{G} is kept constant at 0 V. Here, the field-plate length L_{FP} = 0.6 μm, the surface-state length L_{S} is 0.4 μm, and the surface-state density is $3\mathrm{x}10^{12}$ cm^{-2}. The thickness of SiO_2 layer T_{i} is 0.3, 0.1 and 0.02 μm, respectively in Figs. 2(a), (b) and (c). In Figs.2(a) and (b), the drain current I_{D} remains at a low value for some periods (10^{-10} – 10^{-1} s) and begins to increase slowly, showing drain lag behavior. It is understood that the drain current begins to increase when the deep-acceptor surface states begin to capture holes [12] or emit electrons. It is clearly seen that the change of drain current is smaller for the case with thin T_{i}, and the slow transient disappear when T_{i} is 0.02 μm. We will descuss below why this happens. Figure3 shows the changes of ionized deep-acceptor density N_{SA}^{-} at the interface when (a) T_{i} = 0.3 μm and (b) T_{i} = 0.02 μm. When T_{i} = 0.3μm, N_{SA}^{-} decreases corresponding to the increase in I_{D}. On the other hand, when T_{i} = 0.02 μm, N_{SA}^{-} is almost unchanged. It is understood that in this case the surface-state effects are completely masked by the field plate.

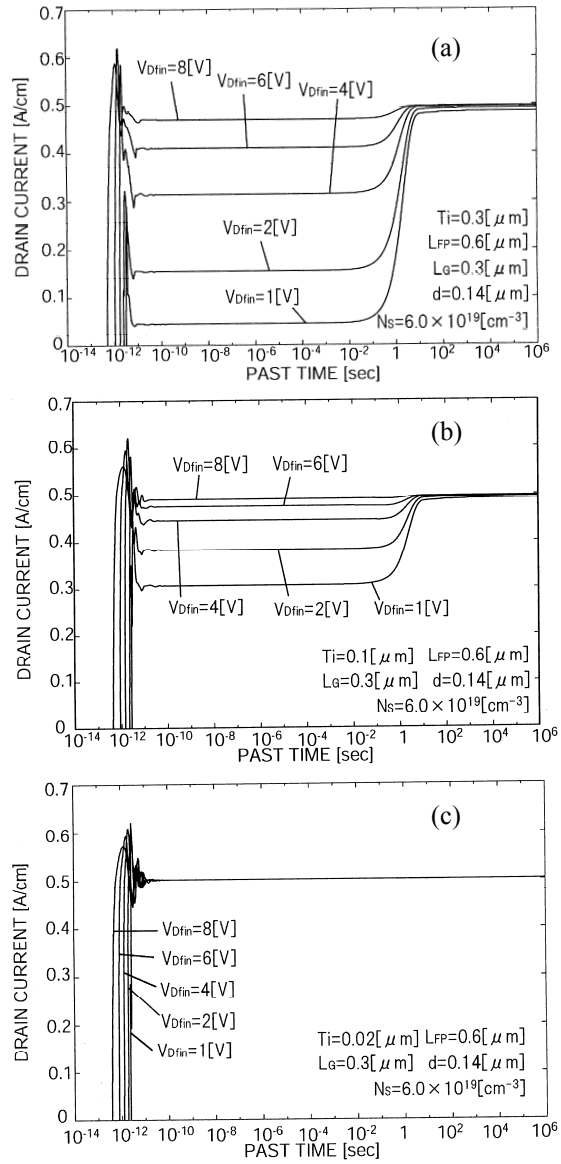

Figure 2: Calculated drain-current responses of GaAs MESFETs when V_{D} is lowered abruptly from 10 V to V_{Dfin} and V_{G} is kept constant at 0 V. L_{FP} = 0.6 μm. N_{S} = $3\mathrm{x}10^{12}$ cm^{-2} and L_{S} is 0.4 μm. (a) T_{i} = 0.3 μm, (b) T_{i} = 0.1 μm, (c) T_{i} = 0.02 μm.

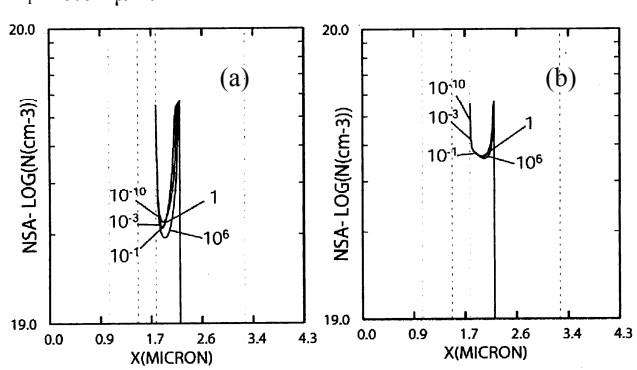

Figure 3: Change of ionized deep-acceptor density with time t, corresponding to Fig.2 (V_{Dfin} = 2 V). (a) T_{i} = 0.3 μm, (b) T_{i} = 0.02 μm.

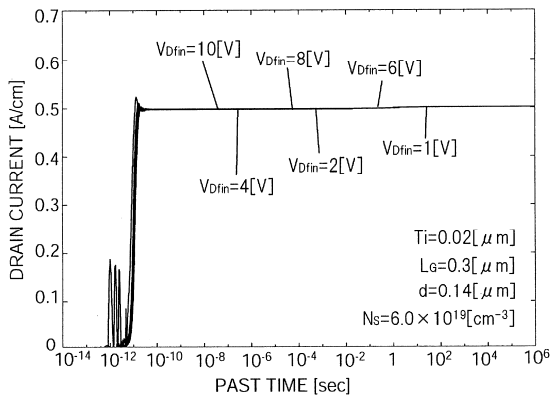

Figure 4: Calculated turn-on characteristics for L_{FP} = 0.6 μm and T_i = 0.02 μm when V_D is lowered abruptly from 10 V to V_{Dfin} and V_G is changed from V_{th} to 0 V. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

4 TURN-ON CHARACTERISTICS AND CURRENT SLUMP

Next, we have calculated a case when V_G is also changed from an off point. V_G is changed from the threshold voltage V_{th} to 0 V, and V_D is lowered from 10 V to V_{Dfin}. V_{th} is defined here as a gate voltage where the drain current I_D becomes 5x10^{-3} A/cm. The characteristics become similar to those shown in Fig.2, although some transients arise when only V_G is changed (gate lag), and hence the current reduction rate becomes higher than that of drain lag. This current reduction is called current slump which is a combined effect of drain lag and gate lag.

Figure 4 shows calculated turn-on characteristics when L_{FP} = 0.6 μm and T_i is thin (0.02 μm). As is similar to the case of drain lag, the slow current transients disappear, indicating that current slump are completely removed in this case. This is because the surface-state effects are completely masked by the field plate when T_i is thin.

5 FIELD-PLATE PARAMETER DEPENDENCE AND REMOVAL OF CURRENT SLUMP

We have next studied dependence of lag phenomena and current slump on the field-plate length L_{FP} and on the SiO_2 layer thickness T_i.

Figure 5 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, with T_i as a parameter. Here L_{FP} = 0.6 μm. As T_i becomes thin, the lags and current slump are reduced, and they are completely removed when T_i becomes thinner than 0.02 μm. This is because surface-state effects are completely masked by the field plate, as mentioned before. When T_i is thin, the gate parasitic capacitance becomes a problem, but this removal of current slump is still a very interesting result.

Figiure 6 shows current reduction rates $\Delta I_D/I_D$ due to current slump as a function of SiO_2 layer thickness T_i, with

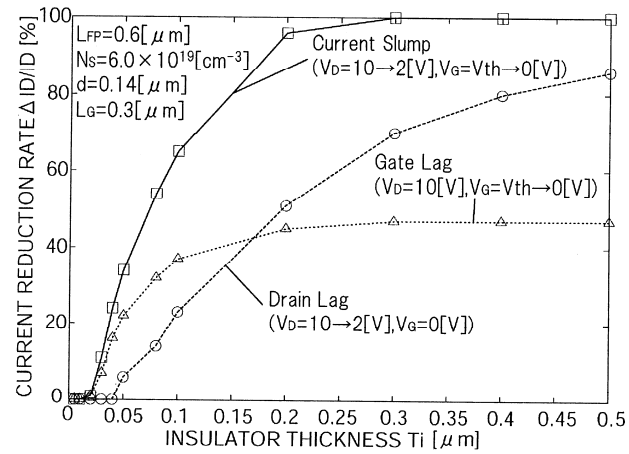

Figure 5: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag as a function of SiO_2 layer thickness T_i in the case of L_{FP} = 0.6 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

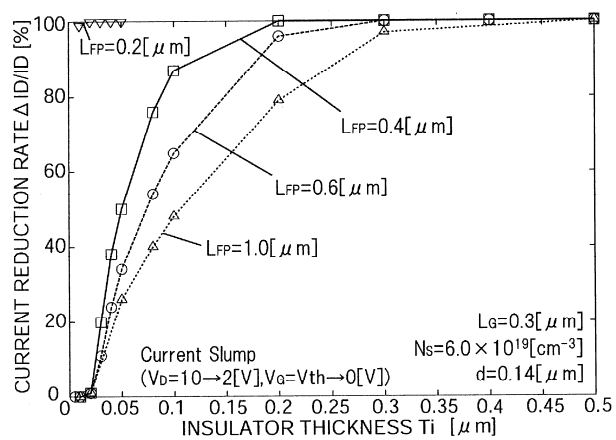

Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current slump, as a function of SiO_2 layer thickness T_i, with field-plate length L_{FP} as a parameter. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

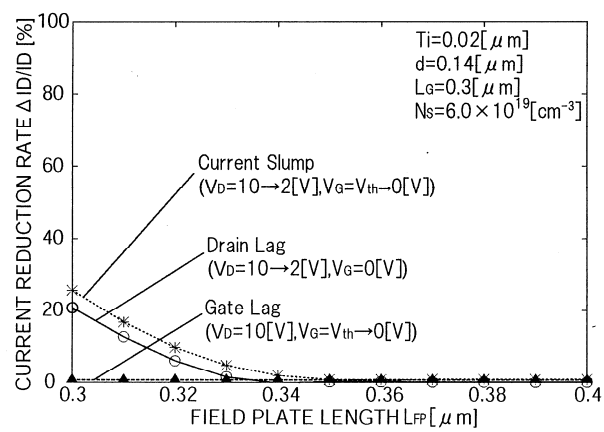

Figure 7: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag as a function of field-plate length L_{FP} (between 0.3 and 0.4 μm) in the case of T_i = 0.02 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

field-plate length L_{FP} as a parameter. It is seen that when L_{FP} becomes shorter, the current slump becomes larger, but it is completely removed when T_i becomes thinner than 0.02 μm even if L_{FP} is equal to the surface-state layer length L_S (0.4 μm), although the current slump becomes very large when L_{FP} = 0.2 μm.

In order to study how short we can reduce the field-plate length L_{FP} while maintaining the removal of current slump, we calculate in detail the lags and current slump between L_{FP} = 0.3 μm and 0.4 μm in the case of T_i = 0.02 μm. Figure 7 shows the results. From this figure, we can conclude that the current slump is completely removed even if L_{FP} is shortened to 0.35 μm.

6 CONCLUSION

Two-dimensional transient analysis of field-plate GaAs MESFETs has been performed by considering surface states in the region from the gate toward the drain. The field-plate length and the thickness of SiO_2 passivation layer are varied as parameters. It has been shown that the drain lag is not removed when the SiO_2 layer is thick even if the field-plate length is longer than the length of surface-state region. But when the SiO_2 layer becomes thinner than 0.02 μm, the drain lag, gate lag and current slump are completely removed by introducing a field plate longer than the surface-state layer length because the surface-state effects may be masked. By carefully examining the field-plate length dependence of lags and current collapse when the SiO_2 layer thickness is 0.02 μm, it has been found that they are completely removed even if the field-plate length is a little shorter than the surface-state layer length.

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