

Reliability-aware Device Compact Modeling and Implications on Circuit Aging Simulations

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ABSTRACT

This paper describes a reliability-aware device compact modeling method which addresses the aging feedback and coupling effects. The device reliability characteristics are introduced first including these two effects, which requires considerations from circuit aging simulations. Following that the current landscape of the circuit aging simulations is reviewed. A reliability-aware compact modeling method, the dynamic time evolution method (DTEM) developed to address the emerging simulation requirements is described, which integrates a reliability module, e.g. the transistor degradations with its operation time, inside the compact model together with other advanced effect models. The DTEM applications in circuit aging simulations are demonstrated after its implementation into a SPICE program.

Keywords: reliability modeling, circuit aging simulation, aging feedback, coupled aging

1 DEVICE RELIABILITY REQUIREMENTS ON AGING SIMULATION

Circuit reliability simulations are mandatory practices in today's IC design due to the reduced degradation margin with scaling. There are basically two categories of common reliability concerns: the probabilistic one (e.g. the time dependent dielectric breakdown, TDDB) and the non-probabilistic one (e.g. the hot carrier injection, HCI and negative bias temperature instability, NBTI). While a mean time to failure (MTTF) is always used to describe the significance of the former category, an evolutionary change of the transistors' characteristics like their threshold voltage is observed in the later category. A variety of models are derived based on the device reliability physics to describe the transistor parameter shift in the time domain. After incorporating these reliability models in a circuit simulator, circuit aging simulations are to obtain gradual changes of the circuit performance subject to its working environment. As such certain algorithms are needed at the interface of the reliability models and the simulator, to allow accurate and fast aging simulations on top of the circuit function designs. For the consideration of the simulation accuracy, the unique reliability physics need to be covered in the algorithm.

Fig.1 show one category of the important features in the HCI and NBTI induced transistors' threshold voltage shift of NMOS and PMOS respectively. A classical model [1] with a time power function (t^n) is used to describe the HCI (the dash line) in Fig.1 (a). While the model matches with the data well in a short time range, clear deviations are seen when the total threshold voltage shift reaches the *mV* level. This unique feature that has been reported in the literatures [2] is not explained by the model. One reason is that along with the transistor aging its saturation current drops and the reduced drain/substrate current decrease further degradation rate. Ignoring of the negative feedback property termed as the aging feedback causes overestimate of the HCI effects on the circuit aging. Fig.1 (b) plots the PMOS threshold voltage change during the NBTI stress phase and recovery phase. One common feature of several NBTI models [3,4] is that the recovery rate depends on the peak threshold

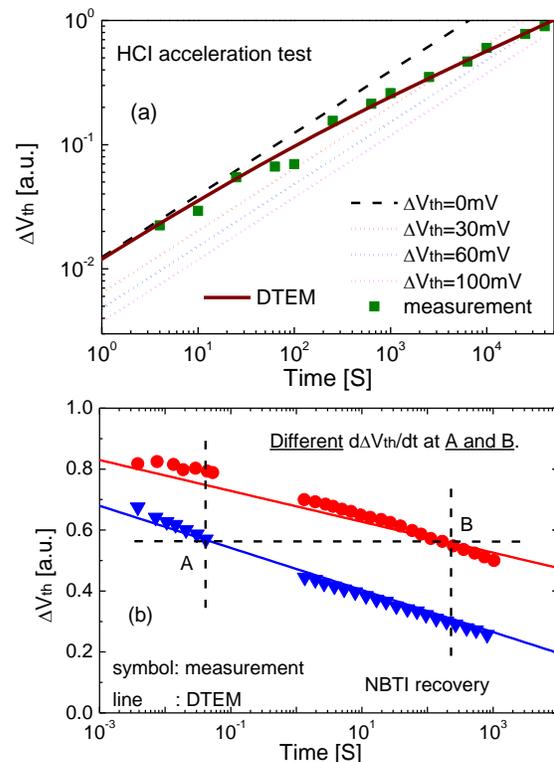


Fig.1 Unique features of the reliability physics. (a) aging feedback in HCI and (b) history dependent NBTI.

shift. Fig.1 (b) shows that one model [4] reproduces the the stress and recovery phases (solid line). During practical circuit operations, accounting for this history dependent recovery is essential under the dynamic voltage scaling when the recovery phase switches to a new stress phase.

Another uniqueness of the reliability physics is the coupling between different mechanisms, like the coupling of TDDB and NBTI based on their shared dependence of oxide trap states, the coupling between self-heating and reliability. Fig.2 plots the significant temperature dependence of NBTI simply due to the thermal related activations. In nanoscale transistors like FinFET or nanowires, the self-heating effect is significant which accelerates the NBTI degradations. The inset in Fig.2 shows one example simulation of the transistor self-heating. Certain algorithm is needed in the aging simulations to account for the coupling between the self-heating and degradation for a more accurate prediction.

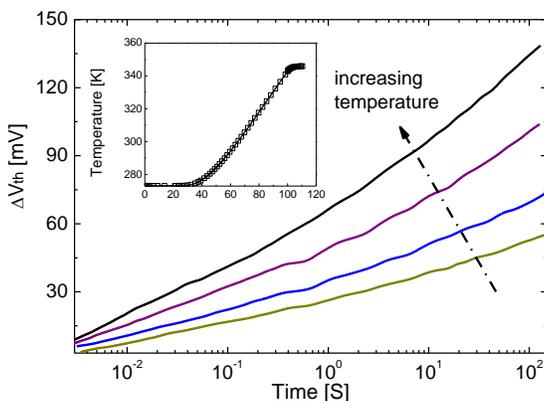


Fig.2 Measured NBTI induced threshold voltage shifts show clear temperature dependences, which in principle makes the NBTI a coupled effect with device self-heating. The inset shows one example self-heating simulation.

2 CURRENT AGING SIMULATION METHODS

Generally, aging simulations are done by running a circuit transient simulations together with a proper extrapolation algorithm. After the transient simulation for a representative period of circuit operations, degradations of the transistor parameters e.g. its threshold voltage are calculated with the corresponding HCI or NBTI models. Note that a step-by-step calculation of the reliability model is necessary since the circuit simulations are done in a time discretized way, so a certain ‘integral’ method is needed to accumulate the degradations in the transient simulation period. By assuming the circuits repeat its behaviors in the successive periods, a certain extrapolation algorithm is needed to calculate the transistor degradations after an interested working duration. The final goal is to obtain the circuit performances after a long term, e.g. 10 years as the common end of life (EOL) time.

Currently there are mainly two kinds of circuit aging simulation methods: the table-based method and the model-

based method. They are different in terms of their ‘integral’ to get the degradations during the transient simulation period and of their way of extrapolation to obtain the final aged transistor properties. Fig.3 plots the basic flow chart of the table-based aging simulation method. The first transient simulation is done with the fresh model parameters to yield the circuit nodal waveforms as outputs. These nodal voltages form the time-dependent stress on each MOSFET. After the transient simulations, a compact model is used to calculate the MOSFET’s reliability-related parameters like the terminal current or the oxide electric field. With these time dependent reliability parameters, another standalone program is executed to derive some intermediate variable that can be added or integrated linearly with time. A linear extrapolation follows to further derive this variable at the device EOL. A table composed of experimental data on the one-to-one relationship of this variable and the transistor parameter degradation is used to decide the final aged transistor parameters with necessary interpolations. With the aged parameters, a second circuit simulation is done to calculate the whole aged circuit performance. With an ‘AGE’ parameter as the intermediate variable, this aging simulation philosophy was implemented in the early BERT [5], and later in the Relxper. It separates the reliability calculation from the SPICE and device model, allows successful simulations of HCI induced aging and also flexible programming. This method is a bit unfavored for the NBTI induced aging without a similar ‘AGE’ variable.

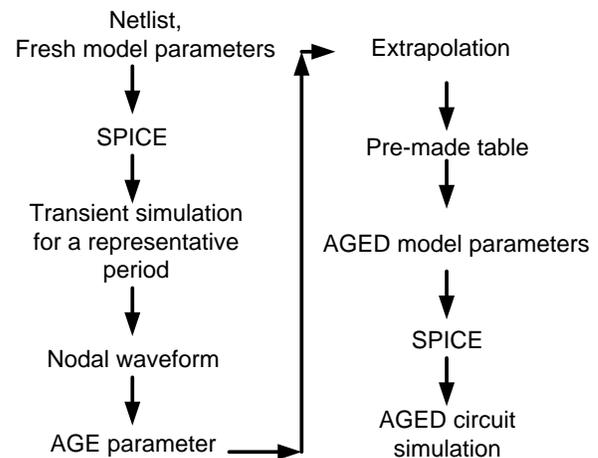


Fig.3 Flow chart of the table-based circuit aging simulation method. Assuming the circuit goes through its lifetime without any degradations, the nodal waveforms form the stress for transistors. By integrating these stress with time till the EOL and obtaining the aged model parameter via table looking-up, the aged model parameters are derived and the aging circuit characteristics.

Fig.4 plots the flow chart of the model-based aging simulation method. Similar to the table method, the two-step calculation (pre-stress and post-stress) is inherited. Without storing the circuit nodal waveforms and doing the table-lookup, in the pre-stress integrations (accumulations)

of each MOSFET's parameter degradation is done simultaneously along with the transient simulation via a certain HCI or NBTI model. The extrapolation is performed to derive the aged transistor parameter at the device EOL. The integration and extrapolation are executed by an routine that reads out the reliability model variables via an interface with the compact model. With these aged parameters the post-stress simulations are used to obtain the aged circuit performances. Another feature of this model-based method is that multiple rounds of pre-stress and post-stress simulations are optionally performed. It is one way to implement the aging feedback effect. In each pre-stress simulations the transistor parameters are those aged ones obtained from previous post-stress simulations. The reason is discussed in the first section. A few simulation tools follows this methodology including the MOSRA [6] and the TSMC model interface (TMI) [7].

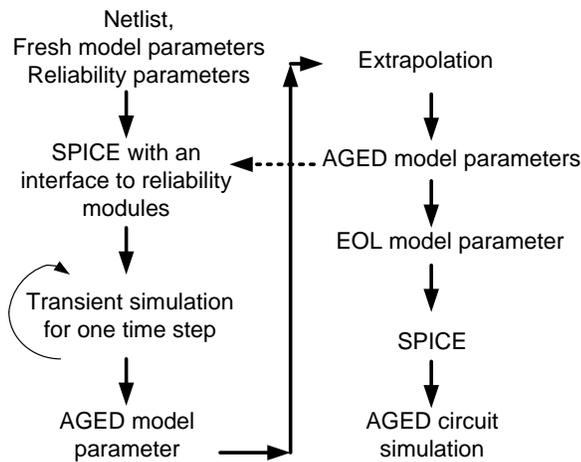


Fig.4 Flow chart of the model-based aging simulation method. SPICE is extended with an interface to reliability modules. During transient simulations, model parameters aging is calculated simultaneously. An extrapolation is used to derive the aged model parameters after a long term. An option of multiple simulation rounds (dashed arrow) is available for the simulation accuracy considerations.

3 RELIABILITY-AWARE MODELING FOR AGING SIMULATIONS

The above model-based simulation method provides one possible solution for both the HCI and NBTI aging. There are several emerging aging simulation requirements for another kind of simulation method. The aging feedback with the dynamic voltage and frequency scalings in modern circuits needs one method that is adaptive to any stress waveforms in the circuit operations. The aging coupling effect requires bi-directional communication between the compact model and the reliability calculation routine which is not supported in the current solutions. A reliability-aware device compact modeling method called the dynamic time evolution method (DTEM) is proposed and under development to address these requirements.

Fig.5 plots the basic flow chart of the circuit aging simulations with DTEM. Aged circuit performances are obtained from one SPICE simulation run. It is done by integrating the reliability module into the compact model routine, together with the core model and advanced effect modules. Different from the available solutions, the interface between the reliability calculation and compact model calculation is eliminated. At each time step of the transient simulations, the reliability module calculates each transistor's accumulative degradations, and dynamically feed the result to the other modules for the next time point circuit calculation. In this way the aging feedback is always taken into consideration. Working with a proper NBTI module, DTEM is compatible with any stress waveforms during the representative operation period, covering the dynamic frequency and voltage scaling. DTEM traces the transistor degradation in a time evolution manner, hence can describe the NBTI recovery and the smooth transitions from the recovery stage to the new stress stage, not confined by certain stress waveforms any more.

With the DTEM-based aging simulation framework, the reliability coupling effects are easily accounted for. During the transient simulations, variables in the reliability module are available to other modules for necessary considerations of coupled effects. For example, the threshold increase will cause a reduction in the current which further reduce the self-heating effect and the device temperature.

In terms of the functions and implementations of the reliability module, they are similar to the self-heating modules in some compact models, which usually use an internal thermal node and a RC subcircuit to represent the time domain differential equation. The extrapolation algorithm as part of the DTEM is embedded in the reliability module. A decision is made at each time point for the time evolution or extrapolation. For the extrapolation, the

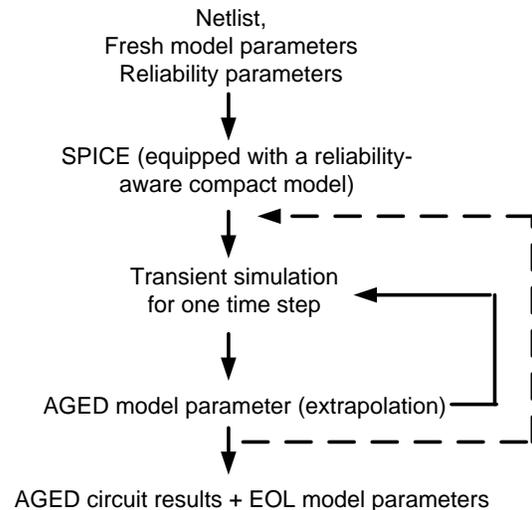


Fig.5 Flow chart of the DTEM for circuit aging simulation. SPICE is equipped with a reliability-aware compact model. Model parameters are aged and fed into the circuit immediately by the model, where the extrapolation is also performed.

algorithm considering the aging feedback of HCI and NBTI is executed and used in the next time evolution simulation. Similar to the current simulation solutions, multiple evolution and extrapolations are designed to mitigate the extrapolation errors. To the SPICE simulator there is no difference between the evolution and extrapolation stages. The evolution and extrapolation algorithms of the reliability module are built on top of the current SPICE architecture.

Fig.6 plots the time evolution of the NBTI degradation with the dynamic voltage and frequency scalings. The NBTI model [4] is used. Based on an equivalent time concept [8] the time duration and voltage dependent degradation rate is considered. Partial recovery from high to low stress depends on the low stress level and the transition from the recovery to new degradation under the low stress is fully accounted. At the same time, the partial recovery shows dependence on its time duration under the dynamic frequency scaling, without a constant recovery factor. These properties of NBTI stress and recovery observed in experimental data are reproduced with the DTEM. The SPICE simulation stability is possibly one concern for the DTEM due to the dynamic feedback. It proves that the simulation instabilities during the evolution phase are weaker than those during the extrapolation phase due to the smaller absolutely changes of the parameter shift, while the later one is tolerant in the current solutions.

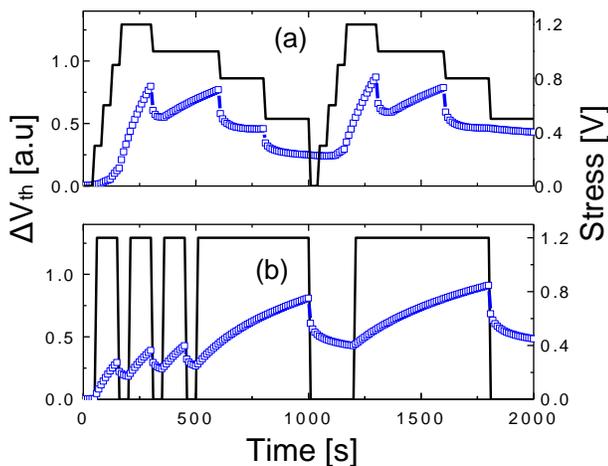


Fig.6 NBTI calculations under (a) the dynamic voltage scaling and (b) the dynamic frequency scaling are made possible with DTEM.

DTEM for the reliability-aware compact modeling is implemented in a SPICE simulator to demonstrate the aging simulations. No internal node is added thus the circuit matrix dimension does not change compared to fresh circuit simulations, and the matrix solver is not affected. The circuit and each transistor are monitored with the parameter shifting. DTEM is tested with different circuits including the nand gate, the SRAM, the cross couple LC-VCO etc without instability issues. As one example, Fig.7 plots the aging trace of two transistors in the first stage of a 17-stage ring oscillator (RO), and the overall degradations of the RO

frequency. The results show that for the long term 10 year aging, a 17% overestimation of the NBTI threshold shift is avoided by considering the aging feedback. The reliability-aware modeling allows the monitoring of a continuous parameter changes in the circuit and each transistor.

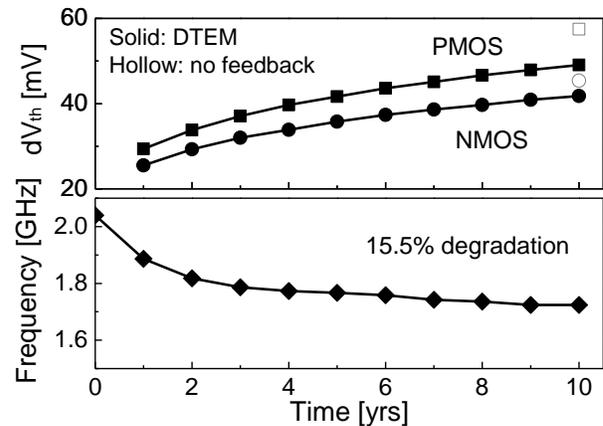


Fig.7 DTEM traces the aging of each transistors and the whole circuit with accounting for the feedback effect.

4 CONCLUSIONS

One reliability-aware compact modeling method, the dynamic time evolution method (DTEM) is described in this paper. It covers the aging feedback and coupling effect by integrating the reliability module inside the compact model. Compared to the current aging simulation solutions, the DTEM models the circuit reliability under dynamic voltage and frequency scaling. Circuit aging simulations demonstrate the versatility of DTEM and also its stability, with considering different coupling effects.

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