Proposal of a router circuit based on nanoelectronic devices

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ABSTRACT

In this work a fully nanoelectronic circuit for an information router based on single-electron devices aiming at Network-on-Chip (NoC) applications is proposed and simulated. Digital modules were designed and evaluated to build the whole router circuit. The performance was also analyzed and compared to other nanoelectronic circuit implementation. It will be shown that the SET-based router has a promising performance considering parameters such as speed, power consumption and area.

Keywords: router, nanoelectronic, single-electron transistor

1 INTRODUCTION

An information router in a communication network should deliver data packages from one node to other node. For executing this delivery task efficiently, the router should choose the best path between the nodes. The best path can be fixed or can change every time a new data package must be delivered [1,2].

Router circuits can be used on Network–on-Chip (NoCs) to keep track of communication paths inside the chip [3]. This solution can solve the performance requirements of the modern single chip with billion transistors processors. The NoC approach provides a highly structured and scalable solution to tackle the communication problems in those complex systems, due to the high bandwidth, relatively low power consumption and low latency exhibited by NoCs in comparison to more conservative designs. It is important to highlight that because of the router a NoC is able to reduce the number of physical interconnection required between modules to build a fully connected network [1,3]. So, area and power consumption are also reduced. All these features make NoCs suitable architectures for nanoelectronic devices [4]. Comparing to CMOS technology nanodevices are not sufficiently mature. However, the disadvantages of such a new technology can be offset in part by alternative architectures/systems [4].

Other important aspect concerns the physical implementation of nanodevices. In the begining these devices could operate simulateously with microelectronic devices, in order to maximize the performance of current processors in specific applications, such as memories [4].

In this paper a router circuit completely based on nanoelectronic devices aiming at Network-on-Chip (NoC) applications will be proposed and simulated. Digital modules will be designed and evaluated to build the whole router circuit. The performance will also be analyzed and compared to other nanoelectronic circuit implementation [5,6]. It will be shown that the SET-based router has a promising performance considering parameters such as speed, power consumption and area.

2 SINGLE-ELECTRON TRANSISTOR

The single-electron transistor (SET) consists of two tunnel junctions connected together, forming an island between them, as shown in figure 1 [7,8,9,10].

Its operation is based on the flow control of a single electron or a small group of electrons by tunneling which lends to a very low power consumption during operation. The gate voltage manipulates the Fermi level, i.e., the higher energy quantum level occupied on the island, thus controlling the conduction electrons by the transistor. The operation of SETs up to 350 K have already been reported [10].

For this work was employed a SET model for SPICE proposed by Lientsching *et al.* [11], which operates at room temperature.

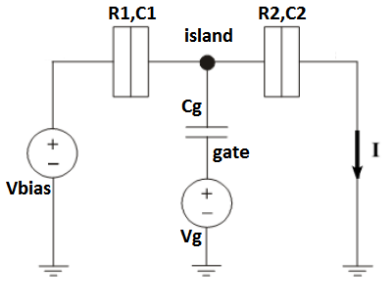

Figure 1: Single-electron transistor

3 ROUTER ARCHITECTURE

The concept of a generic router can be separated into two planes: the control plane and the data plane (also known as fowarding plane). Whereas the control plane deals with the routing protocols and routing table, the data plane is all about the actual data traffic through the router. This work focus on the data plane. The choosen architecture has been previously implemented with QCA [5] and the final results will be compared.

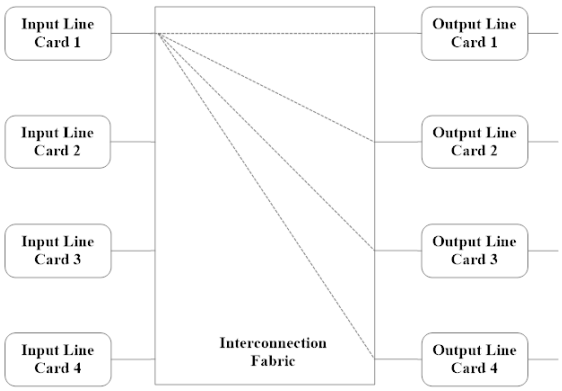

Figure 2: Router data plane.

Figure 2 shows a high level view of the data plane. This work presents a 4x4 router and its major components are:

- Input Line Card: it is the interface through which the router receives the data. It determines the output interface through the router look-up table
- Interconnection Fabric: it connects the input line cards to the output line cards
- Output Line Card: it receives and stores the data fowarded through the interconnection fabric and transmits the packets through the link.

Figure 3 presents the router architecture with its components. Each input line card consists of a demultiplexer (abbreviated as demux). It receives the input bit and forwards it accordingly to the look-up table, which is given by the select lines of the DEMUX.

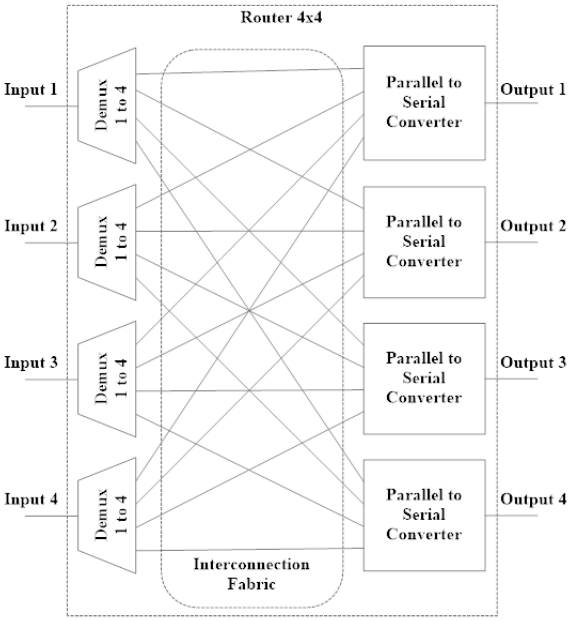

Figure 3: Router Architecture.

The interconnection fabric consists of a direct connection between the input line cards and output line cards. The last component is the output line card, which consists of a parallel-to-serial converter (PISO). The PISO queues all the received parallel bits and forwards them through the link.

All the components of this digital architecture were designed with a nanoelectronic NAND gate (nanoNAND) as base element. This nanoNAND gate consists of four SET transistors [12]. Even the NOT gate was implemented from a NAND gate, just by shorcircuiting both inputs. A NOT symbol was created to simpify the circuit assembly. All simulations were made using LTSpice [13] and the following circuit images are snapshots of the simulations.

The next subsections will describe how each of the router components has been designed and works, and the following sections will present the simulations and results.

3.1 DEMUX

A DEMUX is an electronic device consisting of one input and multiple outputs. The input data is switched to one of the outputs through the select control.

This router makes use of 1-to-4 DEMUXs, which cosists of one input X, four outputs Y0, Y1, Y2 and Y3, two select lines C1 and C0 and an enable switch (figure 4). By choosing the output to which will be sent the data the select lines act as the router look-up table.

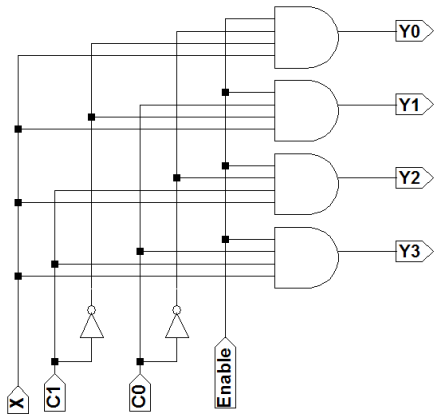

Figure 4: DEMUX 1 to 4.

This DEMUX consists of four AND gates with four inputs. The AND gates were designed with six nanoNAND gates, as shown in figure 5.

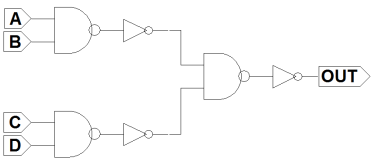

Figure 5: Four input AND gate.

3.2 Parallel-to-Serial Converter

The parallel-to-serial converter, or parallel-in serial-out shift register (PISO), loads the parallel input when the write/shift control is low. After this, when the control is set to high, the inputs are shifted to the serial output accordingly to the clock cycles.

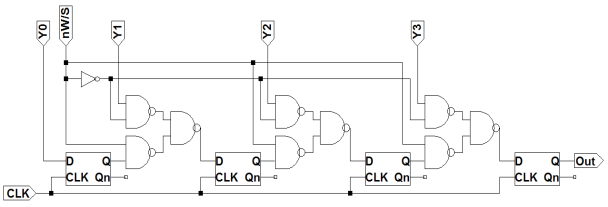

Figure 6: Parallel to Serial Converter.

In figure 6, the parallel inputs are D1, D2, D3 and D4. When in shift mode, everytime the clock goes up the next input is lined in the output, starting with input D4. It is important to note that the write/shtift control must be synchronised with the clock to avoid loading the new data before the last data has been completely shifted to the output. It takes four clock cycles to shift all the four data inputs to the output.

3.3 Router

As shown in figure 7, the router is composed of four DEMUXs, one for each input, and four PISO modules for the outputs. EachDEMUX is directly connected to all four PISO modules. The router look-up table is loaded on the demuxes select controls.

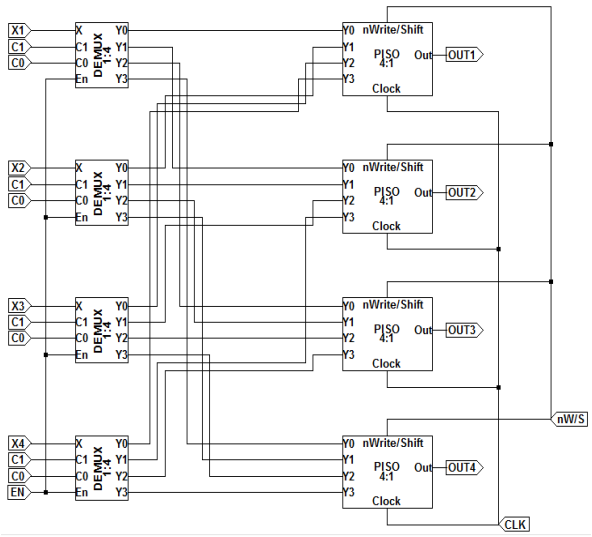

Figure 7: Router 4x4.

4 SIMULATION AND RESULTS

This section presents the simulations made for each component described on the section above and their results.

4.1 DEMUX

During the simulation of the DEMUX, the enable switch were kept at a high level of 0.5 V. The graphic on figure 8 shows input X, the entries on the select control C1 and C0 and the four outputs Y0 through Y3. It is possible to observe that, when selected, the output follows the input X.

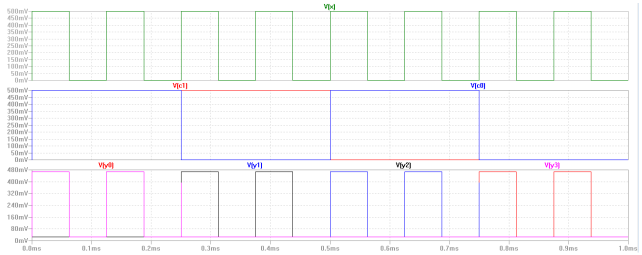

Figure 8: Demux simulation.

4.2 Parallel-to-Serial Converter

During the PISO simulation three different four bit data were sequentialy loaded into the parallel inputs (Table 1). In order to guarantee all three packets are completely forwarded the simulation runs for twelve clock cycles. Also the write control is activated half a cycle before the new packet must be fowarded and the shift control is activated half a cycle after the first bit (D4) has been transmitted.

Table 1: Input packets for PISO simulation.

	D1	D2	D3	D4
Packet 1	1	0	1	0
Packet 2	1	1	0	1
Packet 3	0	1	0	0

The serial string on the output will be D4D3D2D1. Once the first data packet has been transmitted the next packet will be fowarded in the same order. This is shown on figure 9.

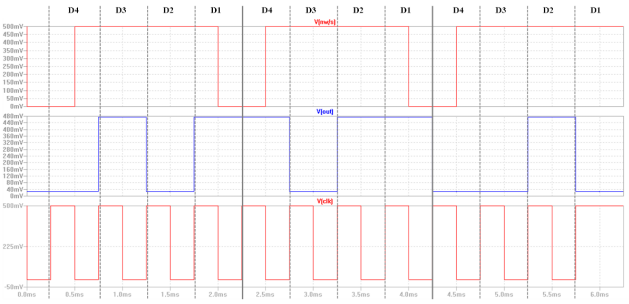

Figure 9: PISO simulation.

4.3 Router

For testing the router two tests were developed. On the first test all inputs are high level at 0.5 V and they are fowarded to random outputs (accordingly to the look-up table in table 2). Comparing with table 2 it is possible to see that data arrives correctly on the selected output (figure 10).

Table 2: Router look-up table.

	C1	C0
Input 1	1	0
Input 2	0	0
Input 3	1	1
Input 4	0	1

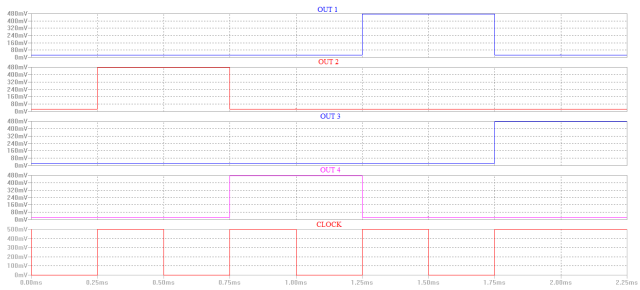

Figure 10: First router test.

The second test consists of all inputs being fowarded to output 3. The sequency employed is the same one on table 2. Figure 11 shows the correct buffering on output 3 whereas the other outputs remains 0.

4.4 Area and Power

Because the circuit is composed of nanoNAND gates it is possible to calculate the area and power consumption [12] of the circuit. Table 3 shows the area and power dissipation for each component of the router.

5 CONCLUSION

The router is an important element of NoCs. A nanoelectronic router based on SET can not only reduce the occupied area but also improve its power and speed performance. It is esteemed that the SET cutoff frequency is arround 1 THz [14].

This router area and power consumption are 55040 nm² and 1120 pW respectively (table 3). The QCA architecture router [5] occupies an area of 13.81 µm² which is a lot more than the SET router.

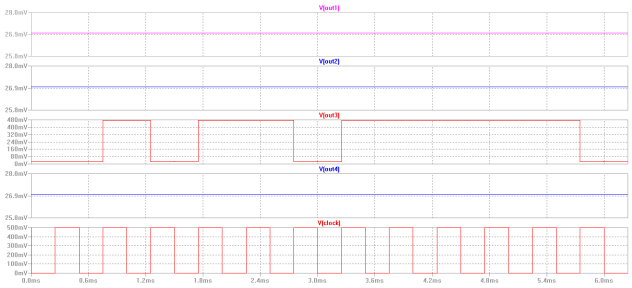

Figure 11: Second router test.

Table 3: DEMUX area and power consumption.

Component	# nanoNand	Area	Power
nanoNAND	1	172 nm²	3.5 pW
Demux	26	4472 nm²	91 pW
PISO	54	9288 nm²	189 pW
Router	320	55040 nm²	1120 pW

ACKNOWLEDGEMENTS

The authors are grateful to CAPES, PQ/CNPq and INCT-NAMITEC for support.

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