Printed Via Technology for Oxide Thin Film Transistors and Inverters

Meilan Xie[1], Shaojing Wu[1], Zheng Chen[1*], Xinzhou Wu[1] and Zheng Cui[1*]

[1]Printable Electronics Research Centre, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, Suzhou, 215123, People's Republic of China,E-mail: zchen2007@sinano.ac.cn

ABSTRACT

Two printed via processes are reported for interconnecting transistors and circuits through dielectric layers. Inkjet printing was used to print corrosive ink materials on dielectric layer, which etch through the dielectric layer to form via holes. Subsequent printing of conductive tracks establishes electric connection between upper and lower levels of circuits. High performance thin-film transistors have been fabricated by printing ITO electrodes and IZO semiconductor channels. The printed transistors were then connected to form inverter circuits through printed via holes. High mobility and high voltage gains were exhibited with the printed transistors and inverters, demonstrating the feasibility of printed via process. The method is scalable to large array of complicated circuits, paving the way to construct integrated circuits in printed electronics.

Keywords: inkjet printing, oxide thin film transisitors, high performance, inverters, printed electronics.

1. INTRODUCTION

In recent years, printed electronics have attracted more and more attentions because of the advantages of high-throughput, large area, flexible and low cost etc [1-4]. Fabrication process can be simplified by using printing-based techniques instead of conventional photolithography and vacuum deposition [5]. Printed thin film transistors have been demonstrated, employing semiconductor inks such as carbon nanotubes, organic polymers or organic small molecules and metal oxides etc [4, 6-9]. Most of the printed transistors so far exhibited high charge mobility of more than 1cm^2/Vs and high on/off ratio. In recent years, printed electronics starts to evolve from single components to systems where interconnects are essential for transistors to be connected into circuits [4, 10,11].

In the present work, two printing-based techniques have been developed to make holes in order to achieve interconnection through dielectric oxide layer. One is employing special silver paste in combination with heating treatment and another is employing inkjet printable alkaline ink. The techniques have been applied to fabrication of bottom-gated metal oxide thin-film transistors where gate electrodes under dielectric layer were connected to source/drain electrodes above the dielectric layer to form a simple inverter circuit. Printing fabrication of other parts of the thin-film transistors was also investigated, including electrodes and semiconductor layer. The present work has demonstrated the feasibility of printed thin-film transistors and circuits without employing any conventional photolithographic patterning and etching processes.

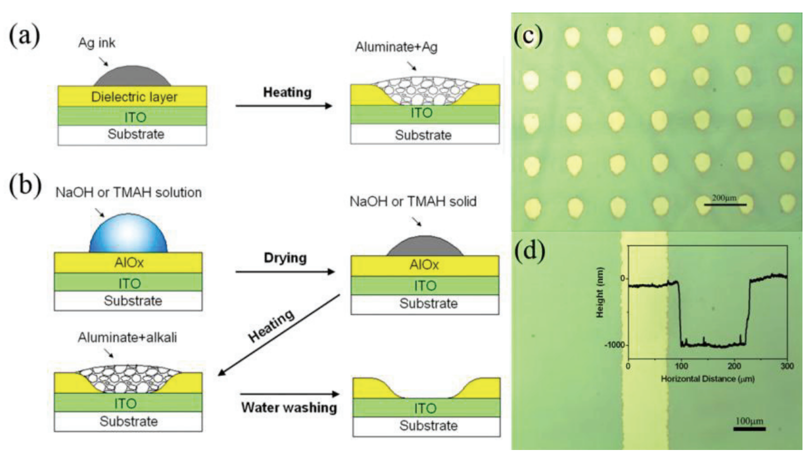

Figure 1 (a) One print-based via technology with Ag paste as the "via agent". (b) Another print-based via technology using the solid alkali as the "via agent" for some oxide dielectric layer, such as AlOx. The optical image of a via dot array (c) and line (d) on 100nm AlOx/ITO/glass, which was prepared by printed NaOH etching at 200^{o}C for 5min as shown in (b).

2. EXPERIMENTAL

Indium tin oxide (ITO) ink and indium zinc oxide (IZO) ink were prepared by dissolving tin (IV) chloride ($SnCl_4 \cdot 5H_2O$), indium chloride ($InCl_3 \cdot xH_2O$) and zinc chloride ($ZnCl_2$) in 2-methoxyethanol. The molar ratios of ITO and IZO were Sn/In=10/90 and In/Zn=70/30, respectively. Small amount of ethanolamine was added to the solution for long-term stability. Eagle XG glass substrates were purchased from Corning and they were cleaned by ultrasonic washing in P3 Siliron HS aqueous solution and deionized water in turn, prior to use. All of the electrodes, semiconductor channels and interconnects were fabricated by printing ITO ink and IZO ink using an ink-jet printer (Dimatix DMP-2831). Dielectric layer was made of aluminum oxide (AlOx) by atomic-layer-deposition (Cambridge NanoTech) at 300^{o}C.

To achieve conductive "via" in the aluminum oxide dielectric film, two printing-based techniques were used. In the first one, silver paste (Inktec, TEC-PA-045) was dip printed on the dielectric oxide layer, following by heating at 550^{o}C for 1 hour. In the second method, NaOH was ink-jet printed on the dielectric layer using its aqueous solution, followed by heating and washing. With both methods, small via openings through the dielectric layer were obtained.

The thickness and morphology of printed layers were measured by Dektak 150 Surface Profiler. The electrical characteristics were measured under dark conditions in ambient air using Keithley semiconductor parameter analyzer (model 4200-SCS). To measure the dielectric constant of the aluminum oxide layer, Al top electrode with area of 0.5mm^2 was thermally evaporated on the surface of the aluminum oxide layer grown on the ITO glass.

3. RESULTS AND DISCUSSION

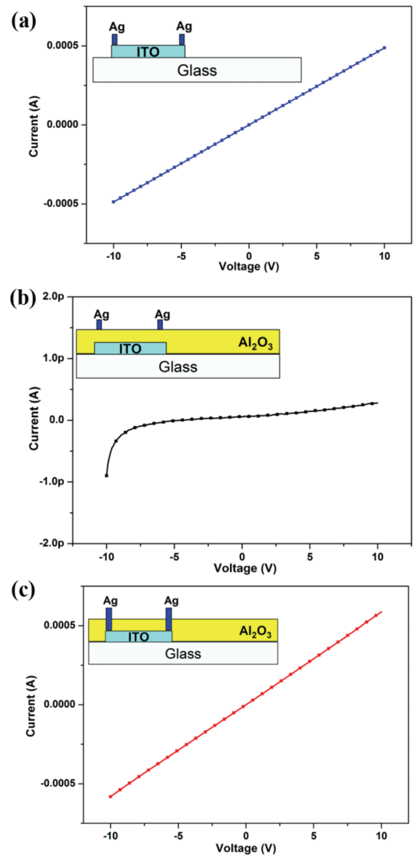

Figure 2 (a) I-V characteristic of the a printed ITO wire on glass, (b) I-V characteristic between the two silver paste on the dielectric layer under which the printed ITO wire was, (c) I-V characteristic between the two silver paste, which destroyed the insulation of the under dielectric layer after heating at 550^{o}C for 1hour.

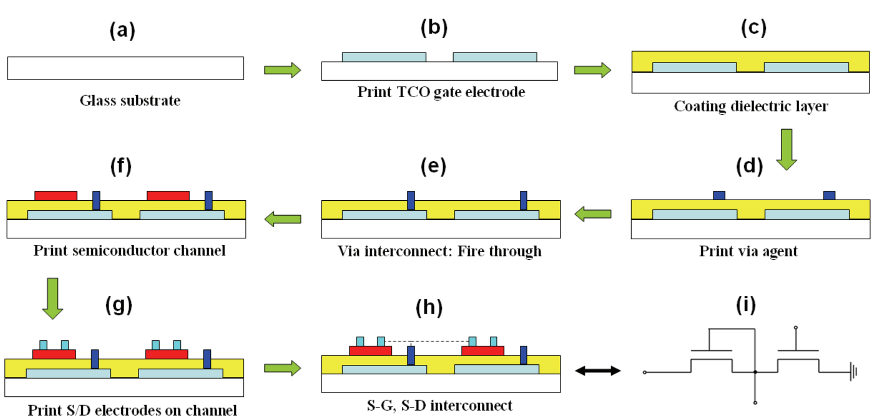

Figure 3 Fabrication process of an inverter with two unipolar transistors: (a) glass substrate, (b) printing TCO gate electrodes, (c) deposition of dielectric layer. (d) via agent were printed, (e) the via agent etch the dielectric layer and the electrical channel formed, (f) printing semiconductor channels, (g) printing source/drain electrodes, (h) electrodes were interconnected, (i) the inverter circuit diagram.

The details of printed via techniques are depicted in Figure 1. In our work, a "fire-through process"method [12] has been employed to make via holes as illustrated in Figure 1a. After thermal treatment in air, the printed Ag paste has 3b). Then, aluminum oxide dielectric layer covering the whole substrate is deposited using ALD (Figure 3c). Following the deposition of dielectric layer, via holes are fabricated by printing according to the aforementioned routes

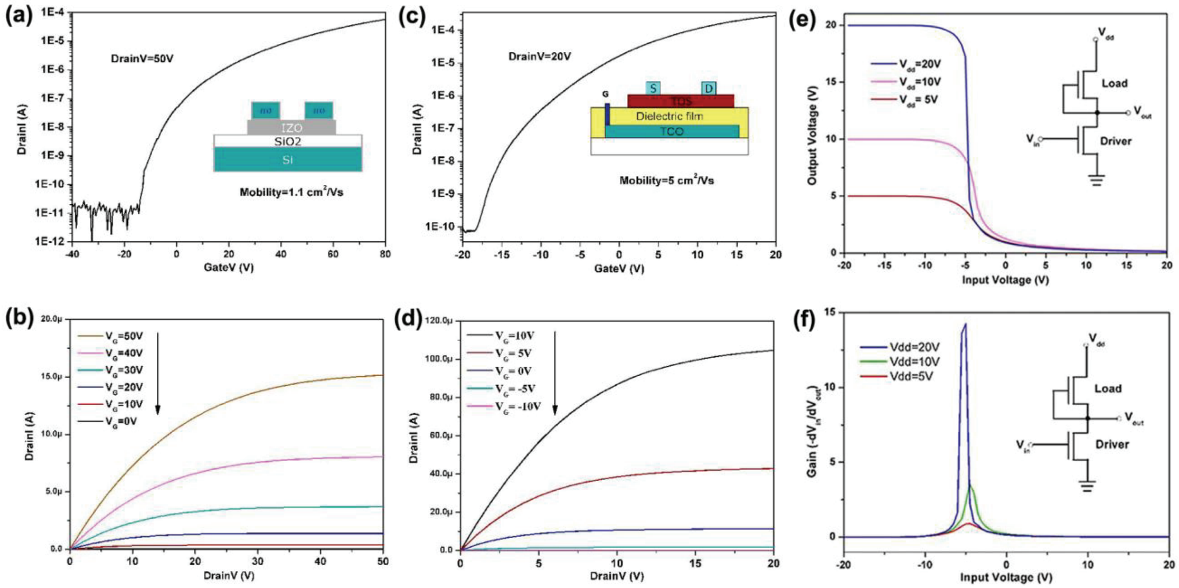

Figure 4 (a) Typical transfer characteristics of an optimal IZO TFT (W/L = 500/200μm), which consisted of printed IZO channel, printed ITO S/D electrodes, dielectric layer of 300nm SiO2 and gate electrode of heavily doped Si substrate. (b) The output characteristic of the same transistor in (a). (c) Typical transfer characteristics of an optimal IZO TFT (W/L= 500/200μm) as the route show in Figure 2, which consisted of printed IZO channel, printed ITO S/D electrodes, printed ITO gate electrode and 100nm dielectric layer of aluminum oxide. (d) The output characteristic of the same transistor in (c). (e) Voltage transfer characteristics of two IZO TFT inverter circuit prepared as the route show in Figure 1, where via was formed using printed NaOH (as shown in Figure 3b) and printed ITO as the interconnected wires. (f) The voltage gain of the inverter.

broken through the insulation of aluminum oxide layer and formed good electrical contact with the ITO film underneath (Figure 2). At least 550^{o}C of thermal annealing is needed if the aluminum oxide layer is 100nm thick, which limits the substrate material only to glass. For low temperature process, printed alkali such as NaOH, KOH and TMAH etc, can be employed to *in-situ* etch the aluminum oxide dielectric layer as illustrated in Figure 1b. This technique has been proved to produce via holes in aluminum oxide layer reliably in large area, as shown in Figure 1c-d. The etching of aluminum oxide is also thermally assisted. Typically, at temperature of 90^{o}C, it needs a few hours to etch through a 100nm aluminum oxide layer in the case of printed NaOH, whereas the etching time can be shortened to less than 5 min at 200^{o}C.

Figure 3 illustrated the process flow of making an inverter by the printed via strategy. The inverter, consisting of two unipolar transistors, is simple but has all the components for a transistor-based circuit, including patterned source/drain (S/D) electrodes, patterned gate electrodes, patterned semiconductor channel and interconnection of the electrodes on the both sides of the dielectric layer. In the first step, ITO ink is printed to form the gate electrodes on glass substrate (Figure 3d-e), which provides the conductive tunnel from the ITO gate electrode to the upper surface of dielectric layer. Then, IZO semiconductor channels and ITO source/drain electrodes are printed on the dielectric layer to construct the transistors. Finally, the transistors are connected by printing ITO lines over via holes to form the inverter, as shown in Figure 3h-i. The whole fabrication process involves only printing and film deposition, excluding any photolithographic patterning.

Figure 4 shows the transfer and output characteristics of printed IZO transistors with printed ITO source/drain electrodes on two types of substrate. For printed transistors on silicon substrate with SiO_2 as the dielectric layer, the field effect saturation mobility was ca. 1.2 cm^2/Vs and on/off ratio reached to 10^6. For printed transistors on glass with AlOx as the dielectric layer, they exhibited higher mobility of more than 5cm^2/Vs and on/off ratio of 10^6, which were superior to those solution process transparent oxide semiconductor (TOS) transistors whose source/drain electrodes were printed [13, 14] and even comparable to those solution-derived transistors with vacuum-deposited source/drain electrodes[8]. The difference of mobility for the two types of substrates was attributed to their different dielectric layers. The dielectric constant of AlOx layer is about 8.5, whereas the dielectric constant of SiO_2 layer is only 3.9.

Based on the aforementioned printed via technology, an inverter circuit was constructed by connecting two transistors through the above NaOH-based printing via technique (Figure 1b). Figure 4e-f showed the characteristics of inverter, which exhibited good logic function with a maximum voltage gain of 14.

4. CONCLUSION

Two printed via processes have been developed for interconnecting transistors and circuits through dielectric layers. With printed Ag paste or alkaline ink, lithographic patterning and etching can be avoided. High performance thin-film transistors have been fabricated by printing ITO electrodes and IZO semiconductor channels. The printed transistors were then connected to form inverter circuits through printed via holes. High mobility and high voltage gains were exhibited with the printed transistors and inverters, demonstrating the feasibility of printed via process. The method is scalable to large array of complicated circuits, paving the way to construct integrated circuits in printed electronics.

5. ACKNOWLEDGMENTS

This work was supported by National Program on Key Basic Research Project (973 Program, Grant No. 91123034), Strategic Priority Research Program of the Chinese Academy of Sciences (Grant No. XDA09020201)

REFERENCES

[1] Tekin, E., Smith, P.J., and Schubert, U.S.: 'Inkjet printing as a deposition and patterning tool for polymers and inorganic particles', Soft Matter, 2008, 4, (4), pp. 703-713

[2] Russo, A., Ahn, B.Y., Adams, J.J., Duoss, E.B., Bernhard, J.T., and Lewis, J.A.: 'Pen-on-Paper Flexible Electronics', Advanced Materials, 2011, 23, (30), pp. 3426

[3] Kaufmann, T., and Ravoo, B.J.: 'Stamps, inks and substrates: polymers in microcontact printing', Polymer Chemistry, 2010, 1, (4), pp. 371-387

[4] Jung, M., Kim, J., Noh, J., Lim, N., Lim, C., Lee, G., Kim, J., Kang, H., Jung, K., Leonard, A.D., Tour, J.M., and Cho, G.: 'All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils', IEEE Transactions on Electron Devices, 2010, 57, (3), pp. 571-580

[5] Fortunato, E., Barquinha, P., and Martins, R.: 'Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances', Advanced Materials, 2012, 24, (22), pp. 2945-2986

[6] Hennek, J.W., Xia, Y., Everaerts, K., Hersam, M.C., Facchetti, A., and Marks, T.J.: 'Reduced Contact Resistance in Inkjet Printed High-Performance Amorphous Indium Gallium Zinc Oxide Transistors', Acs Applied Materials & Interfaces, 2012, 4, (3), pp. 1614-1619

[7] Minemawari, H., Yamada, T., Matsui, H., Tsutsumi, J., Haas, S., Chiba, R., Kumai, R., and Hasegawa, T.: 'Inkjet printing of single-crystal films', Nature, 2011, 475, (7356), pp. 364-367

[8] Jeong, S., Lee, J.Y., Lee, S.S., Oh, S.W., Lee, H.H., Seo, Y.H., Ryu, B.H., and Choi, Y.: 'Chemically improved high performance printed indium gallium zinc oxide thin-film transistors', Journal of Materials Chemistry, 2011, 21, (43), pp. 17066-17070

[9] Zhao, J.W., Gao, Y.L., Gu, W.B., Wang, C., Lin, J., Chen, Z., and Cui, Z.: 'Fabrication and electrical properties of all-printed carbon nanotube thin film transistors on flexible substrates', Journal of Materials Chemistry, 2012, 22, (38), pp. 20747-20753

[10] Xu, W., Liu, Z., Zhao, J., Xu, W., Gu, W., Zhang, X., Qian, L., and Cui, Z.: 'Flexible logic circuits based on top-gate thin film transistors with printed semiconductor carbon nanotubes and top electrodes', Nanoscale, 2014, 6, (24), pp. 14891-14897

[11] Xu, W., Zhao, J., Qian, L., Han, X., Wu, L., Wu, W., Song, M., Zhou, L., Su, W., Wang, C., Nie, S., and Cui, Z.: 'Sorting of large-diameter semiconducting carbon nanotube and printed flexible driving circuit for organic light emitting diode (OLED)', Nanoscale, 2014, 6, (3), pp. 1589-1595

[12] Kaydanova, T., van Hest, M., Miedaner, A., Curtis, C.J., Alleman, J.L., Dabney, M.S., Garnett, E., Shaheen, S., Smith, L., Collins, R., Hanoka, J.I., Gabor, A.M., and Ginley, D.S.: 'Direct write contacts for solar cells': 'Conference Record of the Thirty-First IEEE Photovoltaic Specialists Conference - 2005' (2005), pp. 1305-1308

[13] Song, K., Jung, Y., Kim, Y., Kim, A., Hwang, J.K., Sung, M.M., and Moon, J.: 'Solution-processable tin-doped indium oxide with a versatile patternability for transparent oxide thin film transistors', Journal of Materials Chemistry, 2011, 21, (38), pp. 14646-14654

[14] Woo, K., Bae, C., Jeong, Y., Kim, D., and Moon, J.: 'Inkjet-printed Cu source/drain electrodes for solution-deposited thin film transistors', Journal of Materials Chemistry, 2010, 20, (19), pp. 3877-3882