# SPICE Compact Modeling for Design of Innovative Integrated Circuits in CEA-Leti

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## ABSTRACT

This paper is an overwiew of the recent compact modeling activities in CEA-Leti. Examples of Verilog-A modeling using the surface potential approach of field effect transistors such as GaN based High Electron Mobility Transistors (HEMTs) are given. Modeling of other devices for design of innovative integrated circuits, such as silicon photonics devices or resistive RAM (RRAM, ReRAM or memristor) memories is also presented.

*Keywords*: SPICE, compact model, AlGaN/GaN HEMTs, power transistor, silicon photonics, RRAM, Verilog-A

### **1 INTRODUCTION**

CEA-Leti in Grenoble, France, is one of the most important research-and-technology organization in Europe, with activities in energy, IT, healthcare, defence and security. CEA-Leti is focused on creating value and innovation through technology transfer to industrial partners. It specializes in nanotechnologies and their applications, from wireless devices and systems, photonics, biology and healthcare.

Numerical simulation of processes and of electron devices has always been a historical activity of the CEA-Leti Simulation and Compact Modeling Laboratory. Using TCAD tools, the lab assisted the developement of siliconbased technologies, leading for example to the optimisation of the fully depleted SOI process for low power applications. In parallel, SPICE compact models were developped and integrated in EDA process design kits (PDK) to assist integrated circuits design.

As new devices and technologies are continuously emerging, it is important to sustain the development of new models, think for example of GaN power transistors, light receivers/transmitters/emitters in photonics or resistive RAM memories, which are not yet available in commercial SPICE simulators. Different examples of innovative SPICE compact modeling are given in this paper.

### **2** COMPACT MODELING OF HEMTS

There is a strong interest for power transistors consisting of AlGaN/GaN HEMTs grown on large diameter substrates, in order to reduce costs, while achieving high performance energy conversion circuits, e.g. in automotive, solar/wind renewable energy production and aerospace applications. Several authors [1] have shown that 200 mm silicon substrates could be used for MOCVD growth of heterostructures, replacing much more expensive and smaller (less than 150 mm) silicon carbide substrates.

In parallel to technology development and optimization, there is also a need for developing compact SPICE models to simulate the electro-thermal behavior of such transistors.

Empirical models, although not developed for GaN HEMTs, are at present used for circuit simulation of RF power devices. However, the need for a more physical approach was expressed in 2013-2014 by industrials from the Compact Modeling Coalition (CMC/Si2) [2]. The same need was expressed in the past ten years for bulk MOSFETs, leading to the standardization of the PSP and HiSIM models and allowing precise simulation of very advanced CMOS technologies. As technology continues to progress according to Moore's law, models for FDSOI transistors and FinFET were then developped.

A physical compact modeling approach is preferred as it guarantees a better adaptability based on technological and physical parameters. Surface-potential or charge based models are now prefered to threshold voltage based models as discontinuities of first and n<sup>th</sup> derivatives between different regimes no longer exist and simulation convergence is improved.

In this section we briefly present the physics based compact model called Leti-HSP (acronym for HEMT Surface-Potential model) [3-5]. It is based on the analytical calculation of the Surface-Potential (SP) at the AlGaN/GaN interface. A cross-sectional view of an AlGaN/GaN HEMT is shown in Fig. 1.



Substrate (Si, Sapphire (Al<sub>2</sub>O<sub>3</sub>), SiC, ...)

#### Fig. 1: Cross-sectional view of an AlGaN/GaN HEMT

Fig. 2 shows the Leti-HSP model flow. If not given as an input parameter, the offset voltage  $V_{off}$  is calculated considering thickness and composition of the  $Al_xGa_{1-x}N$ layer.  $V_{off}$  depends also on spontaneous and piezoelectric polarization effects. To adjust  $V_{off}$ , donors (e.g. Si atoms) could be introduced by ion implantation, but their ionization in refractory III-nitride compounds is incomplete and depends on temperature.  $V_{off}$  is allowed to change with  $V_{DS}$  due to the Drain-Induced Barrier Lowering (DIBL) effect.



#### Fig. 2: Leti-HSP compact model flow

The next step is to describe electrostatics and quantum effects and to calculate the 2-DEG sheet charge density. To do this, Schrödinger equation in 2D triangular approximation and Poisson equation has to be solved. This leads to a system of equations which is traditionally solved by a self-consistent numerical method. However, such a resolution is not suitable for a circuit simulator as it is too costly in computation time. A tiedous mathematical developement allows to calculate analytically the Fermi level  $E_F$ . Knowing the Fermi potential, the surface potential  $\Phi_S$  can be calculated as a function of the "channel" potential  $V_C$ , in particular at the source ( $V_C=V_S, \Phi_S=\Phi_{SS}$ ) and at the drain ( $V_C=V_D, \Phi_S=\Phi_{SD}$ ), for a given gate voltage  $V_G$ . We check that our expressions are valid even for very high  $V_{DS}$ , up to 1 kV.

Before proceeding to drain current calculation Id, mobility, velocity saturation effect and channel length modulation have to be calculated. Mobility attenuation due to the transverse electrical field is obtained after application of the Gauss theorem at the AlGaN/GaN interface. This also necessitates to calculate the surface potential at a midpoint in the channel  $\Phi_{SM} = 0.5$  ( $\Phi_{SS} + \Phi_{SD}$ ).

Series resistances and self-heating effects (SHE) may strongly affect the drain current. The channel temperature increase is calculated and all parameters depending on temperature are recalculated. Two models of SHE are included:

 $1\,-\,A$  simple model where an empirical thermal resistance  $R_{th}$  is assumed as a lumped element for the power dissipation,

2 - A more physical approach that models the heat diffusion from channel through a substrate of thickness  $t_{sub}$  whose backside is held at constant temperature  $T_0$  acting as a heat sink. The actual channel temperature could be calculated in substrates of different thermal conductivity, e.g. Si, sapphire or SiC.

The gate charge Qg, is first calculated. Source and drain charges (Qs, Qd) are then evaluated using the Ward-Dutton partitioning scheme. If needed, nine intrinsic capacitances could be calculated as derivatives of the terminal charges. This treatment allows strict charge conservation during transient circuit simulation and requires no fitting parameters.

To the HSP intrinsic core model we must add extrinsic effects. Different source or gate field plates are always present in GaN technologies to maintain the electrical field lower than the breakdown field and help sustain high voltages for applications up to 1.2 kV. Their impact on capacitance are added in transistor charge conservation. Another severe effect in GaN transistors is the presence of traps responsible of electrical shifts and current collapse. These effect is captured through V<sub>off</sub> or R<sub>on</sub> shifts.

In ref. [5], we have shown that this physical approach constitutes an interesting tool for technological development and optimization of AlGaN/GaN HEMTs.

The model has been implemented using Verilog-A and tested in the ADS simulator from Keysight and in the Eldo simulator from Mentor Graphics.

Leti-HSP has been selected during the first two phases of GaN model standardization by the CMC/Si2 GaN subcommittee. During the second phase four models were in competition: the Angelov model [6], the ASM model from University of California at Berkeley [7], the MIT Unified Virtual Source GaNFET (MVSG) model from Massachusetts Institute of Technology [8] and the Leti-HSP model. Only two models were retained for the third phase: the ASM and MVSG. Both models are able to reproduced physics of power GaN transistors, both for power RF amplification and switching applications. At the end of the fourth phase the selected model(s) will be available in commercial simulators and also in parameter extraction tools.

## 3 COMPACT MODELING OF SILICON PHOTONICS DEVICES

There is a growing demand for efficient CAD tools for modeling and designing silicon photonics devices and circuits. However, relatively few publications on modeling of photonics devices and their incorporation in a standard electronic design environment were presented [9]. Models developed in the Verilog-A behavioral language have the advantage of allowing the device to be used in many commercial SPICE circuit simulators.

Previous works use only two quantities to represent the optical signal: Power (in Watt) and Phase (in radian). However to deal with future photonics devices in which light could be polarized along two axis, we define an optical bus consisting of 9 different lines. The first five lines are:

0: Real part of the complex amplitude of the optical field for the X-axis polarization (normalized in  $W^{1/2}$ ),

1: Imaginary part of the complex amplitude of the optical field for the X-axis polarization (normalized in  $W^{1/2}$ ),

2: Real part of the complex amplitude of the optical field for the Y-axis polarization,

3: Imaginary part of the complex amplitude of the optical field for the Y-axis polarization,

4: Wavelength (m).

To account for the bidirectional character of some devices, lines 5-8 are added when light is coming from right using our convention for incident light direction. They represent the same quantities than lines 0-3, respectively. Besides representing a more physical approach, the bus description, which is commonly used in electrical busses such as IEEE-488, allows an important simplification in the schematics view of photonic devices (Fig. 3).





We developed different models of photonic devices. These devices could be purely passive and designed with a SOI technology (straight WG, WG crossing, MMI coupler, beam splitter, combiner). Active photonic devices, such as Mach-Zehnder interferometer modulators (MZIM), without or with a heater, and germanium-on-silicon photodiodes (pin diode biased at a reverse voltage), are also modeled. To monitor optical power or phase, a virtual power and phase meter (PPM) is used. To account for parasitics due to interconnects and SOI substrate, macro models are built for high frequency operation. Fig. 4 presents some available devices in our SPICE tool box.



Fig. 4: Silicon photonics tool box

To create photonics integrated circuits, these models are then incorporated in a process design kit (PDK) which is a process specific library designed to work with the Cadence Design Systems environment. This PDK includes technology files (LVS, DRC, SPICE models), device symbols, Component Description Format (CDF) and parameterized cells (Pcells) as in a standard EDA framework for CMOS technologies (Fig. 5). SPICE circuit simulation of ASPICS (Application Specific PhotonIC's) is then possible.



Fig. 5: Photonics PDK

## 4 COMPACT MODELING OF RESISTIVE MEMORIES

Resistive Random Access Memory (RRAM or ReRAM) is a type of non-volatile memory. Two kinds of RRAM can be distinguished: CBRAM (Conductive Bridge Random Access Memory) and OxRRAM (Oxide Resistive Random Access Memory).

They are made of solid electrolyte sandwiched between two electrodes and work by changing the resistance of a material. For CBRAM, resistance switching is induced by electro-chemically driven growth of a conductive filament and known as set. The destruction of this filament is named reset. Consequently, two states, a 'LRS' (Low Resistive State = set) and a 'HRS' (High Resistive State = reset) are possible, see figure 6 for the set operation.



Fig. 6: Creation of the conductive filament thanks to silver ions for the set operation.

For OxRRAM, it is also a filamentary conduction mechanism based on the breaking oxygen bonds and the migration ions under high electric fields and elevated temperature. Figure 7 shows the instance of a set operation.



Fig. 7: For the set operation, oxygen ions migrate towards the top electrode under high electric field and elevated temperature.

CBRAMs and OxRRAMs are promising breakthroughs due to their permanent retention, low power consumption, ease of integration in the back end of a logic process and low cost. Thus, they are very interesting for the design community as well.

To use these devices in innovative circuits, compact models are mandatory. A compact model should be accurate, fast and robust. We developped a continuous physical compact model for CBRAM cell, implemented in Verilog-A [10] and integrated in simulation tools. Main advantage of this approach is its robustness and flexibility for adding effects as multilevel aspect. The model is based on Mott-Gurney equation and also includes multilevel and statistical dispersions of HRS and LRS resistances (Fig. 8), set and reset switching times. The accuracy of the compact model is demonstrated by comparing with measurements. This model was largely used in circuit design [11].



Fig. 8: Corner plot for optimal programming window, with statistical data from experiment (black circle) and simulation (red circles and blue triangle).

A compact model for OxRRAM is in progress.

## 5 CONCLUSION

This paper has presented some of current SPICE compact modeling topics in CEA-Leti. These models are essential in bridging the gap between emerging technologies and design of innovative integrated circuits.

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