Room-temperature printing of thin-film devices for flexible electronics

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ABSTRACT

Printing of semiconductor devices under ambient atmospheric conditions is a promising method for large-area, low-cost fabrication of flexible electronic products. However, processes conducted at temperatures greater than 150 °C typically are used for printed electronics, which prevents use of a common flexible substrate because of the distortion caused by heat. Here we propose "room-temperature printed electronics", which allows thin-film electronic devices to be printed at room temperature without application of heat. The development of π-junction gold nanoparticles as the electrode material permitted room-temperature deposition of a conductive metal layer. Room-temperature patterning methods also were developed for the Au ink electrodes and an active organic semiconductor layer, which enables fabrication of organic thin-film transistors through room-temperature printing. The devices printed at room temperature exhibited average field-effect mobilities of 7.9 and 2.5 cm^2 V^{-1} s^{-1} on plastic and paper substrates, respectively. These results suggest that this fabrication method is very promising as a core technology for low-cost and high-performance printed electronics.

Keywords: printed electronics, flexible electronics, organic thin-film transistors, organic semiconductor, nanoparticles

1 INTRODUCTION

Printed electronics is an emergent subject for the low-cost and large-area fabrication of flexible electronic devices. Fully-printed organic thin-film transistors (OTFTs) using soluble organic semiconductors is a particularly promising fabrication method that offers lower production costs, reduced energy consumption, and a smaller environmental burden [1-6]. On the other hand, the high processing temperature of ~150 °C is one of the critical problems, which prevents accurate and high-resolution patterning on a common flexible substrate due to the its distortion by heat. This problem becomes more significant as the production size increases.

This report describes the room-temperature (RT) preparation of fully-printed OTFTs involving the formation and patterning of all layers of the devices [7]. To achieve this RT process, novel Au NPs, which exhibit low resistivity of ~9×10^{-6} Ω cm even after RT deposition and drying without use of an annealing process, were developed. High-resolution patterning methods also were developed for the Au NP ink and an organic semiconductor using the surface wettability difference. Thus, high-resolution patterning of OTFT devices on a non-heat-resistant substrate was achieved by RT printing. The Au NP electrodes also improved charge injection into the semiconductor layer, resulting in an average field-effect mobility (μ_{FET}) of 7.9 cm^2 V^{-1} s^{-1} in the OTFT devices formed on a plastic substrate. This value is ten times higher than that of conventional a-Si TFTs and even comparable to that of InGaZnO (IGZO) TFTs, which warrants use of the printed OTFTs in practical high-end display devices. The RT process also enables printing of OTFT devices on paper, with a μ_{FET} of 2.5 cm^2 V^{-1} s^{-1}. This proposed technique has potential applications to other thin-film devices, such as organic photovoltaic cells, and may become a fundamental technology in future printed electronics.

2 EXPERIMENTAL

2.1 π-junction Au Nanoparticles

The critical difficulty in achieving a process for RT printed electronics is the high-temperature annealing process required for metal electrode deposition using metal NP ink. A conventional metal NP ink contains a non-conductive material as the ligand. High-temperature annealing is required to remove it and sinter the metal cores to obtain a conductive metal film. Therefore, we developed π-junction Au NPs for the RT printing of the metal electrodes [8,9]. The schimatic structure of the Au NPs are shown in Fig. 1(a). The Au NPs possess a metal core surrounded by aromatic molecules as the conductive ligand, which is the biggest difference between the new inks and conventional metal NP inks. In the π-junction NPs, orbital hybridization between the π orbitals of the aromatic ligand and orbitals of the metal core improves charge transport among the NPs. Thus, conductive film can be obtained by RT deposition of the ink without removal of the ligand by annealing. A scanning electron microscopic image of the Au NPs deposited on a substrate is shown in Fig. 1(b). The Au NPs clearly have a spherical shape that is maintained in the film. However, it exhibits low resistivity of ~9×10^{-6} Ω cm, which is of the same order of magnitude as that of pure Au of 2.2×10^{-6} Ω cm, without the sintering process because of the smooth charge transport among NPs through the

conductive ligands. Thus, the Au NP film can be used as the electrode material for the RT printing method.

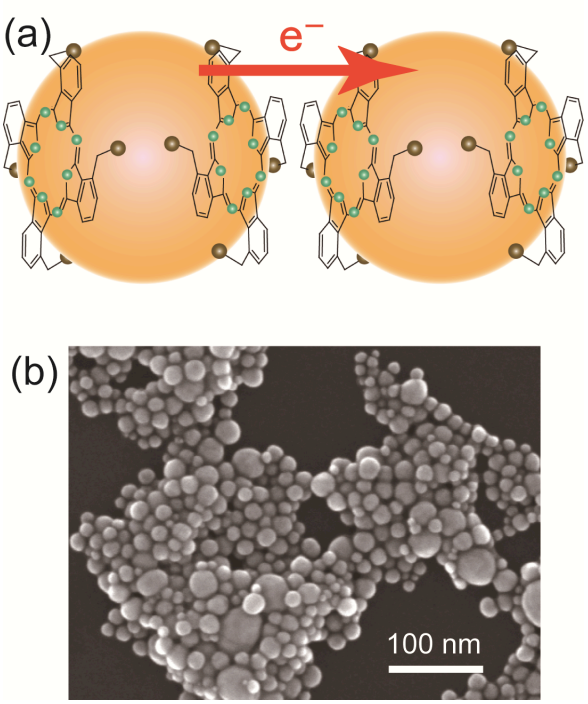

Figure 1: (a) Schematic illustration of π-junction Au NPs. The metal core is surrounded by aromatic molecular ligands. (b) Scanning electron microscope image of Au NPs deposited on a substrate.

2.2 Fabrication of OTFT Arrays

For fabrication of the printed OTFTs using the Au NP ink, a stack of four layers, including source/drain, organic semiconductor, gate dielectric, and gate electrode layers, was prepared to complete the devices, and the RT process was employed for all layers (Fig. 2).

A surface selective deposition method was used to pattern the Au NP ink on the substrate [7]. For this method, selective regions on the hydrophobic polymer surface were exposed to vacuum ultraviolet (VUV) light to transform the surface into a hydrophilic, wettable surface. The VUV exposure under air generates oxygen radicals and ozone molecules, which cause chemical bond dissociation at the polymer surface and render the region hydrophilic, resulting in patterned wettability. The VUV irradiation system was composed of a Xe excimer lamp as the VUV light source (wavelength of 172 nm) and a mask aligner, which allows selected regions on the surface to be exposed to the VUV light through a photo mask under ambient atmospheric conditions. The Au NP ink was deposited by spreading the ink onto the patterned surface using an applicator to obtain the patterned metal layer. The highest resolution achieved by this method was 10 μm for a line or space.

Polyethylene naphthalate (PEN) with a surface planarizing layer of parylene was used as the flexible plastic substrate. The source/drain electrodes, an organic semiconductor layer, and gate electrodes were fully patterned using a solution-based printing method at RT. First, the source/drain electrode patterning was performed on the hydrophobic substrate surface. The source/drain regions on the surface were exposed to VUV irradiation through a photo mask under ambient atmospheric conditions to render the exposed surface area hydrophilic. After surface wettability patterning, the Au NP ink was applied to the surface, resulting in a pattern of Au ink only on the hydrophilic regions. The Au ink dried in several seconds at RT, and the source/drain electrode layer was obtained using a RT process.

Then the organic semiconductor layer was added onto the channel region of the devices using a two-step printing processes, screen printing and solution casting. On the source/drain electrode layer, first a fluorinated polymer layer of Cytop (Asahi Grass Co. Ltd.) was formed around the channel region of OTFTs by screen printing. Then, the Cytop was dried at RT without annealing, resulting in a uniform polymer layer 120 nm thick. The lyophobic nature of the fluorinated polymer surface inhibits deposition of organic semiconductor. Therefore, it acts as a guide for the organic semiconductor solution. Semiconductor layer deposition was performed next, through simple drop casting of 0.5 wt% chlorobenzene solution of dioctylbenzothienobenzothiophene (C_8-BTBT) [10] into the lyophilic channel region. Because of the highly repellent nature of the Cytop surface, the semiconductor solution was deposited only on the channel regions, and a patterned organic layer was formed after solvent evaporation. The high boiling point solvent allows formation of a uniform semiconductor layer with relatively large grain size of ~100 μm.

After the formation of gate dielectric layer of hydrophobic polymer, the top-gate electrode layer was patterned as the last step, accomplished by VUV exposure. The gate electrode regions on the gate dielectric were exposed to VUV light through a photo mask to render them

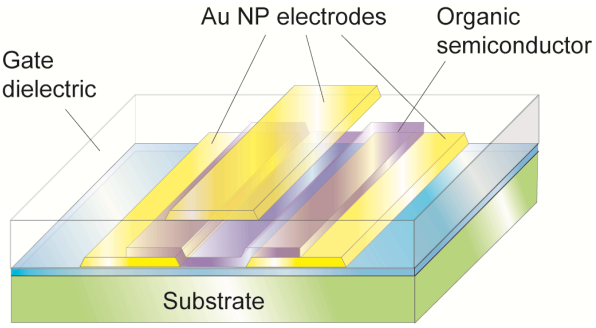

Figure 2: Structure of OTFT devices fabricated by the RT printing process.

hydrophilic, followed by application of Au NP ink using the applicator to selectively deposit it only onto the hydrophilic regions. The Au NPs were dried at RT without application of heat.

3 RESULTS AND DISCUSSIONS

Results of RT printing of OTFT arrays on the flexible plastic substrate are shown in Fig. 3. Since a flexible material was used for all of the layers, the array obtained was a fully flexible OTFT array, as shown in Fig. 3(a). The optical micrograph of the fully-printed OTFT array obtained by RT printing is also shown in Figure 3a. The electrode and semiconductor layers were completely patterned for complete isolation among the devices, which is essential for reducing gate leakage current and inter-device crosstalk (Fig. 3(b)).

The results of electrical characterization for RT-printed OTFTs are shown in Fig. 3(c) and 3(d). The nonlinear increase in drain current in the low-drain-voltage region in the output characteristics (Fig. 3(c)) was attributed to the relatively high contact resistance at the metal/semiconductor interface. Since C_8-BTBT is wide bandgap material and the film has a deep valence band (VB) level (EV = 5.7 eV), a high charge injection barrier can exist at the metal/organic interface due to the energy mismatch between the Fermi level of the Au NP electrodes and the VB of the C_8-BTBT film. In contrast, the drain current in the high-drain-voltage regions shows saturation characteristics, which confirms an ideal MOSFET operation. Figure 3d shows that hysteresis-free transfer characteristics were achieved with a steep increase in drain current in the sub-threshold region. Gate leak current was substantially reduced by complete patterning of the electrode and semiconductor layers, which allowed an on-off ratio of 10^6. The average μ_{FET} and threshold voltage (V_T) of the fully-printed OTFTs were 7.9 ± 1.1 cm^2 V^{-1} s^{-1} and 1.1 ± 0.4 V, respectively. The variation in these two values may be related to the polycrystalline structure of the C_8-BTBT film and the high contact resistance of the OTFTs as reflected in the nonlinear rise in drain current shown in Fig. 3(c). For further improvement in performance uniformity of the device characteristics, reducing this contact resistance is necessary.

The proposed fabrication method of organic electronics at RT enables formation of devices on the surfaces of heat-sensitive materials because of the low fabrication temperature. To confirm the superiority of the extremely low-temperature fabrication process, OTFTs were fabricated using paper as the substrate. A commercially available photo paper (home inkjet printer paper) was selected as the heat-sensitive substrate. This paper degrades at temperatures of approximately 60 °C. Thus, only a RT process could be used to fabricate fully-printed devices on the paper.

First, the logo of our institute was printed on the paper surface using an inkjet printer (Fig. 4(a)) to confirm the

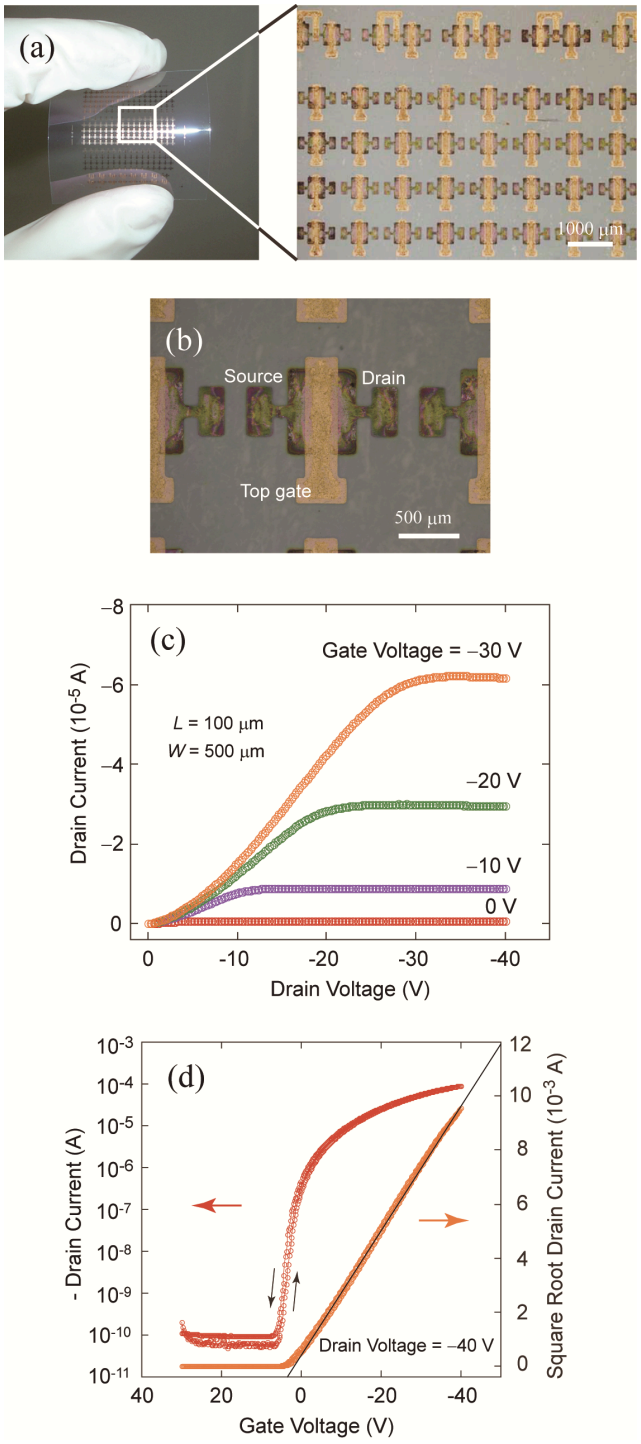

Figure 3: OTFT devices fabricated using the RT printing process on a plastic substrate. (a) Flexing the printed OTFT arrays on the plastic substrate (left). Substrate size was 40 × 40 mm^2. An optical microscope image of the OTFT array (right). (b) Optical microscope image of the individual device. The electrode and organic semiconductor layers are fully patterned to reduce the off current and cross-talk among the devices. (c) Typical output characteristics of the RT printed OTFT. (d) Typical transfer characteristics of the OTFT device.

identity of the substrate as paper. Then the surface was passivated with a parylene layer 3 μm thick, which provided a hydrophobic surface on the paper substrate and reduced surface roughness. Similar procedures used for the plastic substrate also were used to form the devices on the paper. The lines of Au NPs for the source/drain electrodes were patterned by the selective deposition process. Then, an organic semiconductor layer of C_8-BTBT was patterned in the channel region using the combination of screen printing of a guide layer and solution casting of the semiconductor to the defined regions. The polymer gate dielectric layer was formed by spin-coating, followed by drying at RT. Finally, gate lines were drawn by the selective deposition method, and OTFT arrays were successfully formed on the paper substrate. Typical transfer characteristics of the fully-printed OTFTs on paper are shown in Fig. 4(d). Stable operation of the OTFTs was realized without hysteresis behavior. The average μ_{FET} of the fully-printed OTFTs on the paper was estimated to be 2.5 cm^2 V^{-1} s^{-1}.

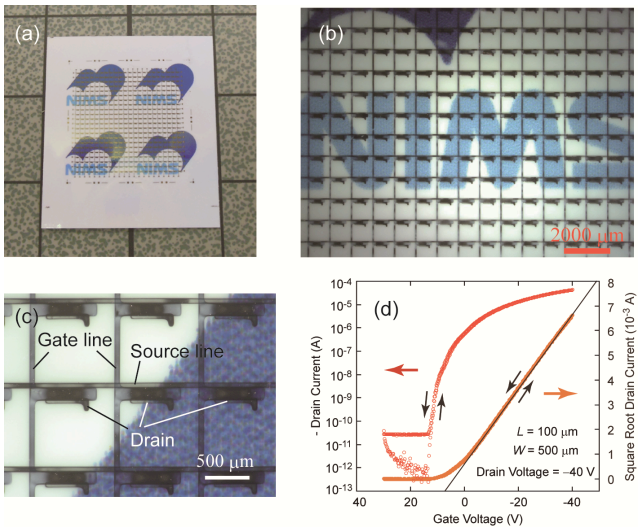

Figure 4: An OTFT active-matrix array assembled on a paper substrate using the RT printing process. (a) OTFT array on the paper substrate. The size of the paper was 40 × 50 mm^2. (b) Optical microscope image of the OTFT array fabricated using the RT printing technique. (c) Enlarged optical micrograph of the RT printed OTFT devices on paper. (d) Typical transfer characteristics of the printed OTFTs on paper.

4 CONCLUSIONS

Flexible electronic devices were printed at RT using π-junction Au NP ink as the electrodes, which demonstrated the usefulness of this method as a core technology for flexible printed electronics. The low processing temperature enables use of non-heat-resistive materials as a substrate. The OTFT devices printed at RT had average values for μ_{FET} of 7.9 and 2.5 cm^2 V^{-1} s^{-1} on plastic and paper substrates, respectively, with minimal hysteresis behavior and a V_T near zero. The high μ_{FET} value obtained from the RT-printed OTFTs is comparable to that of IGZO TFTs. In addition, RT printing may be applied to a broader range of thin-film electronic devices, such as light-emitting devices and photovoltaic cells.

The ability to print plastic electronic devices at RT is expected to promote major advances in electronics production technology, because of several key advantages. Thermal damage is avoided due to the RT process, which allows the use of many flexible substrate types. A flexible substrate is necessary for large-scale roll-to-roll fabrication of devices, thus this RT process provides a method for future printed electronics. Device fabrication based on this simple printing process under ambient conditions is a low-cost and high-throughput process. This advantage can be enhanced by increasing production size and volume. Finally, the methods used to produce the high-performance devices described here can be applied to other practical electronic products. Mass production of devices, such as fully flexible electronic papers or displays, becomes possible because of the flexibility and high mobility of the printed OTFTs. Thus, this RT printing process is a promising method as a core technology for future semiconductor electronics. One can find the detailed report in Ref. [7].

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