Wafer-Scale Planarization using Location Specific Gas Cluster Ion Beam (GCIB) in Advanced CMOS Logic Technology

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ABSTRACT

In sub-14nm advanced CMOS logic technology, controlling wafer-scale planarization or uniformity became tremendously critical. This is mainly due to the CMOS integration scheme where chemical mechanical polishing (CMP) is used to create the transistor gate. The precise gate height control is extremely important since any within wafer or within chip non-uniform gate height can cause degradation in device performance and yield. Especially, the technology requirement in the wafer-scale planarization at the advanced CMOS technology is beyond the capability a conventional CMP process can deliver. This technology limitation initiated the need for alternative integration scheme or planarization technology. The wafer-scale planarization using location specific gas cluster ion beam (GCIB) is considered as a potential technology to meet this stringent requirement.

In this paper, the fundamentals of GCIB technology are explained and the potential applications in CMOS integration are addressed.

Keywords: gas cluster ion beam, chemical mechanical polishing, planarization, location specific process, uniformity

1 INTRODUCTION

GCIB is a focused beam enabled by clusters of gas molecules and can remove surface material in molecular scale. This gas cluster is created by the high pressure gas mixture going through volume expansion and condensation caused by adiabatic expansion. Then, the gas clusters are ionized and accelerated to the wafer surface. Prior to its impact on wafer surface, the bream is neutralized to prevent the device damage by electro-static discharge (ESD). The gas clusters bombard into the molecules of the wafer surface and remove the surface material by physical and chemical means. The amount of material removed is controlled by the total energy applied on the gas cluster and the composition of gas cluster molecules. Even though the total amount of energy is high, the energy on an individual cluster molecule is low and the gas cluster does not cause any sub-surface damage. The depth of material removed by a single cluster can range from 2nm to 20nm, Figure 1. The temperature of the surface within GCIB impact zone can go up to 10,000 °C, but the duration is extremely small which is less than 10 pico seconds and the rest of material remains as in room temperature. [1]

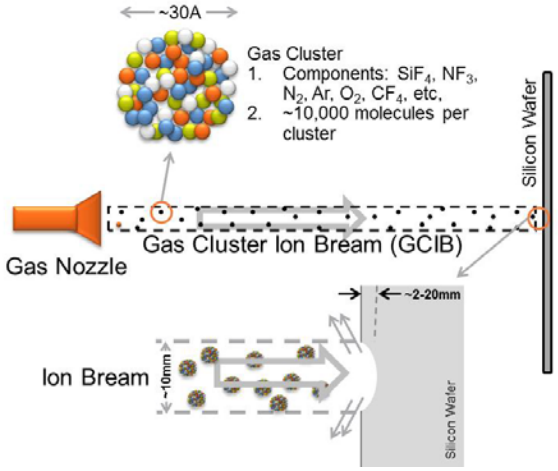

Figure 1: Gas Cluster Ion Beam (GCIB)

Location Specific Processing (LSP) can improve the within-wafer uniformity significantly better than the best profile controlled by the CMP process, Figure 2. Each wafer is measured using on-board metrology as a pre-process measurement. This pre-measurement determines the location of the 'non-uniformity' on the wafer surface. The duration of the ion beam at the specific location on the wafer surface is manipulated by the pendulum motion from the wafer chuck. While the wafer is oscillated back and forth from this pendulum motion at up to 150 cm/s maximum speed, it also moves up between scans by 1-2 mm typical pitch. This movement creates a complete wafer scanning motion and LSP map, Figure 3.

The LSP algorithm makes the wafer stay longer when the gas cluster ion beam hits on the non-uniform location by making the wafer scanning motion slower. The GCIB process recipe is updated for every wafer from the pre-measurement data by using automatic process control (APC) algorithm.

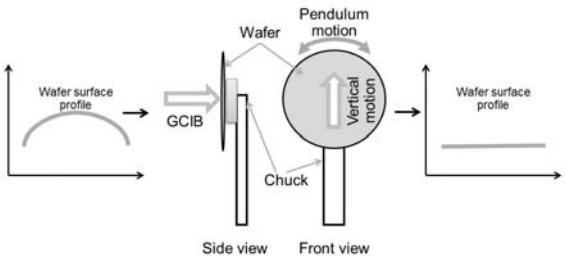

Figure 2: Location Specific Process (LSP)

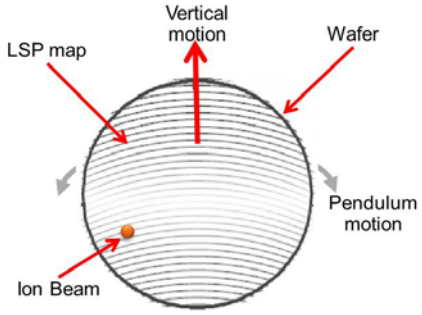

Figure 3: LSP Map

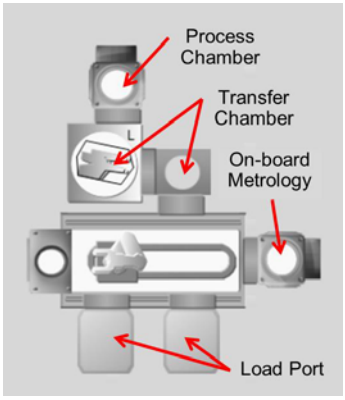

Figure 4: GCIB system

The wafer is picked up from load port and moves to on-board metrology for pre-measurement, Figure 4. After the measurement, the wafer moves to process chamber via wafer transfer chambers to control and maintain the appropriate vacuum level inside of process chamber. After GCIB process, the wafer moves back to the load port. The wafer can be re-measured at on-board metrology to check post GCIB film thickness.

2 GCIB APPLICATION

2.1 Dummy Poly Gate Planarization

One of the potential applications of GCIB in advanced CMOS logic technology is the dummy poly gate planarization for FinFET device, Figure 5.

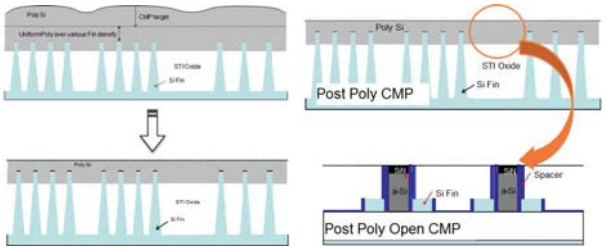

Figure 5: Dummy Poly Gate Planarization

Integration requirement for sub-10nm logic technology brings significant challenges in chemical mechanical polishing (CMP) process. The GCIB with LSP technology can provide the process enablement as a supplemental step to CMP process to ensure the wafer uniformity within required process specification.

In the fabrication of the FinFET device, the dummy poly gate is deposited on the top of FIN structure. In order to planarize this polysilicon surface, several CMP steps and 'multiple' other process steps are required. This is due to the strict process specification we need to meet to control the height of the dummy poly gate in within-die and within-wafer scale. The polysilicon height after poly CMP and planarization step is directly transferred to dummy poly gate and, eventually, metal gate in replacement metal gate module. Therefore, it is absolutely critical to control the height of the remaining polysilicon film after CMP and other planarization steps.

The proposed idea is to planarize the polysilicon film by using only poly CMP and GCIB step. This makes the overall poly planarization integration scheme simplified while maintaining within-die and within-wafer poly height specification.

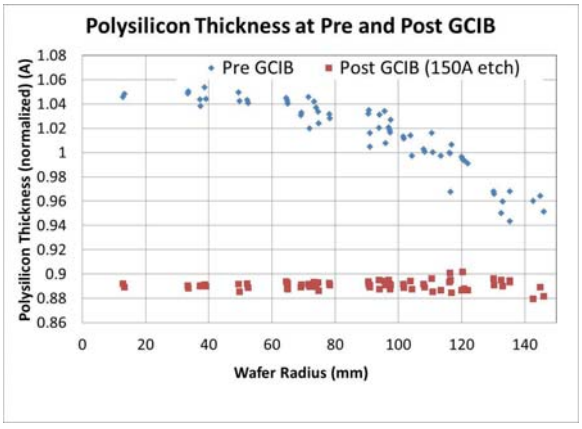

Figure 6: Poly Planarization by LSP-enabled GCIB

After polysilicon deposition, the wafer was processed using a conventional poly CMP process to make initial planarization of polysilicon film. The within-wafer non-uniformity at post CMP step can range up to 100-150A. The same wafer was measured prior to GCIB process in order to create specific LSP map. The wafer at post GCIB process showed 7-10x improvement in within-wafer non-uniformity. The LSP algorithm was able to provide good and stable uniform wafer surface.

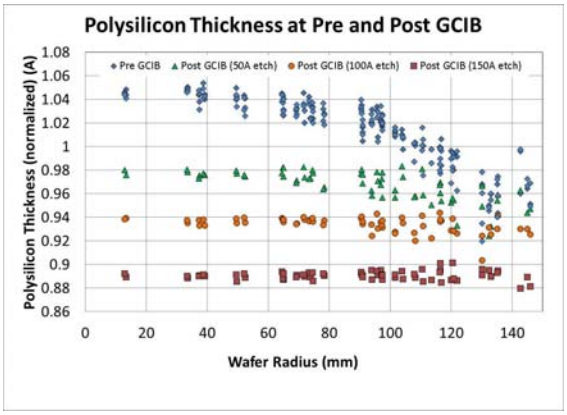

Figure 7: Uniformity Improvement with Etch Amount by GCIB

The amount of material to remove can be determined by the incoming uniformity range of the film we need to planarize. With gradual change in profile, the amount of thickness to remove, in general, corresponds to the incoming non-uniformity. The higher the non-uniformity of the incoming film is, the more the amount of material GCIB needs to remove, Figure 8. The requirement for the larger amount of material removal can decrease the process throughput from the longer process time.

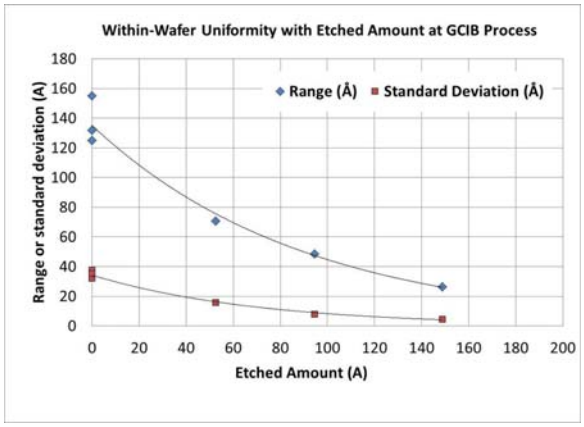

Figure 8: Uniformity Improvement with Different Etched Amount by GCIB

3 GCIB FOR SEMICONDUCTOR MANUFACTURING

The surface roughness of oxide surface was compared with GCIB-processed oxide wafer. Due to the nature of material removal process by bombardment from gas molecule cluster, a certain amount of surface roughness can be expected. However, SEM analysis showed almost equivalent surface roughness on oxide surface with and without GCIB process.

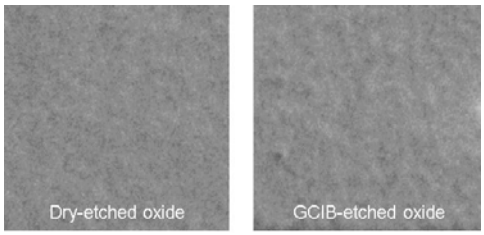

Figure 9: SEM Images of oxide surface

In order to verify the manufacturability of GCIB process, multiple process marathon tests and daily process qualification have been performed, Figure 10.

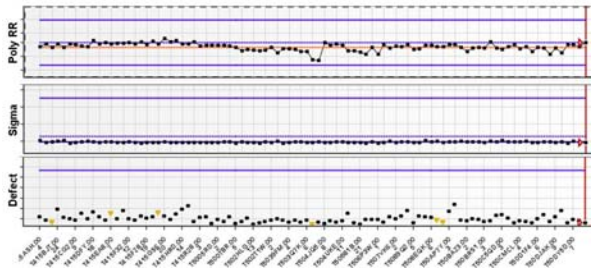

Figure 10: Process Qualification for Removal Rate and Defectivity

The stable process control of GCIB was also demonstrated from the extended process marathon test and daily qual. Due to the advanced controllability at GCIB process and system, the specification of the daily qualification for the removal rate and the defectivity was tightened far more than one in the conventional CMP process qualification. Among the three process parameters, the sigma of the surface uniformity showed extremely consistent controllability. Overall variation was less than 5A.

4 CONCLUSION

The gas cluster ion beam (GCIB) process was explained for its fundamentals, its application in semiconductor fabrication process, and its manufacturability. It showed excellent profile control capability which is beyond what conventional CMP can achieve.

After CMP process started to be implemented to fabricate the metal gate in the advanced technology node, the requirement of the within-wafer and the within-die uniformity became extremely tightened. Particularly, the stop-in-film CMP process may not be able to achieve such a

tight uniformity specification. In a certain integration scheme, additional process steps are required to achieve this tightened uniformity specification. GCIB can be an alternative process option to achieve such tightened within-wafer uniformity.

Even though GCIB cannot replace CMP due to its inability in planarizing the incoming surface topography, it can be a supplemental process to help CMP in order to deliver stringent wafer-scale uniformity. Due to the exceptional capability to achieve good wafer-scale uniformity, its application can expand beyond dummy silicon planarization application addressed in this publication.

REFERENCES

[1] N. M. Russell, *et. al* 'Precision integrated thickness control with gas cluster ion beam etch', Proc. SPIE 9054, Advanced Etch Technology for Nanopatterning III, March 2014.