Simulation of Current Slump Removal in Field-Plate GaAs MESFETs

A. Nomoto, Y. Sato and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan, horio@sic.shibaura-it.ac.jp

ABSTRACT

Two-dimensional transient analysis of field-plate GaAs MESFETs is performed by considering surface states in the region from the gate toward the drain. The field-plate length L_{FP} and the thickness of SiO_2 passivation layer d are varied as parameters. It is shown that the drain lag and current slump are reduced by introducing a field plate longer than the length of surface-state region L_S, but they are not removed completely when d is thick. It is clearly shown that when d becomes very thin ($\leq$ 0.02 μm), the lags and current slump are completely removed for L_{FP} longer than L_S. By carefully examining the L_{FP} dependence for d = 0.02 μm, it is found that they are completely removed even if L_{FP} is comparable to L_S.

Keywords: GaAs FET, current slump, surface state, drain lag, gate lag

1 INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [1,2]. This is called drain lag or gate lag, and undesirable for circuit applications. Slow transients indicate that dc and RF current-voltage (*I-V*) curves become quite different, resulting in lower RF power available than that expected from dc operation [3]. This is called current slump. These phenomena occur due to surface states and/or bulk traps [1-5]. Experimentally, the introduction of field plate like Fig.1 is shown to reduce the lags and current slump [3,6,7]. However, few simulation studies on field-plate structures have been made, although GaN-based FETs with bulk traps are studied [8]. In previous works [9,10], we made two-dimensional analysis of field-plate GaAs MESFETs including surface states, and showed that surface-related lags and current slump could be reduced by introducing a field plate and that in some cases, they were completely removed. In this work, we have further studied the field-plate effects and studied the condition when the lags and current collapse are completely removed.

2 PHYSICAL MODELS

Figure 1 shows a device structure analyzed in this study. The gate length L_G is typically set to 0.3 μm. The gate

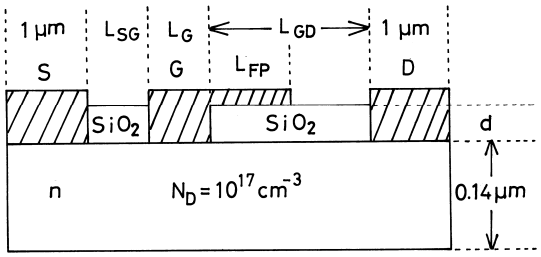

Figure 1: Device structure analyzed in this study.

electrode extends on to SiO_2 passivation layer. This is called a field plate. The field-plate length L_{FP} is varied as a parameter. The thickness of SiO_2 layer d is also varied. Relatively high densities of surface states are considered only at the drain edge of the gate region. This situation can occur after the device has been stressed or due to device degradation. Here the length of surface-state region L_S is set to 0.4 μm from the gate edge toward the drain. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities (N_{SD}, N_{DA}) are typically set to 6×10^{19} cm^{-3} (3×10^{12} cm^{-2}). As for their energy levels, the following case based on experiments is considered as in a previous work [9,10]: E_{SD} = 0.87 eV, E_{SA} = 0.7 eV, where E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. In this case, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap.

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels [11-14]. These are expressed as follows.

1) Poisson's equation

$$\nabla^2 \psi = -\frac{q}{\varepsilon}(p - n + N_D + N_{Di} + N_{SD}^{+} - N_{SA}^{-}) \qquad (1)$$

2) Continuity equations for electrons and holes

 TechConnect Briefs 2015, TechConnect.org, ISBN 978-1-4987-4730-1

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - (R_{n,\mathrm{SD}} + R_{n,\mathrm{SA}}) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - (R_{p,\mathrm{SD}} + R_{p,\mathrm{SA}}) \quad (3)$$

where

$$R_{n,\mathrm{SD}} = C_{n,\mathrm{SD}} N_{\mathrm{SD}}^{+} n - e_{n,\mathrm{SD}} (N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) \quad (4)$$

$$R_{n,\mathrm{SA}} = C_{n,\mathrm{SA}} (N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) n - e_{n,\mathrm{SA}} N_{\mathrm{SA}}^{-} \quad (5)$$

$$R_{p,\mathrm{SD}} = C_{p,\mathrm{SD}} (N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) p - e_{p,\mathrm{SD}} N_{\mathrm{SD}}^{+} \quad (6)$$

$$R_{p,\mathrm{SA}} = C_{p,\mathrm{SA}} N_{\mathrm{SA}}^{-} p - e_{p,\mathrm{SA}} (N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) \quad (7)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) = R_{n,\mathrm{SD}} - R_{p,\mathrm{SD}} \quad (8)$$

$$\frac{\partial}{\partial t} N_{\mathrm{SA}}^{-} = R_{n,\mathrm{SA}} - R_{p,\mathrm{SA}} \quad (9)$$

where N_{SD}^{+} and N_{SA}^{-} are ionized densities of surface deep donors and surface deep acceptors, respectively. C_n and C_p are electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are electron and hole emission rates of the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level.

These equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_{D} and/or the gate voltage V_{G} are changed abruptly.

3 SLOW CURRENT TRANSIENTS (DRAIN LAG)

Figure 2 shows calculated drain-current responses of GaAs MESFETs considering surface states when V_{D} is lowered abruptly from 10 V to V_{Dfin}, where V_{G} is kept constant at 0 V. Here, the surface-state density is 3×10^{12} cm^{-2}, and the surface-state length L_{S} is 0.4 μm.. Fig.2(a) shows a case without a field plate, and Fig.2(b) shows a case with a field plate (L_{FP} = 1 μm). The thickness of SiO_2 layer d is 0.1 μm. In both cases, the drain current I_{D} remains at a low value for some periods (10^{-10} – 10^{-1} s) and begins to increase slowly, showing drain lag behavior. It is understood that the drain current begins to increase when the deep-acceptor surface states begin to capture holes [11] or emit electrons. It is clearly seen that the change of drain current is smaller for the case with a field plate when comparing for the same V_{Dfin}, indicating that the drain lag is smaller for the field-plate structure. Without a field plate, a barrier for electrons is formed at the gate-to-drain region during the transients [9], and hence I_{D} becomes very low. On the other hand, with a field plate, the potential under the field plate is almost flat and a small barrier is seen at the field-plate edge, and hence I_{D} becomes larger, resulting in smaller drain lag.

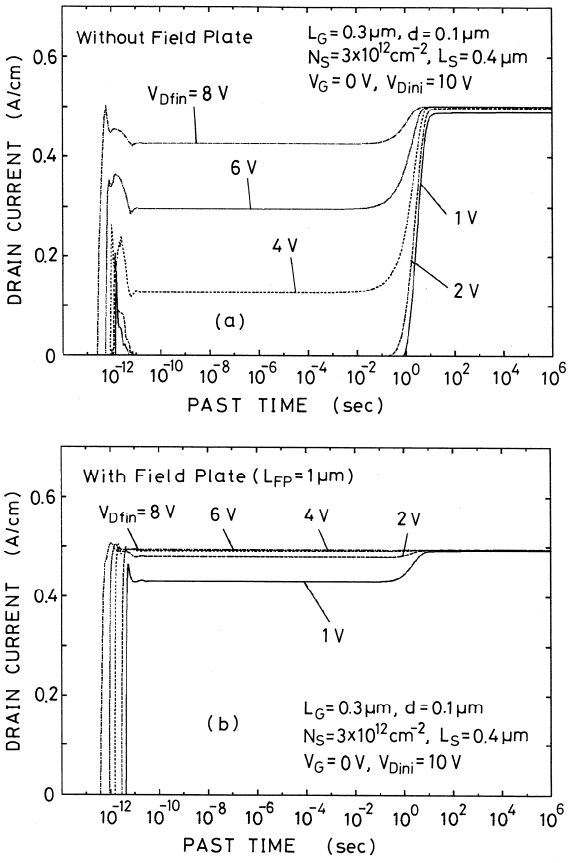

Figure 2: Calculated drain-current responses of GaAs MESFETs when V_{D} is lowered abruptly from 10 V to V_{Dfin} and V_{G} is kept constant at 0 V. d = 0.1 μm. N_{S} = 3×10^{12} cm^{-2} and the surface-state layer length L_{S} is 0.4 μm. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm).

4 TURN-ON CHARACTERISTICS AND CURRENT SLUMP

Next, we have calculated a case when V_{G} is also changed from an off point. V_{G} is changed from the threshold voltage V_{th} to 0 V, and V_{D} is lowered from 10 V to V_{Don} (on-state drain voltage). V_{th} is defined here as a gate voltage where the drain current I_{D} becomes 5×10^{-3} A/cm. The characteristics (not shown here) become similar to those shown in Fig.2, although some transients arise when only V_{G} is changed (gate lag), and hence the current reduction rate becomes higher than that of drain lag. This current reduction is called current slump which is a combined effect of drain lag and gate lag.

Figure 3 shows calculated turn-on characteristics when L_{FP} = 1 μm and d is very thin (0.01 μm). Here, V_{D} is lowered from 10 V to V_{Don} and V_{G} is changed from V_{th} to 0 V. Surprisingly, the slow current transients disappear,

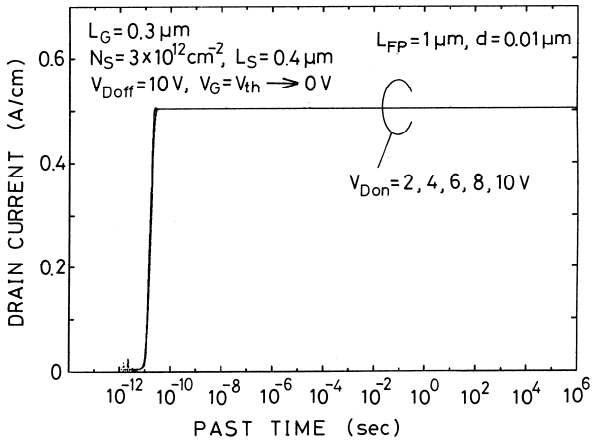

Figure 3: Calculated turn-on characteristics for L_{FP} = 1 μm and d = 0.01 μm when V_D is lowered abruptly from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

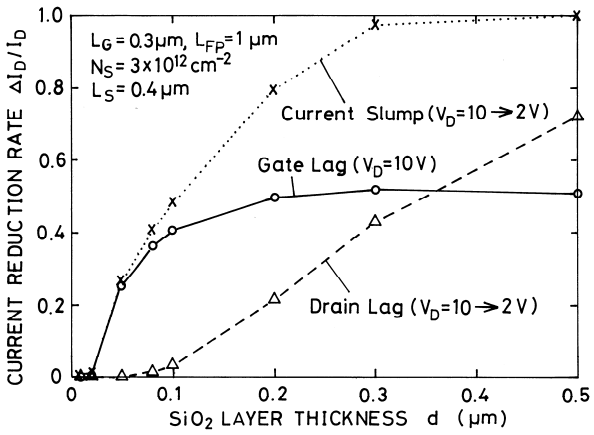

Figure 4: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag as a function of SiO_2 layer thickness d in the case of L_{FP} = 1 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

indicating that the lags and current slump are completely removed in this case. This may be because the surface-state effects are completely masked by the field plate.

5 FIELD-PLATE PARAMETER DEPENDENCE AND REMOVAL OF CURRENT SLUMP

We have next studied dependence of lag phenomena and current slump on the field-plate length L_{FP} and on the SiO_2 layer thickness d.

Figure 4 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, with d as a parameter. Here L_{FP} = 1 μm. As d becomes thin, the lags and current slump are reduced, and they are completely removed when d becomes thinner than 0.02 μm. This may be because surface-state effects are completely masked by the field plate. When d is thin, the gate parasitic capacitance becomes a problem, but this removal of current slump is still a very interesting result.

Figiure 5 shows current reduction rates $\Delta I_D/I_D$ due to current slump as a function of SiO_2 layer thickness d, with field-plate length L_{FP} as a parameter. It is seen that when L_{FP} becomes shorter, the current slump becomes larger, but it is completely removed when d becomes thinner than 0.02 μm even if L_{FP} is equal to the surface-state layer length L_S (0.4 μm), although the current slump becomes very large when L_{FP} = 0.2 μm.

In order to study how short we can reduce the field-plate length L_{FP} while maintaining the removal of current slump, we calculate in detail the lags and current slump between L_{FP} = 0.3 μm and 0.4 μm in the case of d = 0.02 μm. Figure 6 shows the results. From this figure, we can conclude that the current slump is completely removed even if L_{FP} is shortened to 0.35 μm.

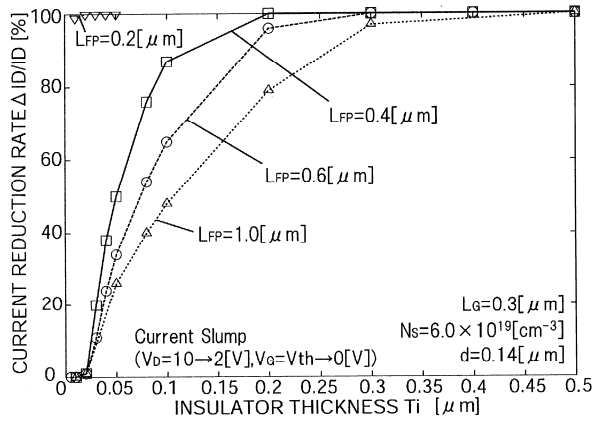

Figure 5: Current reduction rate $\Delta I_D/I_D$ due to current slump, as a function of SiO_2 layer thickness d, with field-plate length L_{FP} as a parameter. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

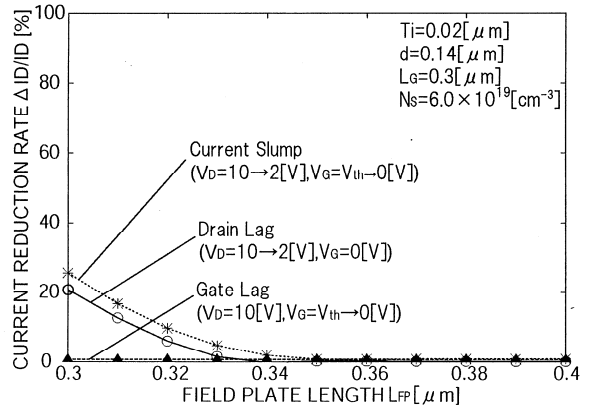

Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag as a function of field-plate length L_{FP} (0.3 ~ 0.4 μm) in the case of d = 0.02 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

6 CONCLUSION

Two-dimensional transient analysis of field-plate GaAs MESFETs has been performed by considering surface states in the region from the gate toward the drain. The field-plate length L_{FP} and the thickness of SiO_2 passivation layer d are varied as parameters. It has been shown that the drain lag and current slump are reduced by introducing a field plate longer than the length of surface-state region L_S, but they are not removed completely when d is thick. It has been clearly shown that when d becomes very thin (≤ 0.02 μm), the lags and current slump are completely removed for L_{FP} longer than L_S. By carefully examining the L_{FP} dependence for $d = 0.02$ μm, it has been found that the lags and current slump are completely removed even if L_{FP} is comparable to L_S.

REFERENCES

[1] J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with improved breakdown voltage for *X*- and *Ku*-band power applications", IEEE Trans. Microwave Theory Tech., vol.41, pp.752-759, 1993.

[2] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs", Proc. IEEE, vol.90, pp.1048-1058, 2002.

[3] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers", Proc. IEEE, vol.96, pp.287-305, 2008.

[4] G. Koley, V. Tilak, L. F. Eastman and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of SiN_x passivation and UV illumination", IEEE Trans. Electron Devices, vol.50, pp.886-893, 2003.

[5] V. Desmaris, M. Rudzinski, N. Rorsman, P. R. Hageman, P. K. Larsen, H. Zirath, T. C. Rodle, and H. F. F. Jos, "Comparison of the dc and microwave performance of AlGaN/GaN HEMTs grown on SiC by MOCVD with Fe-doped or unintentionally doped GaN buffer layers", IEEE Trans. Electron Devices, vol.53, pp.2413-2417, 2006.

[6] A. Koudymov, V. Adivarahan, J, Yang, G. Simon, and M. A. Khan, "Mechanism of current collapse removal in field-plated nitride HFETs", IEEE Electron Device Lett., vol.26, pp.704-706, 2005.

[7] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure", IEEE Trans. Electron Devices, vol54, pp.1825-1830, 2007.

[8] K. Horio, A. Nakajima, and K. Itagaki, "Analysis of field-plate effects on buffer-related lag phenomena and current collapse in GaN MESFETs and AlGaN/GaN HEMTs", Semicond. Sci. Technol., vol. 24, pp.085022-1–085022-7, 2009.

[9] K. Horio, T. Tanaka, K. Itagaki and A. Nakajima, "Two-dimensional analysis of field-plate effects on surface state-related current transients and power slump in GaAs FETs", IEEE Trans. Electron Devices, vol.58, pp. 698-703, 2011.

[10] H. Hafiz, M. Kumeno, and K. Horio, "Analysis of removal of surface-state-related lags and current slump in GaAs FETs", IEEE Electron Device Lett., vol.34, pp.1361-1363, 2013.

[11] K. Horio, H. Yanai and T. Ikoma, "Numerical simulation of GaAs MESFET's on the semi-insulating substrate compensated by deep traps", IEEE Trans. Electron Devices, vol.35, pp.1778-1785, 1988.

[12] K. Horio and T. Yamada, "Two-dimensional analysis of surface-state effects on turn-on characteristics in GaAs MESFET's", IEEE Trans. Electron Devices, vol.46, pp.648-655, 1999.

[13] K. Horio, A. Wakabayashi and T. Yamada, "Two-dimensional analysis of substrate-trap effects on turn-on characteristics in GaAs MESFET's", IEEE Trans. Electron Devices, vol.47, pp.617-624, 2000.

[14] A. Wakabayashi, Y. Mitani and K. Horio, "Analysis of gate-lag phenomena in recessed-gate and buried-gate GaAs MESFETs", IEEE Trans. Electron Devices, vol.49, pp.37-41, 2002.