

Simulation of High- k Passivation-Layer Effects on Breakdown Voltage in AlGaN/GaN HEMTs

H. Hanawa, Y. Satoh and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Saitama 337-8570, Japan, horio@sic.shibaura-it.ac.jp

ABSTRACT

Two-dimensional analysis of breakdown characteristics in AlGaN/GaN HEMTs is performed as parameters of relative permittivity of the passivation layer ϵ_r and its thickness d . It is shown that as ϵ_r increases, the off-state breakdown voltage V_{br} increases, because the electric field at the drain edge of the gate is weakened and the buffer leakage current is reduced. It is also shown that V_{br} increases as d increases. It is concluded that AlGaN/GaN HEMTs with a high- k and thick passivation layer should have high breakdown voltages.

Keywords: GaN, HEMT, breakdown voltage, high- k passivation layer, two-dimensional analysis

1 INTRODUCTION

AlGaN/GaN HEMTs are attracting considerable interest for high-frequency power amplifier and high-speed power switching device applications [1, 2]. It is well known that the introduction of a field plate enhances the power performance of AlGaN/GaN HEMTs [1, 3, 4] because the current collapse is reduced [1, 5, 6] and the off-state breakdown voltage V_{br} is increased [7-9]. This increase in V_{br} occurs because the field plate reduces the electric field at the drain edge of the gate. However, the introduction of field plate increases the parasitic capacitance and may degrade the high-frequency performance.

As another way to improve V_{br} , the introduction of a high- k passivation layer can be considered. The increase in V_{br} may occur because the electric field profiles between the gate and the drain can be smoothed by introducing a high- k dielectric [10-12]. There have been few or no experimental and theoretical studies on how the high- k passivation layer affects the breakdown voltages of AlGaN/GaN HEMTs. Therefore, we performed a two-dimensional analysis of breakdown characteristics in AlGaN/GaN HEMTs as functions of the relative permittivity of the passivation layer ϵ_r and the passivation layer thickness d , and found that V_{br} is enhanced when ϵ_r is high and d is thick.

2 PHYSICAL MODELS

Figure 1 shows the device structure analyzed in this study. The gate length L_G is 0.3 μm , and the gate-to-drain

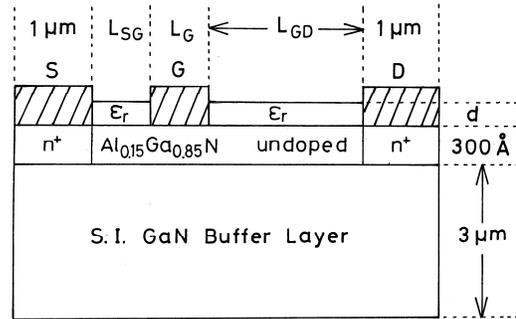


Figure 1: Device structure analyzed in this study.

distance L_{GD} is typically set to 1.5 μm . The relative permittivity of the passivation layer ϵ_r and the thickness of the passivation layer d are varied as parameters. Polarization charges of 10^{13} cm^{-2} are set at the heterojunction interface, and the surface polarization charges are assumed to be compensated by surface-state charges [7, 9]. Here, we do not consider gate tunneling [7, 9]. Instead, we concentrate on the breakdown due to impact ionization of carriers and due to an increase in the buffer leakage current. In a buffer layer, we consider a shallow donor ($N_{Di} = 10^{15} \text{ cm}^{-3}$), a deep donor, and a deep acceptor [13-15]. We take an energy level of $E_C - 2.85 \text{ eV}$ ($E_V + 0.6 \text{ eV}$) for the deep acceptor. For impurity compensation, we consider $E_C - 0.5 \text{ eV}$ as the deep donor's energy level [9]. As values of the deep-acceptor density N_{DA} , we consider a case with a high N_{DA} of 10^{17} cm^{-3} [9]. To mitigate the short-channel effects, a study [16] indicates that the acceptor density in a buffer layer should be higher than 10^{17} cm^{-3} . In a Fe- or C-doped buffer layer, the deep-acceptor density should be very high.

Basic equations to be solved are Poisson's equation including ionized deep-level terms and continuity equations for electrons and holes including the carrier generation rate by impact ionization and carrier loss rates via the deep levels [9, 17-21].

3 PERMITTIVITY DEPENDENCE OF BREAKDOWN VOLTAGE

Figure 2 shows the calculated drain current I_D – drain voltage V_D curves and gate current I_G – V_D curves of AlGaN/GaN HEMTs when the gate voltage V_G is – 8 V, which corresponds to an off state. The parameter is the

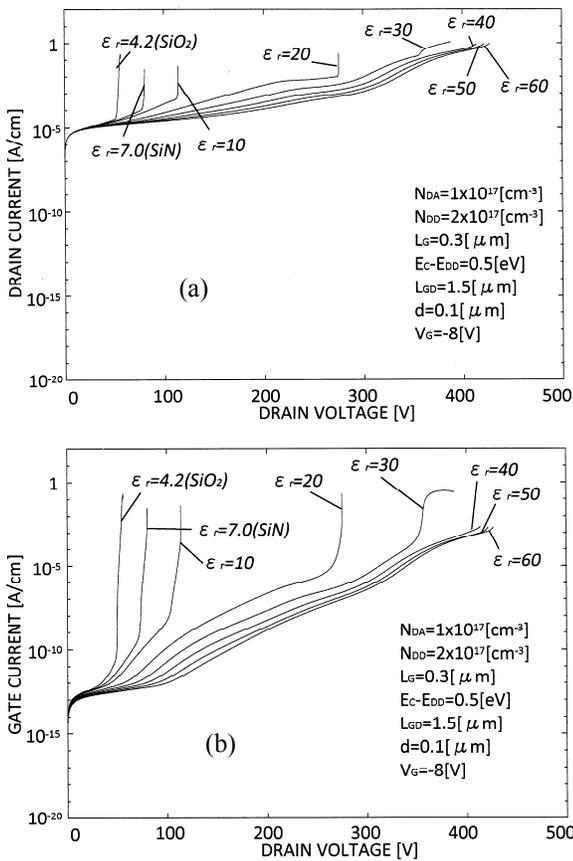


Figure 2: Calculated $I_D - V_D$ curves ((a)) and $I_G - V_D$ curves ((b)) of AlGaIn/GaN HEMTs, where $L_{GD} = 1.5 \mu\text{m}$ and $d = 0.1 \mu\text{m}$. $E_C - E_{DD} = 0.5 \text{ eV}$. $V_G = -8 \text{ V}$.

relative permittivity of the passivation layer ϵ_r . Here the thickness of the passivation layer d is $0.1 \mu\text{m}$. It is seen that for relative low values of $\epsilon_r (\leq 20)$, a sudden increase in I_G corresponds well to a sudden increase in I_D , that is, the breakdown. In this case, I_G is nearly equal to I_D , and it is almost composed of hole current. It is understood that electrons and holes are generated by impact ionization due to a high electric field particularly at the drain edge of the gate. The generated electrons flow toward the drain to cause the sudden increase in I_D , and the generated holes mainly flow toward the gate to cause the sudden increase in I_G . This is the cause of the breakdown. On the other hand when $\epsilon_r \geq 40$, the sudden increase in I_G is not yet observed, but I_D becomes a rather high value ($> 1 \text{ mA/mm}$). In this region, I_G is very low compared to I_D , and I_D is almost equal to the source current. Therefore, the buffer leakage current becomes very high in this region. In the GaN device field, the drain voltage at which I_D becomes 1 mA/mm is regarded as an off-state breakdown voltage. So, we call this voltage as the off-state breakdown voltage here.

Figure 3 shows a comparison of the electric field profiles along the AlGaIn/GaN heterojunction interface when ϵ_r is relatively low. Fig.3(a) shows the case of $\epsilon_r = 7$, and Fig.3(b) shows the case of $\epsilon_r = 20$. When $\epsilon_r = 7$, the increase in V_D is entirely applied along the drain edge of the

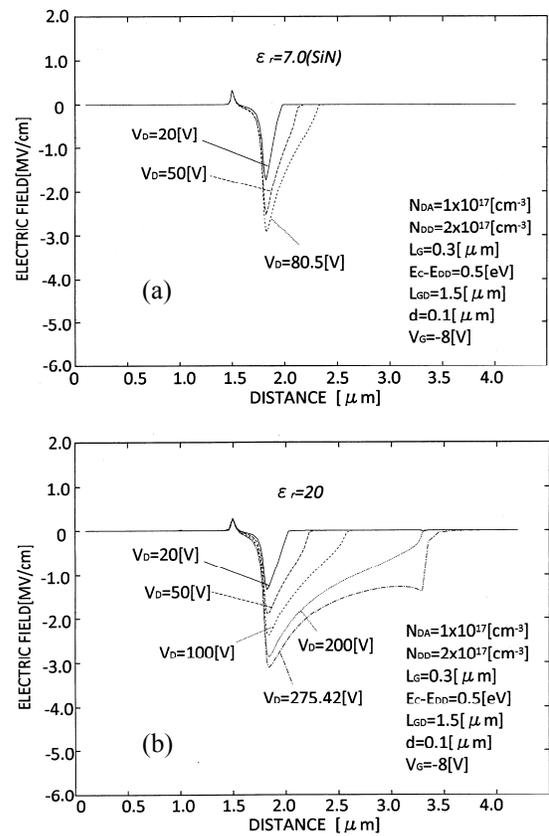


Figure 3: Comparison of electric field profiles along the heterojunction interface. $d = 0.1 \mu\text{m}$. $V_G = -8 \text{ V}$. (a) $\epsilon_r = 7$, (b) $\epsilon_r = 20$

gate, leading to the direct gate breakdown at around $V_D = 80 \text{ V}$. On the other hand, when $\epsilon_r = 20$, the electric field at the drain edge of the gate is weakened, and it is not so high even when $V_D = 100 \text{ V}$. This occurs because in the insulator the applied voltage tends to drop uniformly in general, and hence when the insulator is attached to the semiconductor, the voltage drop along the semiconductor becomes smoother at the drain edge of the gate if the ϵ_r of the insulator is higher and the effect of the insulator becomes more significant. As V_D increases, the electric field between the gate and the drain increases, and the high electric field region reaches the drain. In this situation, the impact ionization of carriers may occur to some extent in the entire region between the gate and the drain. Then the electric field at the drain edge of the gate becomes very high ($\geq 3 \text{ MV/cm}$) and the impact ionization there becomes very significant, reaching the direct gate breakdown at approximately $V_D = 275 \text{ V}$.

Figure 4 shows an off-state breakdown voltage V_{br} as a function of ϵ_r . A case of $V_G = -10 \text{ V}$ is also shown for reference. V_{br} is defined here as a drain voltage when I_D becomes 1 mA/mm . V_{br} increases with ϵ_r when ϵ_r is relatively low and saturates when ϵ_r becomes high. In the region where ϵ_r is high, V_{br} becomes higher for $V_G = -10 \text{ V}$. This is because the buffer leakage current becomes lower when V_G becomes more negative.

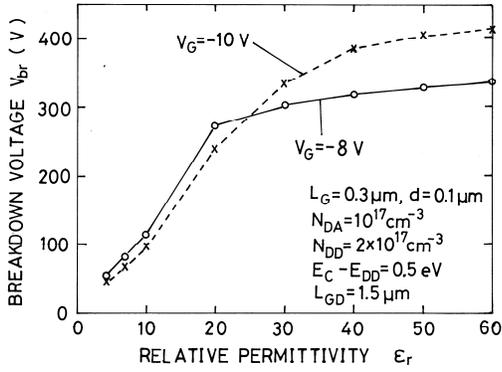


Figure 4: Calculated off-state breakdown voltage V_{br} versus relative permittivity of the passivation layer ϵ_r . $L_{GD} = 1.5 \mu\text{m}$ and $d = 0.1 \mu\text{m}$

It should be mentioned that for longer L_{GD} , the off-state breakdown voltage for high ϵ_r (> 30) could increase, because the high electric-field region can extend more toward the drain. In fact, as shown in Fig.5, V_{br} becomes higher for longer L_{GD} when ϵ_r is high.

4 INSULATOR THICKNESS DEPENDENCE OF BREAKDOWN VOLTAGE

Figure 6 shows the calculated $I_D - V_D$ curves and $I_G - V_D$ curves of AlGaIn/GaN HEMTs when V_G is -8 V , which corresponds to an off state. The parameter is the thickness of the passivation layer d . Here $\epsilon_r = 20$. It is seen that for a relatively thin d ($\leq 0.1 \mu\text{m}$), an increase in I_G corresponds well to a sudden increase in I_D , that is, the breakdown. As in the case of low ϵ_r in Fig.2, the gate current is almost composed of hole current, and it is nearly equal to I_D . Therefore, in this case, the breakdown occurs owing to impact ionization of holes at the drain edge of the gate. On the other hand, in the case of a relatively thick d ($\geq 0.2 \mu\text{m}$), I_D becomes very high ($> 1 \text{ mA/mm}$) before an abrupt increase in I_D . In this region I_G is very low compared to I_D , which is almost equal to the source current. Therefore, in this case, the increase in buffer leakage current seems to be a cause of the large drain current, as in the case of the high ϵ_r in Fig. 2.

Figure 7 shows the calculated off-state breakdown voltage V_{br} as a function of d . Here, $\epsilon_r = 20$. V_{br} increases with d when d is relatively thin, and saturates when it becomes thicker than $0.1 \mu\text{m}$. When V_G is more negative (-10 V), V_{br} is lower in the relatively thin d region because the electric field at the drain edge of the gate becomes higher. But, V_{br} becomes higher in the relatively thick d region because the buffer leakage current becomes lower.

From the above points, we can conclude that increasing d has the same effect as increasing ϵ_r : the off-state breakdown voltage is increased.

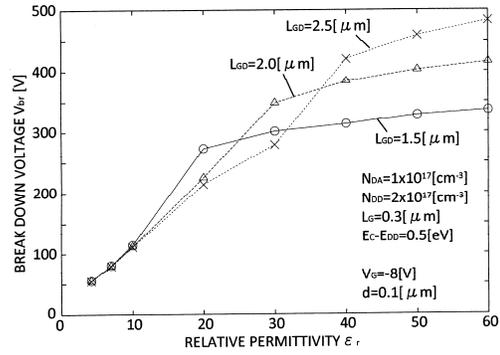


Figure 5: Calculated off-state breakdown voltage V_{br} versus ϵ_r , with L_{GD} as a parameter. $d = 0.1 \mu\text{m}$. $V_G = -8 \text{ V}$.

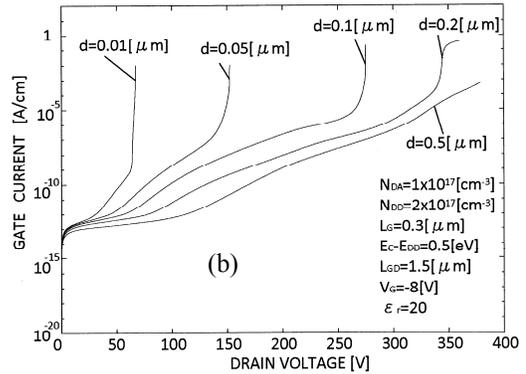
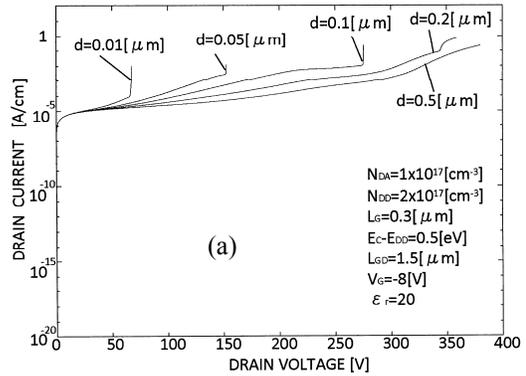


Figure 6: Calculated $I_D - V_D$ curves ((a)) and $I_G - V_D$ curves ((b)) of AlGaIn/GaN HEMTs, where $L_{GD} = 1.5 \mu\text{m}$ and $\epsilon_r = 20$. $E_C - E_{DD} = 0.5 \text{ eV}$. $V_G = -8 \text{ V}$.

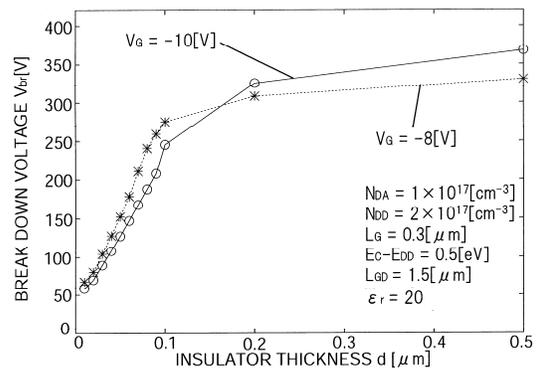


Figure 7: Calculated off-state breakdown voltage V_{br} versus passivation-layer thickness d . $L_{GD} = 1.5 \mu\text{m}$ and $\epsilon_r = 20$.

5 CONCLUSION

Two-dimensional analysis of breakdown characteristics in AlGaIn/GaN HEMTs has been performed as parameters of relative permittivity of the passivation layer ϵ_r and its thickness d . It has been shown that as ϵ_r increases, the off-state breakdown voltage V_{br} increases. This is because the electric field at the drain edge of the gate is weakened as ϵ_r increases and V_{br} due to impact ionization increases. V_{br} saturates when ϵ_r becomes high, because the buffer leakage current increases and reaches a current level corresponding to the breakdown. It has also been shown that V_{br} increases as the thickness of the passivation layer d increases. Increasing d has the same effect as increasing ϵ_r . It is concluded that AlGaIn/GaN HEMTs with a high- k and thick passivation layer should have high breakdown voltages

REFERENCES

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers", Proc. IEEE, vol.96, pp.287-305, 2008.

[2] N. Ikeda, Y. Niiyama, H. Kambayashi et al., "GaN power transistors on Si substrates for switching applications", Proc. IEEE, vol.98, pp.1151-1161 2010.

[3] Y.-F. Wu, A. Saxler, M. Moore et al., "30-W/mm GaN HEMTs by field plate optimization", IEEE Electron Device Lett., vol.23, pp.117-119, 2004.

[4] Y. Hao, L. Yang, X. Ma et al., "High-performance microwave gate-recessed AlGaIn/AlN/GaN MOS-HEMT with 73% power-added efficiency", IEEE Electron Device Lett., vol.32, no.5, pp.626-628, May 2011.

[4] A. Brannick, N. A. Zakhleniuk, B. K. Ridley et al., "Influence of field plate on the transient operation of the AlGaIn/GaN HEMT", IEEE Electron Device Lett., vol.30, no.5, pp.436-438, May 2009.

[5] K. Horio, A. Nakajima, and K. Itagaki, "Analysis of field-plate effects on buffer-related lag phenomena and current collapse in GaN MESFETs and AlGaIn/GaN HEMTs", Semicond. Sci. Technol., vol.24, pp.085022-1-085022-7, 2009.

[7] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaIn/GaN high electron mobility transistors using a field plate", IEEE Trans. Electron Devices, vol.48, pp.1515-1521, 2001.

[8] E. Bahat-Treidel, O. Hilt, F. Brunner et al., "AlGaIn/GaN/AlGaIn DH-HEMTs breakdown voltage enhancement using multiple gating field plates (MGFPs)", IEEE Trans. Electron Devices, vol.57, pp.1208-1216, 2010.

[9] H. Onodera and K. Horio, "Analysis of buffer-impurity and field-plate effects on breakdown characteristics in small sized AlGaIn/GaN high electron mobility transistors", Semicond. Sci. Technol., vol.27, pp.085016-1-085016-6, 2012.

[10] Q. Luo and Q. Yu, "Electric field modulation by introducing a HK dielectric film of tens of nanometers in AlGaIn/GaN HEMT", Nanosci. Nanotechnol. Lett., vol.4, pp.936-939, 2012.

[11] H. Hanawa and K. Horio, "Increase in breakdown voltage of AlGaIn/GaN HEMTs with a high- k dielectric layer", Phys. Status Solidi A, vol.211, pp.784-787, 2014.

[12] H. Hanawa, H. Onodera, A. Nakajima, and K. Horio, "Numerical analysis of breakdown voltage enhancement in AlGaIn/GaN HEMTs with a high- k passivation layer", IEEE Trans. Electron Devices, vol.61, pp.769-775, 2014.

[13] K. Horio, K. Yonemoto, H. Takayanagi, and H. Nakano, "Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors" J. Appl. Phys., vol.98, no.12, pp.124502-1-124502-7, 2005.

[14] A. Nakajima, K. Fujii and K. Horio, "Numerical analysis of buffer-trap effects on gate lag in AlGaIn/GaN high electron mobility transistors", Jpn. J. Appl. Phys., vol.50, pp.104303-1-104303-6, 2011.

[15] K. Horio, H. Onodera, and A. Nakajima, "Analysis of backside-electrode and gate-field-plate effects on buffer-related current collapse in AlGaIn/GaN high electron mobility transistors", J. Appl. Phys., vol.109, pp.114508-1-114508-7, 2011.

[16] M. J. Uren, K. J. Nash, R. S. Balmer et al., "Punch-through in short-channel AlGaIn/GaN HFETs", IEEE Trans. Electron Devices, vol.53, pp.395-398, 2006.

[17] K. Horio, H. Yanai and T. Ikoma, "Numerical simulation of GaAs MESFET's on the semi-insulating substrate compensated by deep traps", IEEE Trans. Electron Devices, vol.35, pp.1778-1785, 1988.

[18] K. Horio, K. Asada and H. Yanai, "Two-dimensional simulation of GaAs MESFETs with deep acceptors in the semi-insulating substrate", Solid-State Electron., vol.34, pp.335-343, 1991.

[19] K. Horio and K. Satoh, "Two-dimensional analysis of substrate-related kink phenomena in GaAs MESFET's", IEEE Trans. Electron Devices, vol.41, pp.2256-2261, 1994.

[20] K. Horio and A. Wakabayashi, "Numerical analysis of surface-state effects on kink phenomena of GaAs MESFETs", IEEE Trans. Electron Devices, vol.47, pp.2270-2276, 2000.

[21] Y. Mitani, D. Kasai and K. Horio, "Analysis of surface-state and impact-ionization effects on breakdown characteristics and gate-lag phenomena in narrowly-recessed-gate GaAs FETs", IEEE Trans. Electron Devices, vol.50, pp.285-291, 2003.