

Novel Nanoelectromechanical Switches for VLSI Power Integrity Improvement

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ABSTRACT

Complementary Metal Oxide Semiconductor (CMOS) is facing extreme difficulties to realize energy efficient designs while the scaling of channel length has been being at the same pace in the past several decades. In this paper, we presented a novel Nano-Electrical-Mechanical Switch (NEMS), which is developed to address some intrinsic limitations of the CMOS technology due to the feature size shrinking, such as short channel effects, sub threshold leakage, gate tunneling, band to band tunneling current and so on. Theoretical calculation and FEA software simulation have been done to model the NEMS device. To demonstrate the advantages of the novel NEMS devices, a Ternary Content Addressable Memory cell is implemented with only 6 NEMS devices, compared with 12 transistors in the traditional CMOS technology. The reduced number of devices decreases the delay time, realized a better yield and better operation margins. The static and dynamic powers of this NEMS Ternary Content Addressable Memory cell are also calculated. The leakage power of the NEMS TCAM is almost zero. The dynamic power consumption is shown much lower than the TSMC 0.13 um CMOS devices. In this paper, we also study the NEMS switches from the power integrity point of view, and the NEMS devices exhibits a better performance compared with CMOS transistors.

Keywords NEMS Power Integrity TCAM VLSI Decoupling Capacitors

INTRODUCTION

The Moore's law has been closely followed by the microelectronics industry in the past several decades. The VLSI integration density increases 60% per year and the circuit speed is getting faster as well. However, due to the short channel effects, sub threshold leakage, gate tunneling, band to band tunneling current and so on, all these advantages on the speed and integration density are paid at the price of much higher power consumption. The traditional CMOS device is hitting the theoretical limits soon [1]. The world is entering the era of "More Moore Devices" The advance of the micro-fabrication technology makes the Nano size electromechanical switches circuits possible. Because of the dramatically reduced leakage current, which means reduced static power consumption, the NEM switches are much demanded for making memories. The NEMS switches

have been intensively studied during the past ten years. These devices have different structures and operation principles such as laterally switching structures, cantilevered beam, and doubly-clamped beams; different materials, such as silicon, carbon nanotube and silicon carbide. A list of representative NEMS devices developed since 2000 are summarized in table 1. The on resistance and operating voltage are also listed for comparison purpose.

Device	R _{on} (Ohm)	Operating voltage (volt)
Rueckes.T et al	10 ²	2.5
Lee, S et al	10	3
Smith, R et al	10 ² -1 ⁴	5
Dujardin, E et al	10 ⁴	3.5
Jang, J et al	10 ⁴	24
Kaul, A et al	10-10 ⁴	2.5
Subramanian, A	10 ² -10 ³	0.8
Hayamizu, Y et	10 ³	50
Jang, W et al	<10 ⁶	12
Lee, T-H et al	-	6

Table 1 Summarization of reported representative NEMS switches since 2000 [2]

Besides these simple structure NEMS switches. There are some NEMS logic gates devices were also reported in the literature. Hamed Dadgour, et al has demonstrated a laterally actuated double electrode NEMS device, which can realize the NAND, XOR and NOR gates by only one device [3]. However, the pull-in voltage is up to 20 volt, which is too high to make this device to be compatible or compare with CMOS technology. A theoretical single device CNEM inverter was reported by from Stanford University [4]. Based on the calculation results, this proposed CNEM inverter can be operated by less than 3 volt and at the frequency range from several hundred MHz to GHz. Elad Alon's group developed a NEMS device relay to realize the low power circuit design [5]. The fabricated device could save up to 10x energy compared with the same size CMOS devices.

However, the device is only tested and simulated at ~100MHz.

As discussed above, all these Nanoelectricalmechanical switches suffer from different kinds of problems that are difficult to overcome by themselves, such as the high operation voltage, stiction problem, relatively low resonant frequencies, and incompatible fabrication process with CMOS technology. To better accommodate these issues, we design, fabricate a novel NEMS switches. This NEMS switch we presented in this paper is fabricated with the CMOS compatible technology and operates at 1~3 volt, depending on the size of the device. A theoretical macro model of this NEMS device was developed. The theoretical calculation results are compared with the ANSYS simulation results. A good correlation between the theoretical results and simulation results are observed. It demonstrates a good merit combining all the characteristics compared with other reported NEMS devices.

NANO ELECTROMECHANICAL SWITCHES

The proposed NEMS switches employ an overlap bridge structures with metal coated Silicon Nitride beams to form voltage operated mechanical switches. Figure 1 shows the schematic of a XOR NEM Switch. The XOR device has four terminals, gate1 (G1), gate2 (G2), drain (D), source (S). The metalized traces on the bridge structures are used as the conducting channel for the device. Similarly, the “AND”, “NAND” and “NOT” gate can be realized by reconfiguring the metal traces layout. Thus the logic gates are implemented in a single device. For the XOR gate, the two gates, G1 and G2, are connected to the external control voltages. Only when the two gates are both applied logic high or low, the two bridges stand still and no conductions between drain and source. When the different logic potentials applied to the gates, the bridges will contact, so the conducting channel is formed by the metal traces. The drain and source overlapping areas are made about 4 times smaller than the gate region intentionally, in order to avoid the drain-source attracting affect. Figure 2 shows the SEM picture of a fabricated XOR NEM witch, and the terminals are labeled accordingly.

NEMS DEVICES MODELING

To understand the operation behavior of the XOR NEMS, including pull in voltage and switching time, the bridge

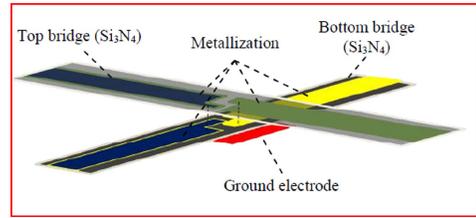


Fig. 1 Schematic of a Nanoelectricalmechanical Switch

structure is studied by both theoretical model and software model methods. The bridge structure can be modeled as a doubly clamped laminated beam. The applied voltage generates a uniformly distributed load on the beam surface. The bridge structure can be considered as a doubly clamped laminated beam. To roughly describe the dynamic behavior of the switching acitivity, some approximations were made. Firstly, in the model studied in this paper, the coated metal electrode is very thin compared with the Silicon Nitride substrate, so the laminated beam can be approximated as a single material structure. Secondly, the high order vibration modes are not considered in the model, only the primary vibration mode is studied. By applying the beam theory equations, the first vibration mode resonant frequency of this beam is [6]

$$f_n = \frac{k_n^2}{2\pi L^2} \sqrt{\frac{EI}{\rho A}}$$

in which E is the Young’s Modulus of the silicon nitride, L is the beam length, ρ is material density and I is the moment of inertia of the beam. k_n is the vibration mode factor of the beam. For the particular device studied in this paper, the beam length is 120 μm . The beam width is 30 μm , and the beam thickness is about 200 μm . The calculated resonant frequency is ~30 MHz. The displacement at any point of the beam to the neutral position can be written as

$$y = \frac{-qx^2}{24EI} (x-L)^2$$

in which, q is the uniform load applied on the beam. x is the distance from one clamped point to interested point. Pull in voltage calculation

$$V_{pull-in} = \frac{2g_0}{3} \sqrt{\frac{k}{1.5C_0}}$$

in which g_0 is the gap between two electrodes at zero voltage. The calculated pull in voltage is ~1.9 volt, compared with the simulation result of 1.8 volt. The calculated spring constant is 2.95 N/m. Figure 3 is the equivalent circuit model for the

NEMS switch. It is composed of variable capacitors, which is corresponding to the capacitor formed by the two bridges overlaying regions, and the resistors, which represent the leakage current and parasitic resistance in the device.

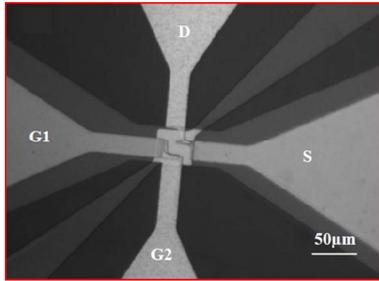


Fig. 2 SEM photograph of a fabricated NEM switch

Figure 3 shows the functional test setup. The input and output waveform of the NEMS device clearly shows the XOR function of the device.

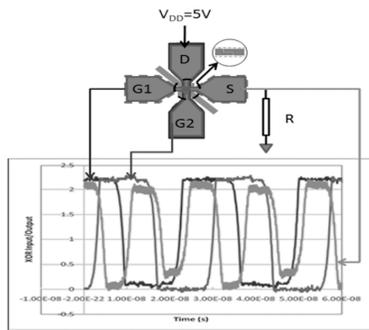


Fig. 3 Test fixture of the NEMS XOR device

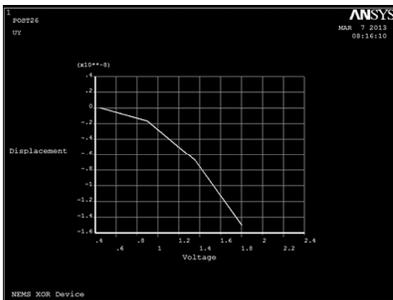


Fig. 4 The displacement of the bridge structure versus applied external voltage.

The NEMS bridge structure has been stimulated by FEA software, ANSYS. By using trans126 element to mimic the capacitor formed by two electrodes, the switching time, resonant frequency, pull in voltage and other mechanical behaviors of the NEMS switches are derived. Figure 4 shows the bridge structure displacement under the applied external operation voltage on the bridge. In the simulation, squeeze

film damping and elastic damping effects are taken into consideration. Figure 4 is the plot of displacement change as the operation voltage increases. TCAM--Ternary Content Addressable Memory, draws a lot of attention from the high speed circuit designers these years. It is widely used in the network application, such as routers. There are a lot of research efforts devoted to reduce the power consumption of the TCAM without sacrificing the performance [7]. The CMOS TCAM is simulated by LTSPICE. The dynamic power of the CMOS TCAM is 0.2 uW.

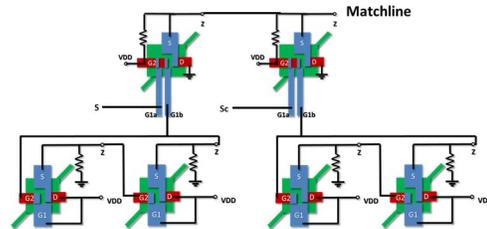


Fig. 5 The TCAM can be implemented by 6 NEMS devices, including four XOR and two AND gates

Match-line power consumption is not considered. The six devices NEMS TCAM is shown in figure 8. The calculated static power is almost zero and dynamic power per search is 28 nW (worst case). Fig.9 shows the TCAM waveforms that indicate “Match” and “Miss” cases.

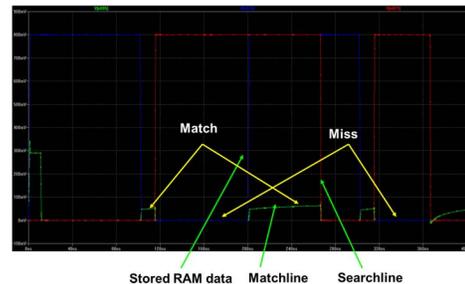


Fig. 6 The output waveform of a TCAM cell

DECOUPLING CAPACITANCE CALCULATION

The on chip decoupling capacitance calculation generally follows two principles, which are decoupling capacitor fabrication density and charge conservation law separately. These methodologies could estimate the decoupling capacitor requirement when the dynamic power consumption is available for the design. However, it has been always a challenge to accurately calculate dynamic power at the early stage of a design. The miscalculated dynamic power

directly leads to the wrong decaps numbers. So the iterations of floor planning work are involved, which increased design turnaround time. There is a strong desire of estimating the number of decaps accurately at the early design stage. Meanwhile, populating the empty area on the chip at the early design stage may cause the timing/clock path routing issues. To accommodate this desire, we proposed a new decoupling capacitor calculation methodology, which can accurately calculate the decoupling capacitance requirement at the early design stage, even before the delivery of netlist. Firstly, the decaps requirement for a single IP is calculated based on the charge sharing principle, to meet the voltage compression target on the power supply, with the awareness of operation frequency, as shown in figure 10. Secondly, the chip supply resonant frequency is calculated to refine the decoupling capacitance assertion. The decoupling capacitance increases during the refining process, the chip resonant frequency decreases. The iteration process of the decoupling capacitance calculation ends up with the converged chip resonant frequency.

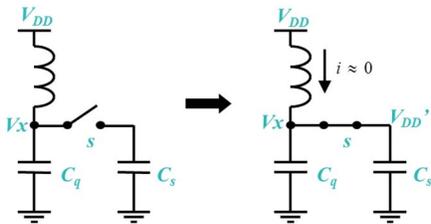


Fig. 7 Charge sharing scheme used to calculate decoupling capacitance for memories

$$C_{decap} = \frac{V_{DD}'}{V_{DD} - V_{DD}'} C_{dynamic} - C_{intrinsic}$$

There are two major parts of the dynamic power compression, one is the caused by the package inductance and chip capacitance, the ring out frequency is relatively low, and the other one is caused by memory switching. Decaps are placed to compensate the first quarter cycle voltage compression waveform.

$$C'_{decap} = \frac{1}{4} \frac{f_{cycle}}{f_{chip}} \frac{V_{DD}'}{V_{DD} - V_{DD}'} C_{dynamic} - C_{intrinsic}$$

CONCLUSION

In this paper, a novel NEM Switch is presented. The theoretical model of the device is compared with the ANSYS simulation results. A good correlation is observed between theoretical results with the simulation results, which proved the feasibility of the device modeling method. The proposed NEMS devices are considered as a very promising device

that can address the issues in the current CMOS technology. To proof the performance superiority of the NEMS switches, a TCAM cell is implemented by using only 6 NEMS devices. The NEMS TCAM could greatly reduce the leakage and dynamic power compared with the conventional CMOS technology. An improved power supply noise mitigation methodology is proposed, which can accurately predicate decaps needed for the ASIC chip at early design stage.

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