Arsenene Substrates Enable a New Era of High-Performance Semiconductors

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ABSTRACT

Recent advances in producing two-dimensional (2D) materials such as Graphene, Silicene and Phosphorene support the concept of an allotropic form of Arsenic being achievable as a layer of Arsenene-on-Silicon (AeOS). The technical community recently published metrological and computational evidence of Arsenene as a potential heterostructure that complements crystalline lattices of a range of semiconductor substrate materials. Until now, a stable process that yields high-quality interfaces between Silicon and a 2D layer of Arsenene has not been demonstrated.

Keywords: 2D materials, Arsenene, Silicene, Si Substrate

1 INTRODUCTION

Silicene has been proposed as a 2D sheet of silicon atoms that can be created by super-heating silicon and evaporating atoms onto a varuous substrates including Silver (111) and Ir (111). The platform is chosen due to its strucutal and chemical properties with regards to the arrangement of the deposited silicon atoms during the heating process, as the atoms fall onto the subtrate. The substrate has a second set of requirements for the new multilayered substrate to be conducive to current semi-conductor design and fabrication processes. Arsenene has recently been predicted to have stable configurations akin to Silicene, but using a process similar to depositing Silicene is not achievable. CSI2D conducted experiments from 2013 to 2014 to identify a stable and affordable process that forms Silicene and Arsenene on a variety of Silicon substrates to overcome Silicene-on-Silver limitations. A recent study [1] suggests that 2D monolayers on Silicon substrates have a strong influence on the arrangement of the surface atoms of the substrate during formation. A related study [2] indicates the high quality opto-electronic properties of multilayered 2D materials are not degraded by lattice mismatching of the layers. Recent reported calculations indicate arsenene should form a stable 2d layer. [3] The semiconductor research community has spent considerable resources over the last 30 years in attempts to improve performance of Si(112)\As\ZnTe\CdTe\HgCdTe IR detectors for medical applications, surveillance sensors and weaponry. Two significant advances for the deposition process for thin film CdTe on Silicon, was 1) employment of Si(112) surfaces, and 2) the use of Arsenic as a buffer layer [4]. IR detection was improved in each step.

2 EXPERIMENTAL

Fabricating two-dimensional layers of Arsenene and Silicene was realized in an earlier phase of CSI2D's research when an ultra-high vacuum reactor was built and used to test a variety of methods for uniform deposition of Arsenic-on-Silicon(112). The key to stable and uniform Arsenene-on-Silicon (AeOS) and Silicene-on-Silicon (SeOS) layers was discovered and optimized by exploiting unique vacuum techniques, temperatures and annealing processes similar to Silicon/CdTe thin film processes. The existence of a high-quality AeOS substrate was confirmed with calculations, metrology and laboratory research.

Early experimentation focused on fabricating an Arsenene layer on Silicon(112) as a baseline to prove process efficacy for additional substrate materials, with a focus on Silicon(112) substrates as the most compelling outcome for major advancements in semiconductor manufacturing for lattice matching. Monolayer Arsenic used for improved lattice matching in (II-IV) detectors was then tested and found to form an Arsenene surface layer. Using a proprietary ultra-high vacuum annealing reactor and MBE of Arsenic, CSI2D conducted a series of trials under varying temperature and annealing times to optimize the surface layers' uniformity for Arsenic-covered clean Silicon surfaces. STM, LEED and XPS analysis was conducted to verify that the Silicene/Arsenic substrate interfaces exhibited uniform dimensional features, and to establish the purity of the Silicene deposition was not corrupted by Oxygen at the interface. Evidence was first recorded using STM, LEED, and XPS analytical techniques.

3 RESULTS AND DISCUSSION

Figure 1 shows the row structures on the surface are periodic, with 2 nm rows running in the [1-10] direction on the Si(112) substrate. Figure 2 is a 3D perspective of a Si(112)/As surface, (24.8×62 nm). The surface was imaged at a bias = 2.0 V and a set point of 0.05 nA. The Z amplitude is 1.4 nm.

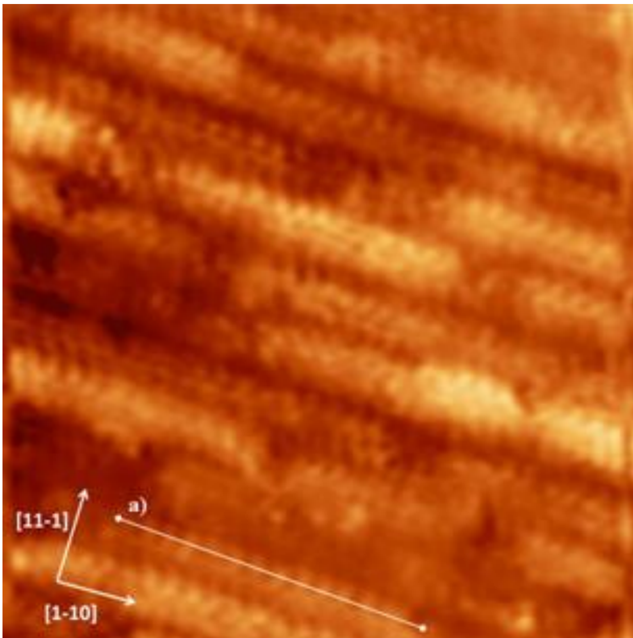

Figure 1: This figure is a (22 × 22 nm) STM image of Si(112)/As. The surface was imaged at a bias = 2.0 V and a set point of 0.05 nA. The Z amplitude = 0.77 nm. Feature a) marks a line of corrugation with a period of 0.78 nm in the [1-10] direction and 0.25 nm in height. Specifically for this feature, there are twelve 0.78 nm periods for corrugations in the [1-10] direction.

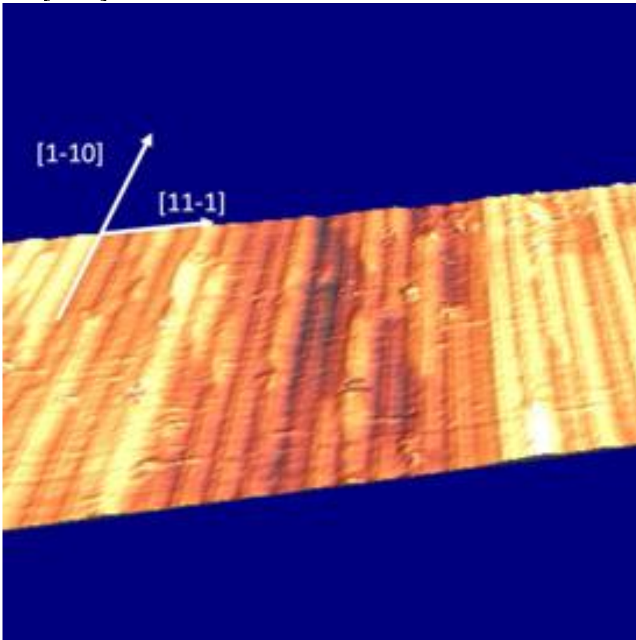

Figure 2: A 3D perspective of a Si(112)/As surface, (24.8 × 62 nm). The surface was imaged at a bias = 2.0 V and a set point of 0.05 nA. The Z amplitude is 1.4 nm.

Two STM images of separate surfaces one of the clean aggressively annealed Si(112) surface and one of the monolayer of arsenic MBE deposited during annealing on the a clean annealed Si(112) surface are shown to have the same large surface structure topology over a 50 x 50 nm region. (Figure 2)

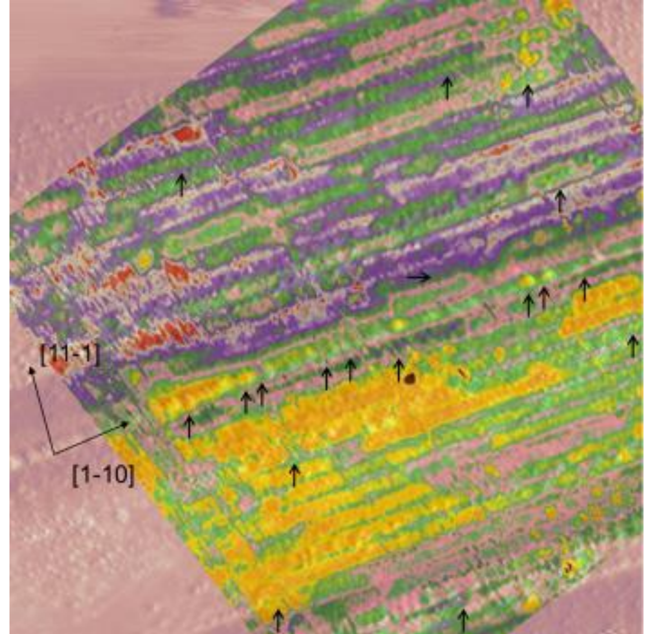

Figure 3: Two STM images of separate surfaces one of the clean aggressively annealed Si(112) surface and one of the monolayer of arsenic MBE deposited during annealing on the clean annealed Si(112) surface.

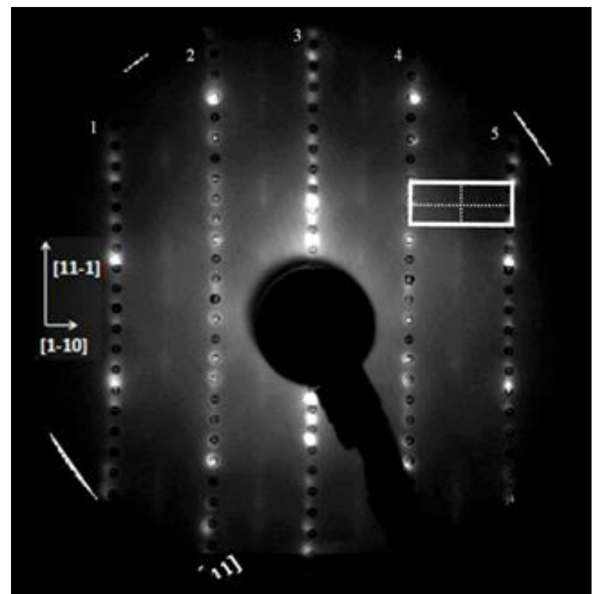

Figure 4: A LEED image of Si(112)/As with a software generated reciprocal lattice overlaid (black circles). The LEED peaks in rows 2 and 4 are matched in the [11-1] direction on a centered rectangular unit cell with a = 0.384 nm and b = 3.759 nm. All the rows align in the [1-10] direction. The LEED image was taken at 137 eV. The white rectangle represents the bulk-terminated unit cell while the dotted lines represent the (2×2) reconstructed unit cell.

4 CONCLUSIONS

After a monolayer of As is deposited on clean, annealed Si(112) surfaces, distinct rows, 2.0 nm wide in the [11-1] direction and running parallel to the [1-10] direction, are observed with STM. STM images of local regions of the Si(112)/As surface demonstrate a Si(111)-like hexagonal periodicity with a = 0.3905 nm. In these regions, the corrugation height along the rows in the [1-10] direction is 0.25 nm. The LEED image of Si(112)/As can be fitted with a centered rectangular unit cell, with a = 0.384 nm and b = 3.7586 nm, which is similar to the clean annealed Si(112) surface in Figure 3. Nanofaceting of the Si(112)/As surface is not observed. The arsenic monolayer suppresses the faceting as the sample is cooled during the annealing step. STM images of the annealed Si(112) and the Si(112)/As surface can be superimposed with strong correlation. When deposited by MBE, the arsenic monolayer preserves the annealed Si(112) surface. These observations are consistant with what would be observed for an Arsenene layer formed on the annealed Si(112) and therefore demonstrated a process for forming arsenene on Si(112) wafer substrates.

REFERENCES

[1] Lei Liu *et. al.*, *PNAS* 111, 47, 16670-16675, November 2014

[2] Yu-Chuan Lin , Chih-Yuan S. Chang , Ram Krishna Ghosh , Jie Li , Hui Zhu , Rafik Addou , Bogdan Diaconescu, Taisuke Ohta, Xin Peng, Ning Lu, Moon J. Kim, Jeremy T. Robinson, Robert M. Wallace, Theresa S. Mayer, Suman Datta, Lain-Jong Li, and Joshua A. Robinson, *Nano Lett.*, 14 (12), pp 6936–6941, December 2014

[3] C. Kamal and Motohiko Ezawa *Phys. Rev. B* 91, 085423, February 2015

[4] L. A. Almeida, Y. P. Chen, J. P. Faurie and S. Sivananthan, J. of Electronic Materials 25 (8), 1402-1405, July 1996