Modeling of Electromagnetic Phenomena Inside Modern Integrated Semiconductor Structures

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ABSTRACT

The electromagnetic phenomena are very important in case of 3D integrated circuit. The current methods and posibilities have been presented in the paper.

Keywords: electromagnetic compatibility, modeling and analysis of semiconductor structures, 3D IC, DRC, ERC

1 INTRODUCTION

One of the fundamental tools for the analog electronic circuit designers is the SPICE simulator, without which the design of industrial systems is unreal. Despite the decades the appearance of the first version of SPICE simulator, there are still real engineering problems difficult to solve using this approach e.g. the circuits with many solutions, harmonic balance analysis, chaotic systems and stiff-problems. In case of each the smallest improvements in electronics will gives important news to electronics will be directly perceptible in the industry.

In case of 3D Integrated Circuits (ICs) , the situation is similar, but the difficulty is at least two orders of magnitude larger. At the moment, 3D IC systems are regarded the further development of electronics called *More-Than-Moore*, which is regarded and hoped to be the answer for the continuous increase of computing power, miniaturization and specialization of electronics systems. Though, the knowledge of the basic physical phenomena is known (Electro Magnetic (EM) phenomena are described by Maxwell's equations, heat transfer by Fourier-Kirchhoff equation, mechanical stress etc.), it is still a significant difficulty in the simultaneous multidomain modeling and simulation of whole 3D IC systems structures due to obtain the correct convergent disbanded such complex structures. The simple example of 3D technology can be presented for an integrated CPU with additional memory, where a typical distribution of the 4 mm electromagnetic field above the surface of the "typical CPU". EM field can be expected to be even significantly more intense in the case of integrated CPU and memory structures made as two or more superimposed semiconductor structures in 3D IC (see IEEE 62433).

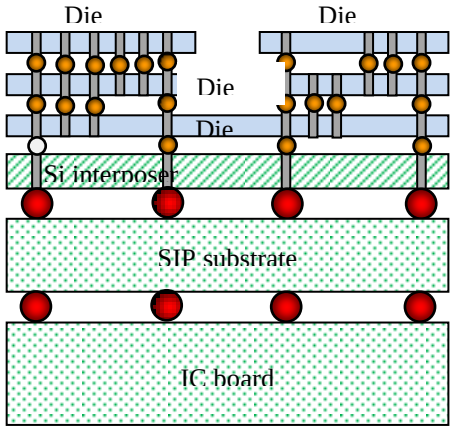

Fig. 2. The 3-D IC containing several structures connected on SIP substrate

Issues adressed in the project will allow to develop of this branch of electronics (giving the algorithms and prepared implementation and furthermore the simulation tools for constractors in the currently developed 3D IC)and thus bring a significant contribution to the discipline of electronics in multidomain modeling and simulation of integrated structures. The 3D technology seems to be specially promising way of producing multi-chip systems, as it significantly reduces length of interconnections and enables various ways of wireless inter-wafer communication. However, growing integration level causes increase of EM emissions, which can disturb circuits in their neighbor area, especially in face-to-face stacked wafers of 3D systems. There are some tools for analysis of EM phenomena in ICs, but they have specific limitations and they are not closely synchronized with IC design-flow environments. Typical design validation tools are able to detect only most obvious problems, like antenna errors. Development and introduction of the new EM approximation method and its application in form of set of effective and validated software tools, applicable during IC design, simulation, and validation stages, will improve progress in IC design and especially their EM properties. Such tools should include EM simulators coupled with electrical simulators, validation tools acting as add-ons/replacements to present tools used for Design Rule Checking (DRC), Electrical Rule Checking (ERC) and Signal Integrity (SI) tests.

This kind of effective tools are also expected to enable design of on-chip or 3D inter-chip wireless communication systems and EM field sensors.This direction of research should enable a new dimension of nano- and microelectronic system integration with 3D technologies. This in turn, should help further integration-scale increase in IC systems. The results are also expected to help 3D technologies in their transformation into a new dimension of nano- and micro-electronic system integration, by minimizing of inter-wafer EM disturbances and contribute to solving the existing problem of inter-wafer connections by enabling application of wireless communication links.

2 METODOLOGY

Reaching such goals, requires development and application of a method which offers significant reduction of calculation time-complexity from $O(n^2)$ down to nearly linear $O(n \log n)$. In addition a method of EMC model automated reduction and synthesis to the equivalent circuit form is to be developed (Fig. 2). Owing to such approach a set of design tools of high precision, numerical stability and calculation speed can be obtained. Such qualities are critical for modeling and simulation of EM phenomena in ICs. Moreover, in order to increase its speed, the system is to be implemented with application of GPGPU (General Purpose Graphic Processing Unit).

This set of software tools is planned to cooperate with professional IC CAD environments. The tools shall include the EM-solver coupled with the electrical solver, for multi-domain simulations, EM oriented circuit extractor and set of design validation tools, based on elaborated sets of design-rules.

The high efficiency of the devised EM phenomena approximation method and related software tools would enable conducting of some specialized time-consuming types of simulation. These include Monte-Carlo and transient-noise simulations. Such specific simulation extends knowledge of possible critical-points in IC, before there are found as sometimes serious faults in fabricated specimens. The possibility of such extensive simulation can lower cost of application of mature, full-fledged IC to its tasks. Universal EM solver with efficient circuit extractor can be useful for simulations of both undesired and planned EM emission (EME) and EM immunity (EMI) effects.

The topic of electromagnetic phenomena in electronic circuits and systems has been known, acknowledged and coped with for years. As for EM phenomena at IC level, situation looks somewhat different [1]. Only since lately, the problem is getting acknowledged, and standards concerning simulation, measurements, test of IC EM emissions and immunity has been emerging and even EMC[1] roadmap of IC are being predicted.

The importance of EM phenomena in IC design and operation increase along with increase of operating speed

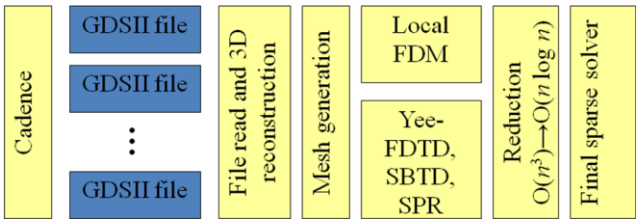

Fig. 2. The architecture of proposed EMC software

[2] and decrease of device sizing and power supply voltage. Operation speed increase slowly but consequently narrow difference between wavelengths of signal harmonics and length of on-chip interconnections. On other hand very high operation speed and very low supply voltage makes device compensate their high power demands by causing high current flows. This in turns may lead to generation of EM disturbances [3].

There is also an increasing number of various circuit solutions and design approaches, concerning specific circuit functionality that takes into account EM properties of the final circuit. There are solutions concerning both schematic and layout alteration.

Most of them are focused on digital logic [4], as these circuits both produce considerable amount of noise and EM emission and have relatively consistent structure of basic cells. Some EM disturbance problem solutions propose direct current and voltage glitch reduction techniques. There are known cases of successful utilization of slew-rate control circuitry for digital logic, clock signal timing shifting for distinct parts of digital systems. So called non-periodic and spread-spectrum clock signal application are also reported. Higher level approaches include replacement of synchronous sequential logic with asynchronous combinational logic, if possible. Another interesting study suggests that change of a whole logic implementation system can improve EM properties of final integrated system, e.g. CSL has been reported to be superior to CMOS logic in this matter.

Of course, several solutions are layout based, and thus can be used also in case of analog and mixed-signal systems. Layout improvements against EM disturbances include minimization of parasitic inductance, application of small serial resistors and decoupling capacitors on each of supply nets [5] or separation of supply systems for I/Os and distinct signal processing blocks. The latter idea can be extended so that special supply grids can be introduced in layout with bulk isolation technique [6], Apart from power nets, also signal nets should be specially placed in order to provide limited current densities and to avoid creation of signal paths forming antennae or loops.

From schematic point of view, analog and mixed-signal circuits may often require more specific approach regarding both EME and EMI, as their structure largely vary according to circuit functionality and application. This additional difficulty can be observed. The analytical approach to the device models can suggest ways of

[1] EMC – Electro Magnetic Compatibility

improvements, but special analysis is required for every distinct analog functional block. Highly specialized and various internal structure of analog circuits causes general shortage of EM disturbance reduction techniques of general application, apart from layout-based techniques for specific structures. Such specialized solution are usual for voltage-mode circuits [7], including high-voltage circuits and systems [8].

One of layout-based techniques is shielding circuit against EM disturbances through an application of metal layers as protective screens. Practically, number of metal layers is a process limitation on its own and additional sacrifice of these layers for sake of circuit shielding may be too high a price to be taken. Although, metal layers make become a problem in case of EM-active devices, like on-chip antenna, which also requires special analysis [9]. 3D circuits show limitation of this approach twofold. First, usually 3D circuits are a stack of matrices of sensors and signal conditioning and processing circuitry. The resolution of such matrices is a crucial parameter. Reduction of accessible metal layers number can be reached only with larger silicon area for the pixel in a matrix, which means lower resolution. Secondly, as long as only two wafers are to be connected to create a 3D circuitry, wafers may be placed face-to-face, which makes it possible to use metal layers as protective screen. In case there are three or more layers in a 3D circuit such approach is impossible, there will be face-to-rear connections and rear side of wafer is usually just bare silicon, thinned down to a few tens of micrometers. Thus, again at least one level of circuitry is directly exposed to emissions from another one.

Apart from electromagnetic phenomena treated as side effects of IC operation, another area of interest emerges. This area is related to increasing complexity of the modern ICs and its consequences for multi-wafer integrated systems, like SoC or especially 3D. Numerous and long interconnections cause problems in modern ICs. Long interconnections are a problem because of signal delays and possible EM phenomena generated in relation to such lines. Numerous interconnections are a problem in case of multi-wafer systems. A possible substantial improvement to this situation is application of wireless interconnections [10] or even whole networks of interconnections. Though the idea seems to have generated of on-chip wireless links on single-wafer circuits, it has potential to find its application in various 3D systems [1]. In case of single-wafer ICs the main way of transmission was electromagnetic link through inductive devices, both planar and vertical [11][12]. In case of multi-layer systems other possibilities also emerge. Optical links are expected to work as point-to-point signal links [13][14]. Similar application area may be covered by electromagnetic links based on capacitive devices and effects [15]. It can be seen that inductive electromagnetic links seems well suited for point-to-multipoint applications, like clock-signal propagation.

Application of such wireless on-chip (intra-chip) and inter-chip links and networks requires application of proper transmitters and receivers. Such devices require proper operation analysis and design, but also all the rest of chip contents needs to be proofed against EM influence.

Moreover, the trend of complete electronic system integration into a single chip (either single- or multi-wafer), cause on-chip integration of EM transmitters and receivers, for communication with chip external environments. RFID systems are a good example of such application [16]. Here also all the rest of chip internals must be proofed to be immune to EM signals, which now are a part of environments of such ICs.

Conclusion is that EM phenomena importance arises both due to:

- main trends in device level parameters (size, operation speed, supply voltage);
- demands of increasing integration level (SoC, 3D integrated systems with increasing complexity of internal connections);
- increasing importance of wireless applications (especially low-power short-range ones like RFID, which tend to be fully integrated into single ICs).

The presented state of the art also shows that various kinds of ICs and their functional blocks have quite distinct EM properties. It means they have different emissions and different immunity. Thus, the earlier in the design-flow the EMC limitations are taken into account, the better for the final design. First of all, it can be seen that a kind of universal approach concerning EM phenomena modeling and simulation must be applied if further significant progress in the area of EMC of ICs is to be obtained. Such approach must be backed-up with efficient and precise way of EM modeling of ICs, and taking EM phenomena into account in consecutive design-flow stages, (like: schematic design and simulation, laying out, and validation). Validation should be understood as a multi-step process, incorporating: DRC, ERC and SI. Modern design checkers included into professional IC design environments can check various issues related to circuit operation, manufacturability or reliability. Unfortunately EM properties still are out of their scope. The EM properties of a design are usually verified on the prototyping stage of product introduction.

Important effort has been made last years and international scientific committees are agreeing standards related to modeling of EM phenomena in ICs [17]. These models are: ICEM and ICIM. Generally, these models are dedicated for structure description of quite a limited precision. It is an outcome of a trend to get a solution that is compatible with existing simulators, e.g. model description complies with description format for SPICE type simulators. Such general model has limited possibility of adjustment of its precision, according to design requirements.

Some attempts to simulation of EM influence to ICs limits its interest to analysis at level of single device [18] (but not necessarily its layout structure), which also is not a

way for complex circuits analysis with regard to layout geometry.

Some software for IC EM phenomena has been introduced, they use mentioned ICEM or ICIM models. There are various approaches to improve quality of the model but they do not seem to enable universal approach to the EM phenomena problem at device or layout level, especially in case of complete function blocks or complete ICs.

There are several software tools for EM phenomena simulation and investigation, but there are numerous limitations related with them. Additionaly, many existing EM modeling methods are based on over-square time-complexity $O(n^2)$ solving methods, which limit complexity of the analyzed ICs. Concluding, most of existing EM phenomena related software is either too general in its purpose, either too specialized to its predefined tasks. Thus, available tools and methods are not applicable to analysis of IC internal blocks. Moreover, existing EM simulation software solutions use numeric algorithms that are quite time-complex, which limits their application to complex IC system simulations.

The method for IC-focused simulation of EM phenomena, and its application into an EM solver with circuit extractor, and EM-aware design validation tools, proposed in the project, would be very handy in the design process of complex, modern IC systems. To be of practical use, such tool set must be able to approximate IC-level EM phenomena closely based on circuit structure and geometry. Additionally, it should offer high time efficiency and precision of calculations. Finally, it must be able to cooperate with IC CAD environments to interweave EM circuit simulations and design validation into typical IC design-flow. Profound modifications to EM phenomena simulation approach must be introduced, to meet these requirements.

To sum up, the proposed set of EM approximation methods and software tools would be very useful for improving quality of complex IC systems. The goal of this research is to make the design of 3D systems easier by helping to solve crucial problems of such circuits, like face-to-face inter-wafer EM radiation and limited quality of inter-wafer connections.

3 CONCLUSIONS

The EM analisys of IC and 3D IC are very important element of CAD software. Unfortunatly the full-wave analisys is very hard to do very difficult to achieve due to the large number of required mesh nodes and PDE equations. However, it is possible to apply the Haar, Battle-Lemarie or Daubechies wavelets in order to obtain higher-order approximation. Additionally, WENO schemats allow to 64× memory reduction and 13× calculations speed-up. Unfortunately this goall is obtained for a regular mesh and many of EMC phenomenas should be detected using simplified rules (similar to DRC and ERC).

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