Time-Domain Monte-Carlo and Noise Analysis of MAPS Sensors

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ABSTRACT

A non-typical approach to extended simulational analysis for monolithic active pixel (MAPS) based binary pixel readout circuits is presented. Circuit solutions and simulation results are presented and discussed. An unpredicted phenomenon is detected in case of one of circuits under simulations. Shortcomings of typical simulational approach were thus exposed and amended. Operation of the affected circuit was corrected with no need for hardware modifications.
Keywords: MAPS sensors, Monte-Carlo, noise, simulations

1 INTRODUCTION

Applications of particle detection/tracking are quite wide, in general. Detection systems based on same basic operation principle are used for radiation detection in high energy physics [1] like e.g. International Linear Collider. MAPS matrices are present in biomedical equipment.

Progress in semiconductor process versus existing MAPS limitations results with exploration of possible new circuit architectures, like additional feedbacks, multiple storage devices, in-pixel analog-to-digital conversion, etc. [2]. Also, new processes and wafer parameter combinations are investigated in order to obtain new quality of final sensor matrix operation, like solutions with depleted epitaxial layer, for example.

2 BACKGROUND

Scope of this paper is to present results of works related to the LUSIPHER project and conducted during author's post-doc research at Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg [3], among other tasks focuses on similar topics [4]. Some of these works were focused on checking impact of circuit complexity on its operation precision in presence of process mismatches. Current-mode bias dissemination tree was being design and several structures were tested against Monte-Carlo variations.

The outcome was quite interesting, it was found that in case of DC-operating bias circuitry it may be better (in some circumstances) to implement simpler and less precise version of circuit (current mirror in this case) than more complex and refined but more prone to process variation [4]. Fig. 1 shows two versions of simple two-stage current-mirror trees, one based on simple mirrors and one based on cascode mirrors. Fig. 2 presents output current flow for the cascode current mirrors and Fig. 3 for simple current mirrors.

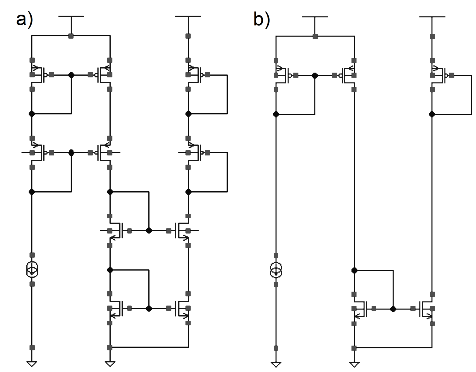

Figure 1: Cascode (a) and simple (b) current mirror tree [4].

It can be clearly observed that complexity of the cascode structure also gets reflected in wider spread of its output current flow when process variation is taken into account. Moreover, in reality current dissemination mirror trees can have more than two stages and the problems gets even more pronounced.

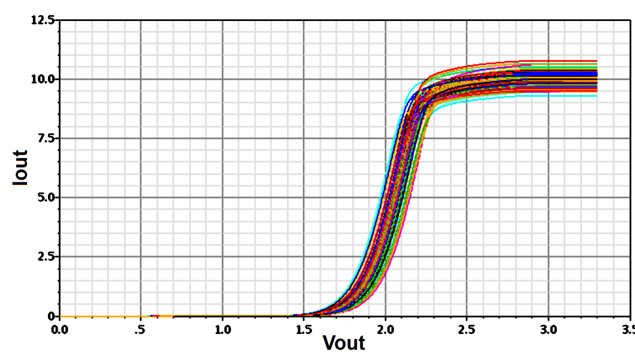

Figure 2: Output current variation of the Fig. 1a circuit [4].

Results of these simple tests were among reasons of subjecting more complex structures to Monte-Carlo and other less typical simulations to study real-life effects on operation quality of the subjected circuits.

3 CIRCUITS UNDER SIMULATION

During studies on MAPS sensors three main circuits were taken into account. All of them were already designed and simulated structures expected to be manufactured when opportunity arises. The simulated circuits are:

1. Rolling-shutter binary readout circuit, presented in Figs. 4 and 5 and described in [5];
2. Shaperless front end (SFE) active pixel of Fig. 6, described in [6];
3. Reduced pitch ampli-shaper-discriminator block presented in Fig. 7, work related to those presented in reference [7].

Circuit one is a switched-power solution using a chain of pretuned simple low-gain amplifier stages. Circuit 2 and 3 are more typical solutions working continuously. Circuit 2 has ability of quantitative charge hit analysis while circuit 3 is setup for only a qualitative detection of charge hit occurrence. For the discussed tests all three circuits were setup for qualitative hit detection of a defined charge.

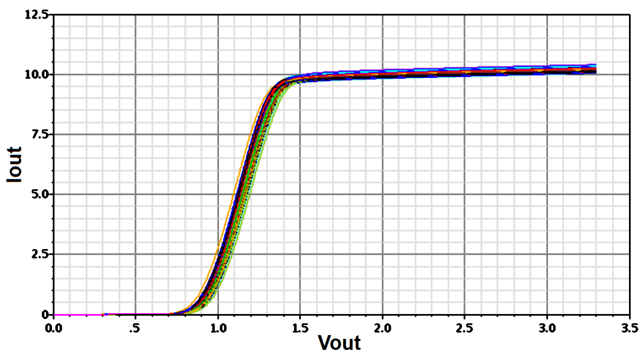

Figure 3: Output current variation of the Fig. 1b circuit [4].

1 SIMULATION SETUP

In case of simulated circuits the pixel circuitry is implemented in XFAB 0.6 µm process, all remaining parts of signal-paths are implemented in Global Foundries 130 nm process. Such a solution simulates a 3D structure that utilized two different wafer one on top of another. The result is that if whole circuits are to be simulated at once, two design kit model set must be setup and used together.

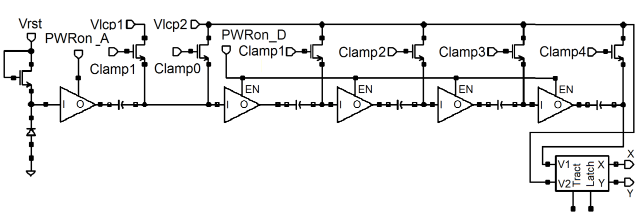

Figure 4: Rolling-shutter pixel circuit [3].

This setup required adaptation of design kit models, e.g. for avoiding same device model names in different model kits. If was found to be feasible to simultaneously run all required simulations for both design kit models. Main goal of the extended simulational test of the designed circuits was to partially simulated tests conducted on manufactured specimens of integrated structures and thus to try and find some possible problems before the circuits are in fact send for production and any changes cannot be introduced any more.

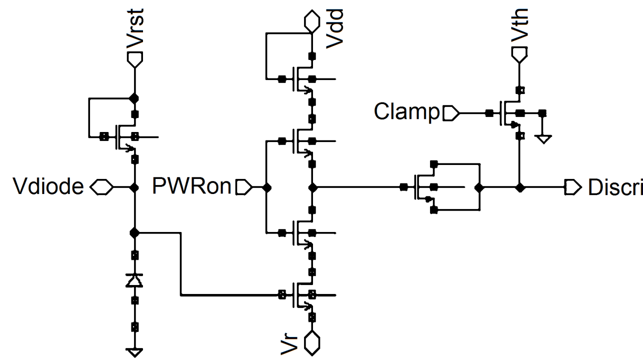

Figure 5: Amplifiers of the rolling-shutter pixel circuit [3].

Limitations of real life technology processes are simulated by Monte Carlo (MC) simulations for available process corner definitions. It is important to note that only local process variations – device mismatch (DM) - were taken into account in the conducted simulations.

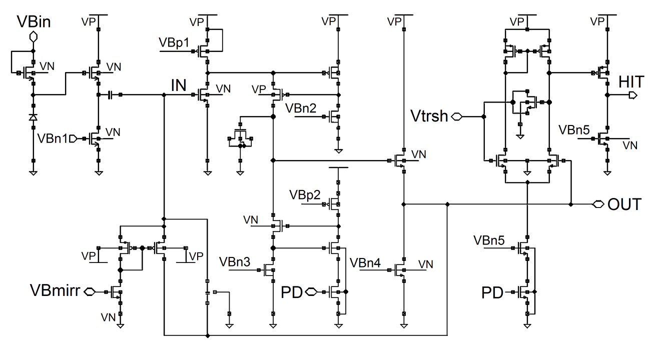

Figure 6: Shaperless front end (SFE) active pixel circuit [3].

Real life environment of integrated circuit operation is simulated by application of transient domain (TD) noise simulations. As a rule, all performed simulations are time domain simulation to include most of possible phenomena present in the simulated circuit structures.

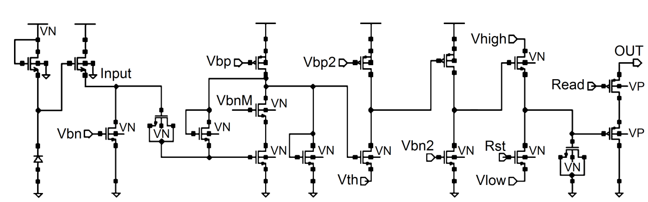

Figure 7: Reduced pitch ampli-shaper-discriminator [3].

All the circuits are tuned to detect a short current surge equivalent to 100e- charge hit with 50 % probability. Single simulation set comprises of 100 simulation runs. Three main simulation sets are performed.

- MC DM simulations.
- TD noise simulations.
- Mixed MC DM with TD noise simulation (ten MC DM sets for each of ten noise patterns).

Time domain noise simulation used the same models as AC noise simulations, but time domain simulations are very time consuming. It is only possible to include limited frequency range of the noise pattern. The lower frequency is limited by total transient simulation time while the upper frequency is limited by minimal simulation step. A few multi-core computers where employed to limit the overall circuit analyses duration.

1 SIMULATION RESULTS

During studies on the three introduced circuits it was found that generally that both circuits working with continuously present power supply have similar resilience against MC DM effects. Similar behavior was found for TD noise simulation. The switched-power solution, however, revealed significantly different behavior. It was found to offer superior operation quality in presence of MC DM variations. This was an expected effect as the whole circuit structure was devised with such a goal in mind [5].

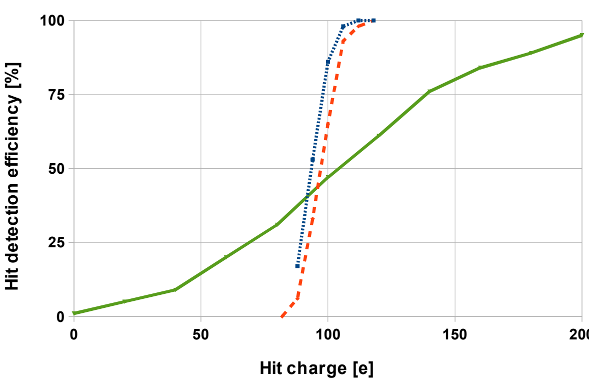

Figure 8: Influence of TD noise [3] on: rolling-shutter binary readout circuit (solid green line), shaperless front end (SFE) active pixel (dashed red line), reduced pitch ampli-shaper-discriminator (dotted blue line).

Though, results of TD noise simulation showed significant problems. Fig. 8 shows number of hit detections in set of 100 simulations in function of hit charge. It can be seen that resolution of the switched-power rolling-shutter circuit is significantly inferior in comparison to both other circuits. At first it was not obvious if it is manifestation of a design error or just a non-typical property of such a non-typical solution. Time domain curves were inspected and it was found that there is a problem with providing proper analog signal to a latching module. Fig. 9 presents this output signal and latching signal in presence of MC DM variations. Fig. 10 presents the same signals in presence of TD noise patterns. Simulation with both MC DM and TD noise effects provides results similar to those presented in Fig. 10. It is then obvious that a design problem has been encountered.

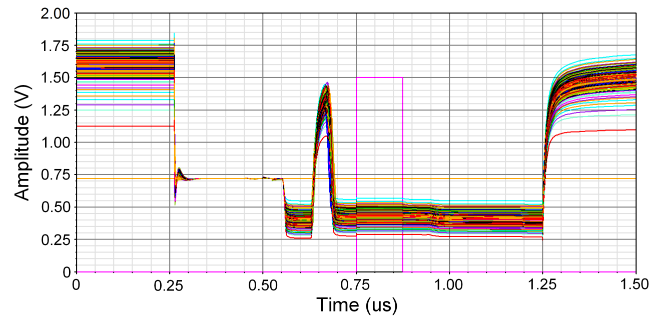

Figure 9: Rolling-shutter pixel circuit [3]: input signal of the analog latch module and the latching signal in presence of device mismatch – 100 simulation runs.

Thorough analysis of the encountered problem showed that the control sequence is to be blamed and luckily the hardware does not necessarily need to be redesigned, as control sequence is provided externally. In detail, the first of amplifier chain (the one placed on the XFAB process tier) is not powered when the circuit gets reset / re-biased before next hit gathering phase. Due to such setup, there is no control over state of output of this amplifier, as it is connected to a capacitor used in re-biasing process. In addition, this capacitor is a MOS-based device and its capacitance depends on voltage drop between its terminals. So, if there is no control of voltage on one of its terminals, there is no precise knowing what its capacitance is.

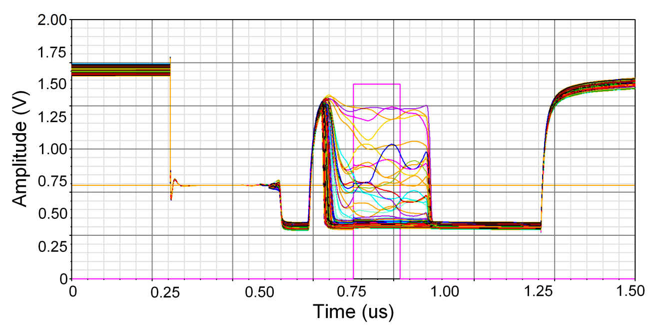

Figure 10: Rolling-shutter pixel circuit [3]: input signal of the analog latch module and the latching signal in presence of transient noise – 100 simulation runs.

The control sequence was redesigned and MC DM and TD noise analyses were repeated for the modified version of the circuit. Fig. 11 presents obtained TD noise results for all three circuits under test. It can be observed that now the rolling-shutter circuit offers operation quality at least similar to remaining circuits. In fact, quality of its resilience against local variations of the technology process got slightly deteriorated, but is still far better than for two other MAPS circuits under simulation. Fig. 12 presents operation quality of all the simulated circuits in presence of MC DM process variations.

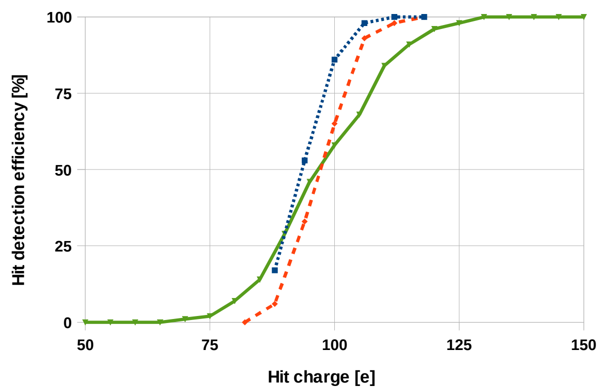

Figure 11: Influence of TD noise [3] on: rolling-shutter binary readout circuit (solid green line) with modified control signal configuration, shaperless front end (SFE) active pixel (dashed red line), reduced pitch ampli-shaper-discriminator block (dotted blue line).

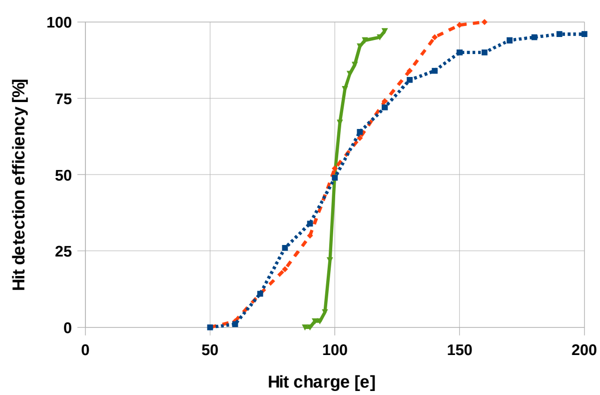

Figure 12: Influence of MC DM variations on: rolling-shutter Binary Readout circuit (solid green line), shaperless front end (SFE) active pixel (dashed red line), reduced pitch ampli-shaper-discriminator block (dotted blue line), with modified control signal configuration.

2 CONCLUSIONS

Rolling-shutter binary readout circuit, shaperless front end (SFE) active pixel and reduced pitch ampli-shaper-discriminator block existing solutions were selected and tested. Unpredicted phenomenon in the first of listed circuits under simulation is detected; its cause tracked down and removed. Conveniently (and luckily for a designer), the problem is found to be manageable solely by means of control signal sequence modifications, with no hardware alterations required. The circuit driven with original control sequence shows potentially very serious problems with immunity to noise, not observed earlier during typical simulations conducted for tracking such issues.

Presented considerations show importance of detailed simulational analysis of circuits in their design phase. In the presented design examples importance of MC device matching and TD noise simulations for revealing possible problems has been presented. The key is time-domain for performing detailed simulation.

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