High-voltage Edge-rounded Trapezoidal Waveform Generators

M. Jankowski, Member, IEEE, and A. Napieralski, Senior Member, IEEE

Department of Microelectronics and Computer Science, Lodz University of Technology Wolczanska 221/223, 90-924 Lodz, Poland, jankowsk@dmcs.pl

ABSTRACT

An approach to design low-voltage and high-voltage trapezoidal waveform generators with edge-rounding ability is described. The paper presents circuits able to produce edge-rounded trapezoidal waveforms, endowed with several means of waveform parameter adjustments. Signal paths in the presented circuits are very short. Most of additional circuitry is placed outside signal paths. Circuit solutions as well as simulational test results are presented and discussed.

Keywords: high-voltage circuits, SOI integrated circuits, trapezoidal waveform generation

1 INTRODUCTION

Trapezoidal waveforms find many applications both digital and analog electronics. There are numerous cases trapezoidal, triangular or more complex pulse shapes are applied instead of square pulses, because such an approach reduces harmonics and thus helps reaching EMC requirements of electronic equipment.

Non-obvious (neither sine nor square) pulses tend to be used in wireless transmission systems. They are signals of choice because EMC requirements are especially high in such systems (signal harmonics can be harmful), though transmissions should be easily decodable. Thus, both square and sine waves are quite often found not optimal solutions. This issue exists among others in case of popular low-cost low-energy and low-range systems using Radio-Frequency Identification (RFID) or several similar protocols. Such transmission systems are present in modern electronics, both specialized systems and mass-production systems.

2 LOW-VOLTAGE GENERATORS AND EDGE-ROUNDERS

Trapezoidal waveform generation can be conducted in various ways. One of classic ways is application of a capacitor as an integrating device charged/discharged with constant currents. Several distinct circuit solutions using mentioned mode of operation are patented [1]. Though most of them are voltage domain circuits and use OPAMPs in signal path, ways of integrating capacitor implementation may differ. Patented solution presented in [2] uses capacitors in OPAMP feedback. Though, circuitry presented in [3] shows how complicated the adjustable

waveform generator can get if based solely on voltagemode function blocks. There are also patented solutions for waveform edge-rounding systems in various systems [4].

Solutions presented in this paper produce voltage-mode waveforms, though current flow control plays important role in generator operation. Though, it is also worth mentioning that it is possible to directly generate various current-mode waveforms, e.g. with use of transconductors.

Authors and their co-workers had opportunity to work on low-voltage (LV) trapezoidal waveform generators with edge-rounding capabilities. Several structures were used for obtaining edge-rounding effect.

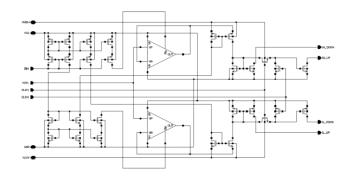


Figure 1: Voltage-range limiting and edge-rounding circuitry using current-stealing from generator module [5].

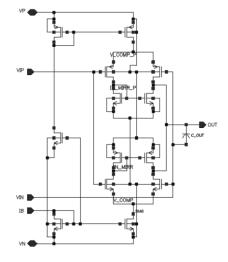


Figure 2: Edge-rounding circuitry based on usage of OPAMP limitations [6].

Structure with current-mirrors stealing current from trapezoidal waveform generation module presented in

Fig. 1 [5], with interconnected simple OPAMPs (Fig. 2) working at edge of their active ranges to generate nonlinear effects on input waveforms [6] were tested.

Interesting solution is a multi-OPAMP structure using diode-resistor non-linear voltage dividers and voltage level preprogramming, proposed in [7] and presented in Fig. 3.

In all the circuits trapezoidal waveforms were generated with use of current-mode stage used for charging/discharging a capacitor.

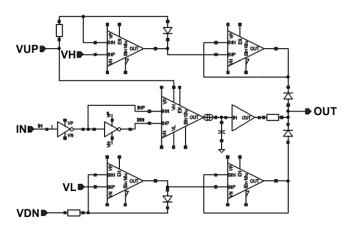


Figure 3: LV edge-rounding circuit presented in [7], later used as a concept prototype for an HV structure.

3 HIGH-VOLTAGE GENERATORS AND EDGE-ROUNDERS

3.1 Process and Simulation Information

All circuits discussed in this section are designed and simulated with Cadence IC Virtuoso and design kit for 0.8 um SOI HV CMOS commercial process. Low supply voltage is always 5 V, high supply voltage is 16 V to 30 V.

3.2 Trapezoidal Waveform Generation

Waveform generation for the HV edge-rounding circuitry is provided by circuit that is based on principle of charging/discharging of an output capacitance [7], exactly like in case of [5], [6] and [7] LV and solutions. Generally, current-mode approach makes LV circuits easier to be adapted to HV operating conditions. Output of the HV generator cannot accept any other loads than its capacitor. Thus, it is followed by a high input-impedance unity-gain buffer devised by one of authors and patented by an industrial company [8].

3.3 Edge-rounding Circuitry

Function-block for HV systems not always can be directly derived from their LV counterparts. The problem is that many LV solutions are based on OPAMPs and such components are difficult for efficient implementation in HV

systems for HV operation. This is difficult especially in case of ensuring high swing of input signal provided to an OPAMP differential pair structure. Many existing edge-rounding topologies were studied by authors, including their own ideas for LV IC systems. It was found that topology presented in Fig. 3 is most universal and offers best operation quality. Though it is based on OPAMPs, most of its signal processing is related to generation and dissemination of DC currents of precisely defined value. Thus, it was checked and found possible to exchange all OPAMP-based sub-blocks with high-quality current-mirror based structures.

Block diagram of the HV edge-rounding circuitry is presented in Fig. 4 and details of its operation are as follows [7]: this function block has two pairs of inputs. VSH and VSL are for providing voltage-range of the input trapezoidal waveform in form of DC voltages equal to minimum and maximum voltages of the waveform. VUP and VDN are for providing required voltage-range of output edge rounded waveform. Input stages of the edge-rounding module convert voltage differences (VSH-VUP) and (VSL-VDN) into currents and conversion ratio is equal to value of the resistor in the output diode-resistor voltage-divider. Structure of V/I converters used in this stage is based on folded-cascode mirrors. It is presented in Fig. 5 and discussed in [9].

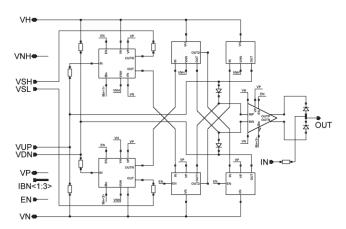


Figure 4: HV edge-rounding circuitry with short signal-path.

The current that flows through the output voltage divider flows through both the resistor and one of the diodes. Current flow through the diode causes voltage drop between input and output waveforms, especially when the input waveform reaches its minimum/maximum voltages.

All resistors in this circuit have same value and all current-mirrors have unity gain. Thus, output currents of the V/I converters are equal to currents flowing through the output divider resistor and diodes for maximum/minimum voltages of the input trapezoidal waveform fed into the edge-rounding circuitry. Owing to this feature, it is possible to recreate maximum voltage drops on the output divider diodes, by means of forcing through these diodes current

identical as in the output resistor-diode divider. This is done with use of auxiliary diodes identical to the output diodes. Required currents are produces by set of precise current-mirrors fed by the V/I converters. Voltage drops produces on auxiliary diodes are then respectively subtracted from VUP voltage and added to VDN voltage. Obtained auxiliary voltage levels feed inputs of two high input impedance unity-gain buffers [8]. These buffers are general purpose modules but in the discussed circuitry they act as auxiliary supply and ground sources used to bias and power resistor and diodes of the output voltage divider.

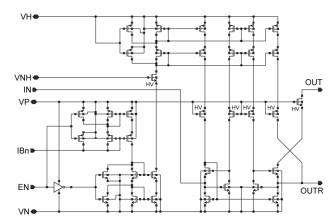


Figure 5: Regulated-cascode current-mirror V/I converter used in edge-rounding circuitry.

Due to such operation, presence of VSH and VSL voltages at input of the output voltage divider produces voltage drops on output diodes that alter minimum/maximum output voltage levels of the divider back to values precisely equal to VUP and VDN, respectively. Voltage-range of the output waveform can thus be precisely controlled.

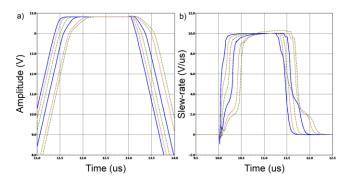


Figure 6: Waveform shape (a) and slew-rate value (b) for different current values; the less current, the more edge-rounding can be observed.

It can be said that due to highly non-linear operation of the resistor-diode output voltage-divider for minimum and maximum voltages of the input waveform, it gets squeezed in its extremities and thus this rounding effect is produced. The circuit presented in this section requires some auxiliary circuitry required for providing its own functionality. But there are strong assets of the presented solution. First, most of this additional circuitry (except for the output resistor-diode voltage divider) works with DC currents and voltages and thus is not prone to mane limitations typical for AC operation solutions.

Even more important asset is that most of this auxiliary circuitry does not propagate processed waveforms as it stays outside the signal-path of the edge-rounding circuitry. From the signal-path point of view, all this structure is reduced to the output resistor-diode voltage divider, with only a single resistor between input and output of the rounding module.

3.4 Simulation results

The designed circuitry was simulated for study purposes and first of all it was found that the waveform generator itself provides some edge-rounding functionality. Amount of edge-rounding is related to current used for charging/discharging of the output capacitor. The less current is used, the more edge-rounding effect is pronounced [7], as presented in Fig. 6. Though the effect is helpful it does not provide required level of edge-rounding and additional circuit for completing this task is still required. The edge-rounding circuitry needs high voltagerange input waveforms to provide sufficient amount of edge-rounding by cost of the output waveform voltagerange reduction. Thus, it was found that if high-swing rounded output waveform is required, the waveform accessible at the output of the edge-rounding circuitry should be amplified around half the high supply voltage.

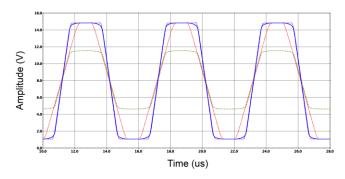


Figure 7: Output waveforms: trapezoidal waveform generator (dashed), waveform generator for edge-rounding circuitry (dotted), edge-rounding circuit output before (dash-dotted) and after amplification to full voltage-range (solid).

Amplification of the output waveform further increases edge-rounding effect. Also, input waveform slew-rate should be reduced by output voltage gain, but gain of such an amplifier should be low, in order not to shift noise and other signal artefacts up in frequency range. Fig. 7 presents

shapes of input and output signals of the waveform generator and edge-rounding circuitry [7].

Fig. 8 presents slew-rate of the input and output waveforms of the edge-rounding circuitry. Reduced slew-rate value for the input waveform and limited edge-rounding effect and be also observed [7].

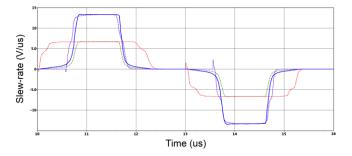


Figure 8: Slew-rates of input (low value) and output (high value) waveforms of the edge-rounding circuity.

Amount of edge-rounding effect can be better observed with use of DFT of specific signals. Fig. 9 presents DFTs for waveforms generated by trapezoidal generator working with high and low output capacitor current values – less and more edge-rounding effect, respectively; Fig. 9 also shows output waveforms of the edge-rounding module fed with each of abovementioned input waveforms [7]. It can be observed that input waveform generated with smaller capacitor current has fewer harmonics and that this effect is retained in the output signal from the edge-rounding block.

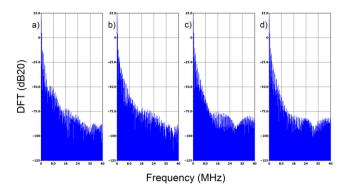


Figure 9: DFT of: generator waveform with high (a) and low (b) capacitor current; output waveforms of rounding block fed with a) and b) signals – (c) and (d), respectively.

4 CONCLUSIONS

Authors' own works show that purely current-mode HV generator with voltage buffer and edge-rounding circuitry at output can produce a circuit able to provide waveform with parameterized slew-rate, voltage-range, operation frequency and harmonics reduction through waveform edge-rounding.

Circuit structures presented in this paper are results of authors' research on possibilities of current-mode circuitry application in HV integrated circuits. The developed circuits show ability of providing functionality while having extremely short signal paths. Offered functions, like signal shape, slew-rate control, and harmonics attenuation widens fields of the circuit possible application in industry-intended HV systems, e.g. wireless ones.

Specific assets of presented solution enable design of complete waveform generation and conditioning signal paths for modern SoI HV integrated systems.

REFERENCES

- [1] US Patent No. 5,642,067, "Variable Slew Rate Pulse Generator," Inventor: James W. Grace; Filed: Jun. 26, 1995; Date of Patent: Jun. 24, 1997.
- [2] US Patent No.5,025,172, "Clock Generator Generating Trapezoidal Waveform," Inventor: Kenneth J. Carroll, Benjamin D. Pless; Assignee: Ventritex, Inc., Sunnyvale, Calif.; Date of Patent: Jun. 18, 1991.
- [3] V. F. Tarasov, "A trapezoidal pulse generator with independent adjustments of amplitude and slopes of leading and trailing edges," Instruments & Exp. Techniques, Vol. 54, pp 372-374, 2011.
- [4] United States Patent No.: US 7,154,310 B2, "Trapezoid Signal Generating Circuit," Inventor: Akio Kojima, Nukata-gun; Assignee: Denso Corporation; Filed: Oct. 7, 2004; Date of Patent: Dec. 26, 2006.
- [5] M. Jankowski, "Adjustable output voltage-range trapezoidal waveform generator with harmonicsreduction functionality," in Proceedings of the 9th International Conference TCSET'2008, Modern Problems of Radio Engineering, Telecommunications and Computer Science, Lviv-Slavsko, Ukraine, Feb. 2008, pp. 19-23.
- [6] M. Jankowski, "Adjustable Output Voltage-Range and Slew-Rate Trapezoidal Waveform Generator with Harmonics-Reduction Ability," International Conference CADSM2011, Polyana-Svalyava (Zakarpattya), Ukraine, 23-25 February, 2011.
- [7] M. Jankowski, A. Napieralski, "High-voltage Trapezoidal Waveform Generator with Edgerounding Functionality Implementations," Proceedings of the 21st International Conference Mixed Design of Integrated Circuits & Systems (MIXDES), Lublin, Poland, 2014, pp. 224-229.
- [8] Patent issued by Polish Patent Office "Uklad bufora napieciowego," (eng. "Voltage Buffer Circuit"), inventor: Jankowski Mariusz, designee: Automatix spółka z o.o., exclusive right kind and number WYN: (11) 212837, granted: 19 June 2012, published: 22 June 2012.
- [9] M. Jankowski, A. Napieralski, "Current-mode Signal Processing Implementation in HV SoI Integrated Systems," Microelectronics Journal, Volume 45, Issue 7, July 2014, Pages 946–959.