The Heat transfer in Fin-FET transistor

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ABSTRACT

The dynamic thermal behaviour of 12nm FinFET transistor for the Fourier-Kirchhoff equation and the Dual-Phase-Lag model has been presented in the paper. The authors show a slower growth of temperature in the FinFET nanometric structure in the case of Dual-Phase-Lag model than by using the Fourier-Kirchhoff model

Keywords: Fourier-Kirchhoff equation, Dual-Phase-Lag model, FinFET, Knudsen number

1 INTRODUCTION

The electro-thermal analysis is one of the most important development steps in the professional design of analogue submicron electronic Integrated Circuits (ICs), power modules design process as well as the modern nanostructures. That kind of analysis is useful to both the power density and the operating conditions estimation (e.g. the electronic circuit operating point, the temperature dependence of electronic device properties as well as the maximum operating circuit temperature).

In general, the heat transfer in a thermally conducting solid medium can be described correctly by using the classical Fourier law (1) and the resulting Fourier-Kirchhoff (F-K) heat equation (2)

$$\vec{q}\left(x,y,z,t\right) = -\lambda\ \nabla T\left(x,y,z,t\right) \tag{1}$$

$$\frac{\partial}{\partial t}\left(c_p\ \rho\ T\left(x,y,z,t\right)\right) = = -\nabla\cdot\vec{q}\left(x,y,z,t\right) + q_{gen}\left(x,y,z,t\right) \tag{2}$$

with mixed boundary conditions, where $T(x,y,z,t)$ represents the temperature distribution in ICs, $q(x,y,z,t)$ is the heat flux, $q_{gen}(x,y,z,t)$ is an internal generated heat density, λ is the thermal conductance, c_p is a specific heat capacity and ρ means the material density.

Unfortunately, the Fourier-Kirchhoff equation postulates some nonphysical behaviours such as:

- heat propagating with infinite speed and
- instantenous change of both the heat flux and the temperature gradient,

what does not agree with experiments in [1], [2]. Another problem is related to the development of the semiconductor manufacturing technology which causes the extreme miniaturization of the device size up-to 14 nm, for example in case of MOSFETs used in the family of Intel Broadwell CPU or in the prototyped 6 nm FinFETs technology [3] and even in a nanowire and a nanotube manufacturing technology. In all of these cases the dimensionless Knudsen number (Kn), which is defined as the ratio of the average free path to the characteristic structure length, is considerably more higher than the unity due to the fact that the phonon free path at 300 K is around 41.8 nm in case of the silicon [4]. It causes that the F-K equation cannot be applied. Therefore, the ballistic heat transport model should be taken into consideration in the mathematical description of the heat transfer (see Fig. 1 and more in [5], [6]).

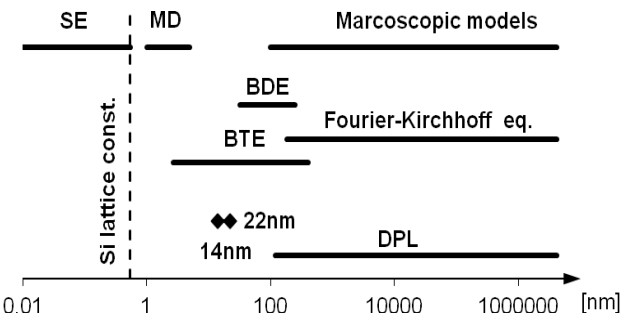

Fig. 1. The estimated scope of the heat transfer model applicability in silicon for the Molecular Dynamics simulation (MD), Schrödinger Equation (SE), Boltzmann Transport Equation (BTE), Macroscopic Energy Treatement using the Fourier-Kirchhoff equation, Ballistic - Diffusive Equation (BDE) – solid lines description; the Intel CPU Broadwell (14 nm, 2.9 GHz) and the Haswell family (22 nm, 4.4 GHz) has been pointed-out using black points; the silicon lattice constant has been marked using dashed lines.

2 THE THERMAL MODEL

The electro-thermal F-K model of FinFET transistor has been already precisely presented by the team of prof. A. Asenova in [7]. In [7] the classical Fourier-Kirchhoff

equation with the special correction for the nanoscale has been applied. Based on the Dual-Phase-Lag (DPL) model [5], [8], [9], the heat transport in FinFET can be approximated by the following equation:

$$c_v \frac{\partial T}{\partial t} + c_v \tau_q \frac{\partial^2 T}{\partial t^2} \cong \nabla \cdot (k \nabla T) + \nabla \cdot \left(k \tau_T \frac{\partial}{\partial t} \nabla T \right) + q_{gen} \quad (3)$$

where τ_q is a very small constant. Assuming the finite slope of the heat flux changes according to the following formula:

$$q_{gen} \gg \tau_q \frac{\partial q_{gen}}{\partial t} \quad (4)$$

The Equation (3) can be reduced to the parabolic equation system

$$\begin{bmatrix} 1 & 0 \\ 0 & \tau_q c_v \end{bmatrix} \cdot \frac{\partial \mathbf{u}}{\partial t} - \nabla \cdot \left(\begin{bmatrix} 0 & 0 \\ k & k\tau_T \end{bmatrix} \nabla \mathbf{u} \right) + \begin{bmatrix} 0 & -1 \\ 0 & c_v \tau_q \end{bmatrix} \cdot \mathbf{u} = \begin{bmatrix} 0 \\ q_{gen} \end{bmatrix} \quad (5)$$

where $\mathbf{u}$ is the column vector, which comprises the primary solution of the equation (3) due to the temperature variable ($\mathbf{T}$) as well as the first time derivative of the temperature ($\boldsymbol{\theta}$):

$$\mathbf{u} = \begin{bmatrix} \mathbf{T} \\ \boldsymbol{\theta} \end{bmatrix}. \quad (6)$$

3 RESULTS ON THE EXAMPLE OF THE FINFET TRANSISTOR

The classical Fourier-Kirchhoff description of the heat transfer in FinFET transistor has been accurately circumscribed for the steady-state by the prof. A. Asenova's team in [7]. However, the dynamic behaviour for the large Knudsen numbers is very important for modern Integrated Circuits, therefore it will be considered in the paper.

We will focus on the 12 nm FinFET transistor presented in [7]. For that device, the length of the channel is 25 nm, the width of the fin is 12 nm, the thickness of the dielectric between the fin and the gate is 0.8 nm, while the fin height is 30nm. Moreover, the 6 nm spacers are introduced on both sides of the gate. The thickness of high-k gate dielectric (Equivalent Oxide Thickness, EOT) is 0.8 nm and the depth of the Buried Oxide (BOX) is 30 nm. The following material parameters has been taken: c_v=1.66 MJ/(m^3 K); k=1.38, 30 and 148 W/(m K) for polisilicon gate, high-k gate dielectric and other, respectively. The DPL heat flow model delays were also assumed as follows: τ_q=3 ps, τ_T=60 ps. The PDE has been approximated by using the Finite Element Method (FEM – 7333 triangles; $\mathbf{T}$ as well as $\boldsymbol{\theta}$ – 7232 points) together with the fifth-order Gear predictor-corrector algorithm. The boundary and initial conditions are as follows:

$$\bullet(x, y, t) = 0 \quad \text{for} \quad y = -30\text{nm} \quad (7)$$

$$\frac{\partial \bullet(x, y, t)}{\partial x} = 0 \quad \text{for} \quad x = 0 \vee x = 20\text{nm} \quad (8)$$

$$\frac{\partial \bullet(x, y, t)}{\partial y} = 0 \quad \text{for} \quad x = 60\text{nm} \quad (9)$$

$$T(x, y, t) = \begin{cases} 1(t) & \text{inside chanell} \\ 0 & \text{outside chanell} \end{cases} \quad (10)$$

$$\theta(x, y, t) = 0 \quad \text{for} \quad t = 0 \quad (11)$$

where $\bullet$ means both T and θ. The computation results are presented in normalized form as the temperature rise related to the maximum steady-state temperature obtained for the Fourier-Kirchhoff model. It should be noted that the maximum temperature is in the point (0, 29.1153 nm, see Fig. 2) localised near the polisilicon gate and the dielectric gate, therefore that area should strengthen during the manufacuring process or the thermo-mechanical properties of mentioned area should be carefully analised.

Obtained simulations shows that the temperature rise is slower in the DPL than in the F-K model (see Fig. 4). The precise value of delay can be calculated using the channel average temperature. Moreover, that value is mostly comparable with τ_T for τ_T/ ($2\tau_q$)=20 (see Fig. 3).

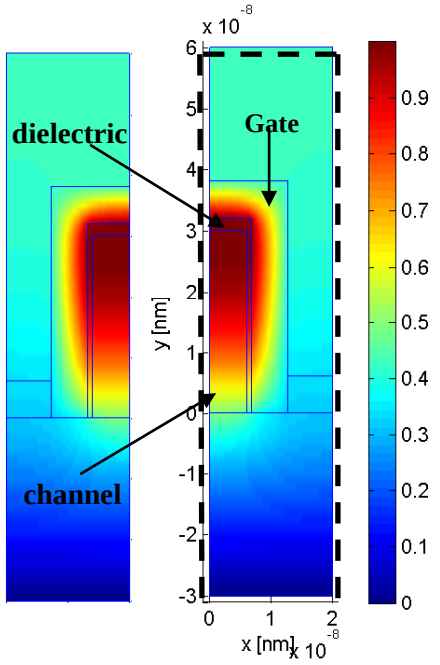

Fig. 2. The temperature distribution of the 12nm FINFET transistor normalized to its maximum temperature. The normalization is performed for the maximum lattice peak of the temperature.

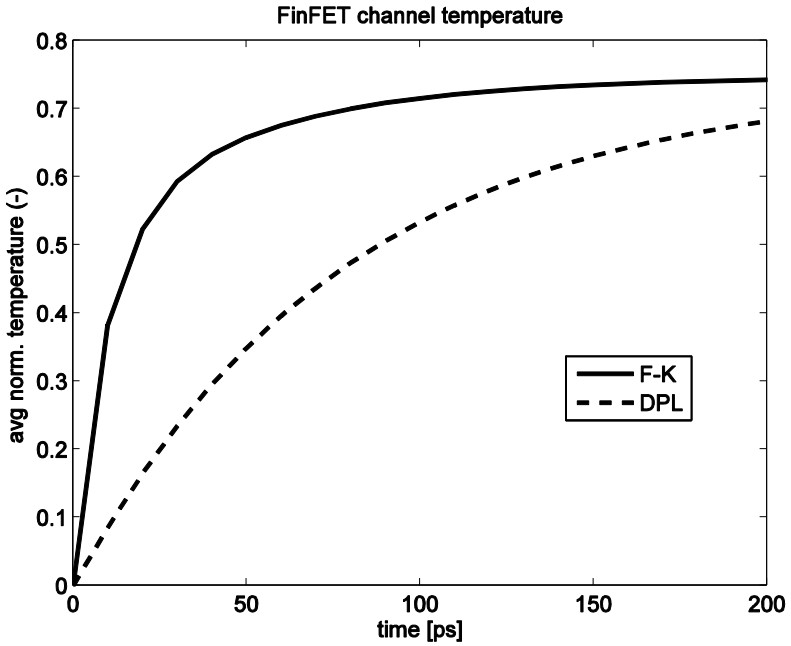

Fig. 3. The comparison of the average normalized temperature rise of 12 nm FinFET channel for both the F-K and the DPL models. The normalization is performed for the maximum temperature obtained in the steady-state simulation.

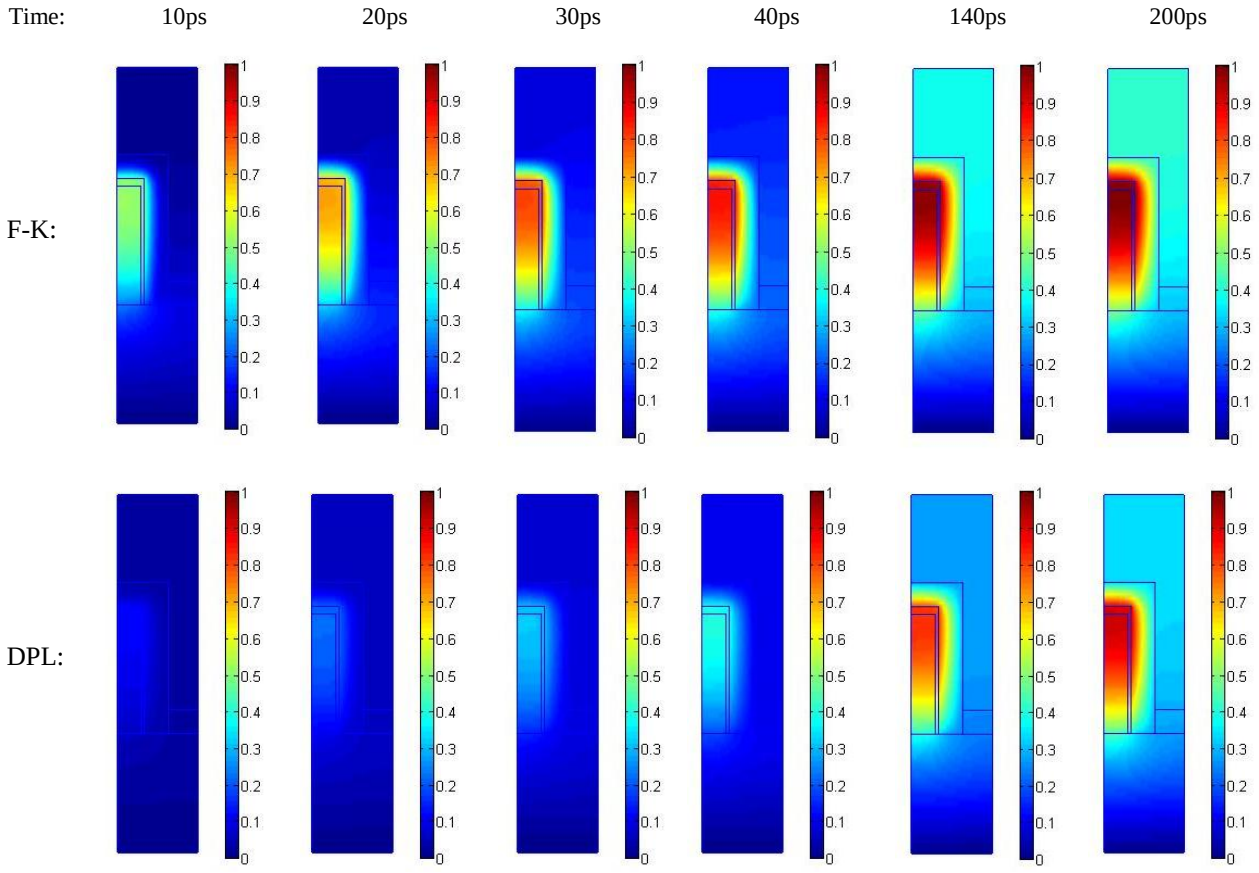

Fig. 4. The temperature rise distribution in the 12 nm FinFET at 10, 20, 30, 40, 140 and 200 ps for the DPL and the F-K models. The normalization is performed for the maximum temperature obtained in the steady-state simulation.

4 CONCLUSIONS

Presented analisys is based on the comparision of the dynamic behaviours of the DPL and the F-K model for the chosen value of the parameter τ_q. The symmetry of the modeling of many transistors arranged next to each other and the uniform distribution of the current density in the channel were also assumed.

For these simplifying assumptions, we noticed a slower growth of temperature in the FinFET nanometric structure in the case of DPL model than by using the F-K model, which is shown in Fig. 3. The future research will endeavor to compare presented results with the Ballistic-Diffusive Equations heat transfer model.

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