

TCAD Analysis of Frequency Dependent Intrinsic and Extrinsic Parameters of GEWE-SiNW MOSFET

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ABSTRACT

In this paper, extrinsic parameters of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET are analyzed in terms of parasitics capacitances, resistances and inductances using 3D-TCAD device quantum simulations. All simulations have been performed using ATLAS and DEVEDIT-3D device simulators. Simulation results reveal significant reduction in intrinsic and extrinsic parameters of GEWE-SiNW in comparison to its conventional SiNW MOSFET. Also, significant improvement in the intrinsic gate and drain transconductance of GEWE-SiNW in comparison its counterpart. Hence, provide its efficacy in high speed switching applications.

Keywords: Gate Electrode workfunction engineering, Quantum Model, Transconductance, Intrinsic and Extrinsic Parameters, Silicon Nanowire MOSFET.

1. INTRODUCTION

Highly scaled CMOS device achieved cut-off frequencies in the range of 10-100 GHz making CMOS technology appropriate for HF and mobile applications [1-4]. However, with scaling down the device dimensions, the so-called Short Channel Effect arises such as mobility degradation, hot carrier effects, drain induced barrier lowering, parasitic capacitances etc. making the scaled devices inapt for high frequency applications [3]. From past few years, new novel device structures such as multi-gate, silicon-on-insulator and silicon nanowire MOSFET have been proposed as promising candidates to overcome the problem of scaling in bulk MOSFET [4-5].

Among them, cylindrical gate MOSFET [6-7] has emerged as a most promising candidate in recent years. Since, it allows excellent electrostatic control of the gate charges over the channel hence overcoming the scaling limitations caused due to the SCEs, thereby improving the device performance. Furthermore, silicon Nanowire MOSFET is receiving more scrutiny for its advantages of reduced short channel effects, high on-current and improved carrier efficiency [8-10], which are the predominant factors that limit how far a MOSFET can be scaled. Also it was proven that it has a merit of outstanding maximum oscillation frequency (f_{MAX}) [11].

In this paper, extrinsic parameters of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET are analyzed in terms of parasitics capacitances, resistances and inductances using 3D-TCAD device simulations. The extracted parameters have been compared with those of conventional SiNW MOSFET with identical device geometry.

2. DEVICE STRUCTURE AND METHODOLOGY

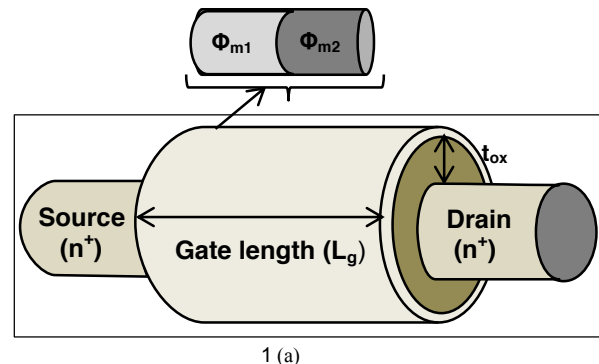


Fig.1 Simulated device structure of (a) SiNW MOSFET and (b) GEWE-SiNW MOSFET

Fig. 1(a-b) shows the simulated 3D device structure of SiNW and GEWE-SiNW MOSFET respectively. All simulations have been performed using ATLAS and DEVEDIT 3D device simulator. The Source/Drain region is highly doped with n-type impurity of $5 \times 10^{19} \text{ cm}^{-3}$. While the silicon nanowire is doped with a p-type impurity of $1 \times 10^{16} \text{ cm}^{-3}$ and t_{ox} thick oxide layer of 1.5nm is embodied in it as shown in Fig.1 The device radius and channel length are 5nm and 30nm respectively. Length of region 1 (L_1) and region 2 (L_2) are 15nm each. In order to fairly analyze the device performances, both the devices are optimized to have the same threshold voltage, i.e., 0.4V. In this simulation all the junctions of the structure are assumed as abrupt and the biasing conditions are considered at room temperature ($T=300\text{K}$) and the doping profiles are uniform. Further, two numerical techniques Gummel and Newton have been considered to obtain the solutions [17]. To obtain the convergence in the inversion region, the DIRECT parameter is added for more

robust solution. In our simulation, we have adopted the Bohm Quantum mechanical model [2] since because the inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension.

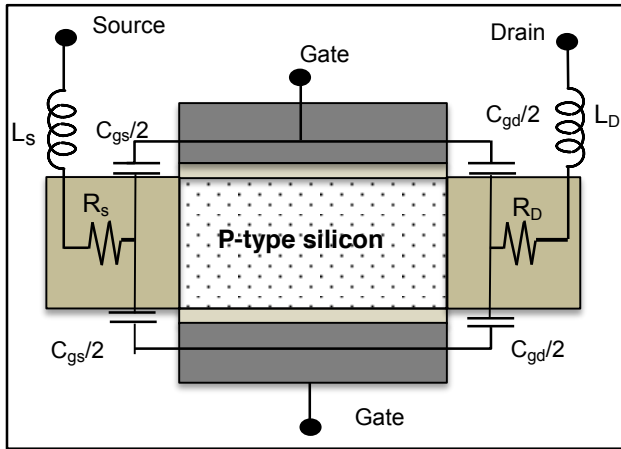


Fig.2 Schematic representation of Equivalent circuit of a SiNW MOSFET in an unbiased condition ($V_{gs}=0V$).

Fig. 2 shows the equivalent circuit of silicon nanowire MOSFET at zero gate bias. C_{gd} and C_{gs} are extrinsic gate-to-drain and gate-to-source capacitances, respectively. R_s and R_d are the source and drain resistances, respectively. L_s , L_d and L_g are source, drain and gate extrinsic inductances respectively. The values of R_d , R_s , L_d , L_s , C_{gs} and C_{gd} were extracted at zero gate bias, which is an OFF-state of the device.

3. RESULTS AND DISCUSSIONS

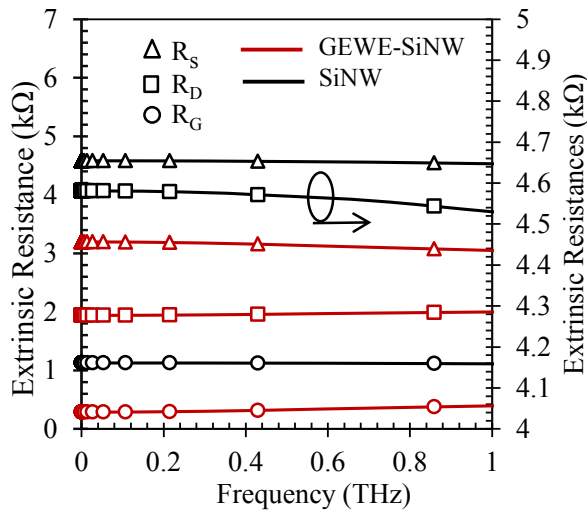


Fig. 3(a): Extrinsic Resistance as a function of frequency for Conventional SiNW and GEWE-SiNW MOSFET at $V_{ds}=0V$ and $V_{gs}=0V$

Fig. 3(a-c) shows the extrinsic parameters of GEWE-SiNW MOSFET in comparison to conventional SiNW MOSFET. As is evident from Fig. 3(a), intrinsic source, drain

and gate resistances are comparatively lower in comparison to SiNW MOSFET. Similarly, intrinsic capacitances and inductances reduce in our device compared to SiNW MOSFET.

These extrinsic parameters were determined by using the zero-biased and pinch-off cold FET methods, as described in [8-9], and the results were summarized in Table I. The detailed procedure for extracting these parameters was not explained here.

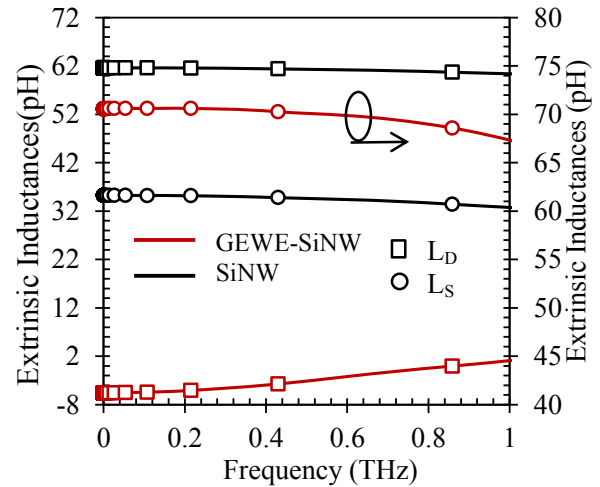


Fig. 3(b): Extrinsic Inductance as a function of frequency for Conventional SiNW and GEWE-SiNW MOSFET at $V_{ds}=0V$ and $V_{gs}=0V$

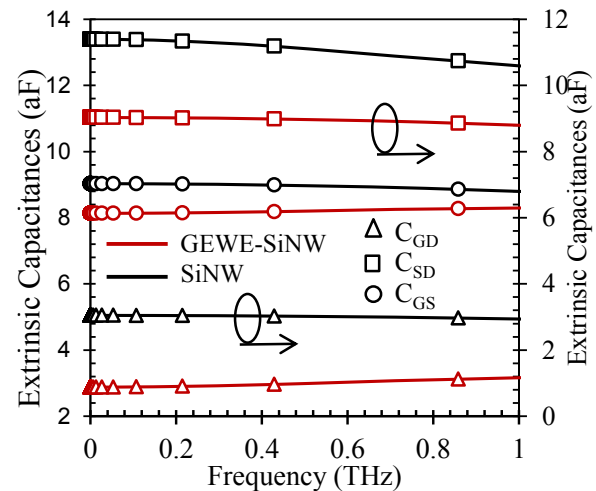


Fig. 3(c): Extrinsic Capacitance as a function of frequency for Conventional SiNW and GEWE-SiNW MOSFET at $V_{ds}=0V$ and $V_{gs}=0V$

Direct extraction procedures for drawing out the intrinsic small-signal parameters were performed. Fig. 4(a-b) shows the bias dependence of the small-signal parameters for GEWE-SiNW MOSFET and SiNW MOSFET in terms of gate to source, gate to drain and source to drain capacitances. The parasitic capacitances of GEWE-SiNW MOSFET turned out to be smaller than that of SiNW MOSFET, as shown in

Fig. 4(a). With the incorporation of GEWE scheme onto Conventional SiNW MOSFET, the parasitic capacitances decreases further with increase in gate bias voltage. This is due to improved screening of channel region from drain bias variations. Hence, lower values of intrinsic parasitic capacitances mean lower intrinsic delay which is suitable for switching applications such as in logic gates. Similarly, in GEWE-SiNW MOSFET capacitance decreases with change in drain bias in comparison to conventional SiNW MOSFET as shown in Fig. 4(b).

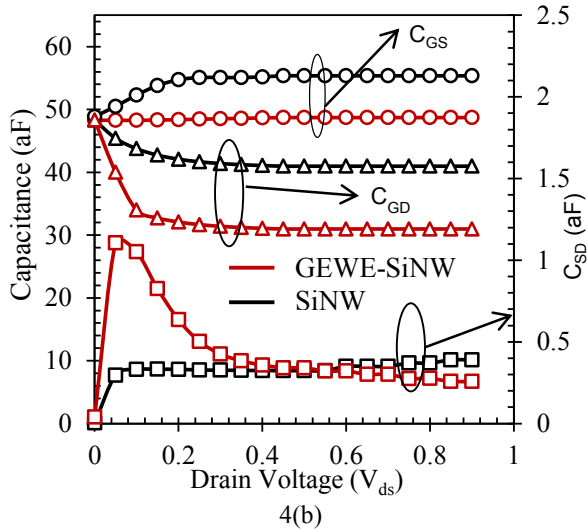
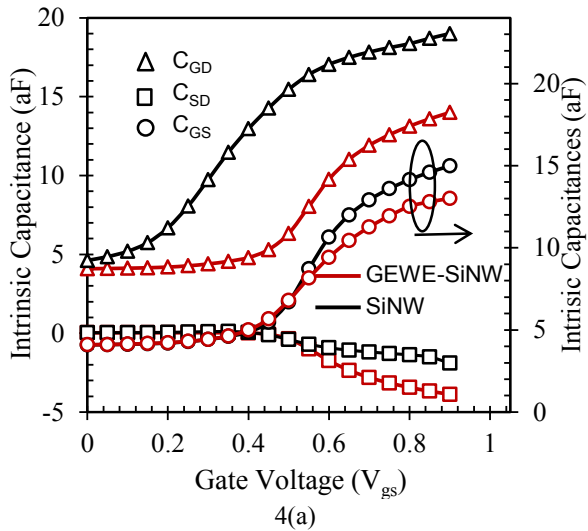


Fig.4: (a-b) Intrinsic Capacitance of Conventional SiNW and GEWE-SiNW MOSFET at different gate and drain voltages respectively.

Fig. 5(a-b) shows the intrinsic gate and drain transconductance of GEWE-SiNW and conventional SiNW MOSFET at gate and drain bias respectively. As is evident from Fig. 5(a), there is an appreciable increment in gate transconductance with increase in gate voltage in comparison to SiNW MOSFET. This is due to enhanced current driving capability of GEWE-SiNW MOSFET in contrast to conventional SiNW MOSFET [10], thus improves the gain of

the device. Further, drain transconductance also increases with increase in drain voltage which also results in enhancement in current driving capability of our device as shown in Fig. 5(b).

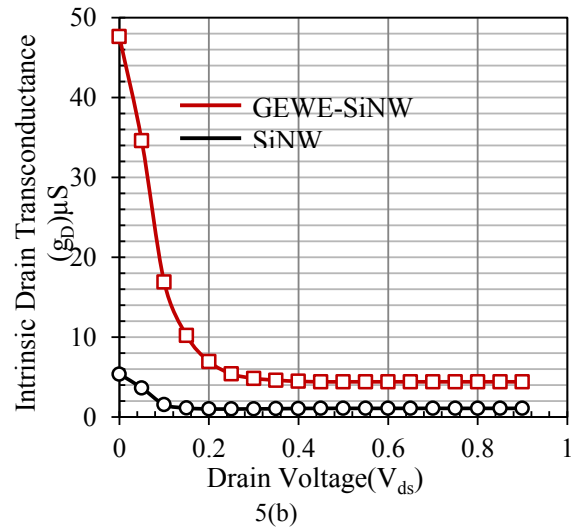
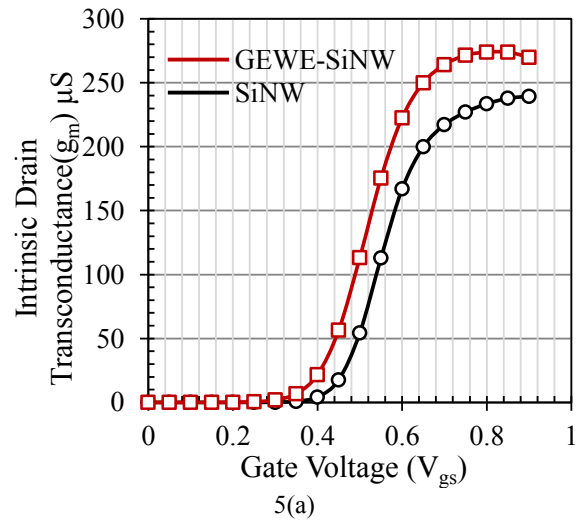


Fig.5: (a-b) Intrinsic gate and drain transconductance of Conventional SiNW and GEWE-SiNW MOSFET as a function bias voltage.

Table I: Extracted Parameters of GEWE-SiNW MOSFET

Parameter	Value Extracted
C_{sd}	9aF
C_{gs}	8.14aF
C_{gd}	0.21aF
R_s	3.0k Ω
R_d	1.98k Ω
R_g	0.37k Ω
L_d	53.22pH
L_s	0.02pH

CONCLUSION

In this work, both extrinsic and intrinsic parameters of GEWE-SiNW MOSFET are directly extracted and compared with conventional SiNW MOSFET with an aim to analyse the effect of these parameters at very high frequency. Simulation results evidence the effectiveness of gate electrode workfunction engineering on small signal parameters of GEWE-SiNW MOSFET by reducing both intrinsic and parasitic parameters of device which hinders the performance of a device at RF frequency.

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