TCAD Analysis of Small Signal Parameters and RF Performance of Heterogeneous Gate Dielectric-Gate All Around Tunnel FET

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ABSTRACT

In this paper, the simulation study of the small signal parameters and RF performance of n-type heterogeneous gate dielectric gate all around tunnel FET (n-type-HD-GAA-TFET) is studied and is compared with n-GAA-TFET, in terms of parasitic capacitances, cut off frequency and maximum oscillation frequency. TFET has entirely different mechanism (different from MOSFET) of inversion layer formulation, so the effect of purposely applied hetero-gate dielectric (to enhance the ON current of TFET) is seen on parasitic capacitances. Cut off frequency is also studied for analyzing the switching speed of the device.

Keywords: band to band tunneling, hetero-gate dielectric, inversion layer, parasitic capaciatance, tunnel FET (TFET).

1 INTRODUCTION

Static and dynamic power dissipation of ICs are main hindrance in growing demands of smart phones and laptops, which require semiconductor devices with low standby power operation. As the conventional MOSFET has a thermodynamic limit of $60mVdec^{-1}$ at room temperature on subthreshold slope SS. So the device, which uses a new operation mechanism other than diffusion over a thermal barrier, came into existence. In this regard, TFET has emerged as a possible replacement candidate [1-2]. Due to its steeper subthreshold slope, lower OFF current, reduced power consumption, lower value of leakage current and negligible short channel effects, TFET have achieved a lot of attention in the recent years [3-5].

TFET uses band to band tunneling mechanism; the gate voltage controls the position of the energy bands, and thus controls the barrier width at the source channel junction (the tunneling junction). For N-type TFET, a positive gate bias lowers the energy band of the channel and for a gate voltage where the conduction band of the channel goes below the valence band of source, the tunneling of electrons from source to channel takes place which results in ON current. In the OFF state of TFET, the valence band of source is below the conduction band of channel, resulting in a large barrier width at the tunneling junction, which obstructs the tunneling of electrons and results into an OFF current of the order of approximately femto amperes [6-7].

Despite of its lower I_{OFF}, steeper SS and negligible short cannel effects, TFET suffers from very low ON state current which make it unsuitable for practical application. Many device architectures were proposed in order improve the ON current, such as band gap engineering (narrow bandgap materials III-V semiconductors), high-k dielectric materials, dual material gate, highly doped pocket geometry [8-9]. Another problem with TFET is its ambipolar conduction [10]. For lowering ambipolar current and simultaneously enhancing the I_{ON} hetero-gate dielectric (HD) TFET have been proposed [11]. In HD-TFET a high-K material located partially near the source side induces a local minimum of the conduction band at the source channel junction and hence reduces the tunneling barrier width and thus enhances the I_{ON} and the low-K dielectric present near the drain side suppresses the ambipolar current. Thus, in this work a HD-GAA-TFET with different high-k combinations and GAA-TFET with SiO_2 and HfO_2 as a gate dielectric are taken into consideration.

2 SIMULATION AND DEVICE DETAILS

All simulations have been performed using the ATLAS device simulator. The models activated during simulation are as follows: concentration and field dependent mobility model, Shockley-Read-Hall for carrier recombination, non-local band to band tunneling, band gap narrowing and Fermi Dirac statistics [12].

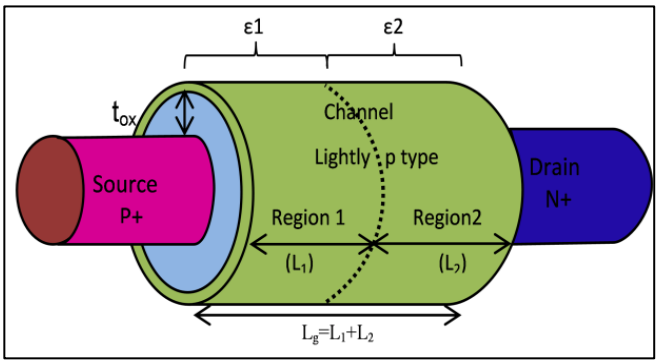

Fig 1: Heterogeneous dielectric Gate- Gate All Around-Tunnel MOSFET.

Fig. 1 shows the simulated structure of n-type HD-GAA-TFET. Table 1 shows Device Geometrical Parameters and the values used in the simulation.

Both the numerical methods Gummel (decoupled) together with Newton's (Fully coupled) has been incorporated to mathematically solve the carrier transport equation.

Parameter symbol	Technology parameter	Value
L	Channel Length	50nm
R	Channel radius	10nm
t_{ox}	Gate oxide thickness	3nm
N_s	Source doping (p^+)	$10^{20}cm^{-3}$
N_{ch}	Channel Doping lightly p type	$10^{17}cm^{-3}$
N_d	Drain doping (N^+)	$5\times10^{18}cm^{-3}$
Φ_m	Metal work function	4.5eV
L_1	Length of region 1	20nm
L_2	Length of region 2	30nm

Table 1: Device Geometrical Parameters and the values used in the Simulation.

All the simulation cases have different dielectric as shown in table 2. Case 1 and 2 is for GAA-TFET with different dielectric (SiO_2 and HfO_2). Case 3, 4 and 5 are of n-HD-GAA-TFET.

	Region 1	Region 2
	Dielectric Constant	
Case 1	3.9	3.9
Case 2	21	21
Case 3	7.5	3.9
Case 4	21	3.9
Case 5	29	3.9

Table: 2 All the Simulation cases.

3 RESULTS AND DISCUSSION

The dynamic performance influencing factors parasitic capacitances are studied for all the simulation cases shown in table 2. The partitioned of total gate capacitance C_{gg} in a TFET is entirely different from that of a MOSFET. This difference is mainly attributed to the difference in the inversion charge distribution. For a MOSFET, both source and drain regions are connected to the inversion layer (operating in linear region) and thus total gate capacitance is symmetrically apportioned between source and drain or (C_{gs} ~ C_{gd} ~ $C_{gg}/2$). But in case of TFET, only C_{gd} contributes a larger fraction of C_{gg} as compared to C_{gs}. For a constant drain bias, at the lower gate bias the inversion charge layer is formed near the drain end, with increase in gate bias the inversion layer extends towards the source side (unlike as in the case of MOSFET) [13].

All the capacitances are extracted by using small signal ac simulations at a constant frequency of 1MHz. The

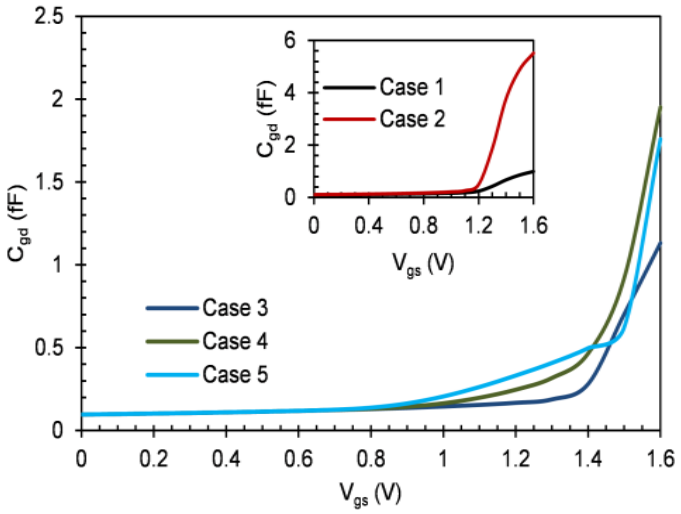

Fig. 2 Gate to drain capacitance as a function of gate bias for all the cases.

miller capacitance C_{gd} as a function of gate bias at a constant drain bias is shown in Fig. 2. As the gate bias is increased the inversion charges present underneath the gate dielectric increases resulting in enhanced gate drain capacitance. The miller capacitance accounts for the response time of the device. There is a reduction of approximately 1.2 times in miller capacitance with the implementation of hetero gate dielectric. Thus results in the reduction of the response time of the device.

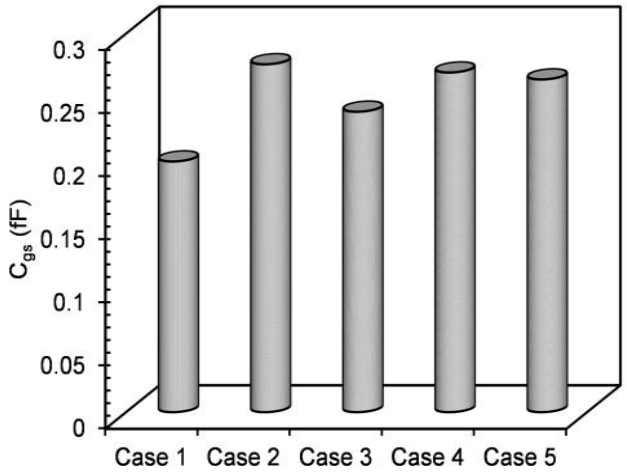

Fig. 3 Gate to source capacitance at V_{gs}=1.2 V and V_{ds}= 1.0V for all cases.

The gate to source capacitance C_{gs} is shown in Fig. 3 at V_{gs}=1.2 V and V_{ds}=1.0 V. As the inversion charges moves from drain to source side which results in lower value of gate to source capacitance as compared to gate to drain capacitance, or total gate capacitance is mainly contributed by C_{gd}. As evident from Fig. 2 and Fig. 3, the order of C_{gs} is very much lower than that of C_{gd}.

Fig. 4 shows the parasitic gate capacitance (total gate capacitance) C_{gg} with respect to gate voltage. Total gate capacitance interrelates to the active power dissipation ($C_{gg}V_{dd}^2f$). It is clear from the fig. 4 that C_{gg} is almost of the same order as that of C_{gd} which clearly shows that total gate capacitance is mainly contributed by gate drain capacitance. As evident from the figure that with the implementation of hetero-gate dielectric the C_{gg} has reduced drastically, which helps in reduction of active power dissipation [14-15].

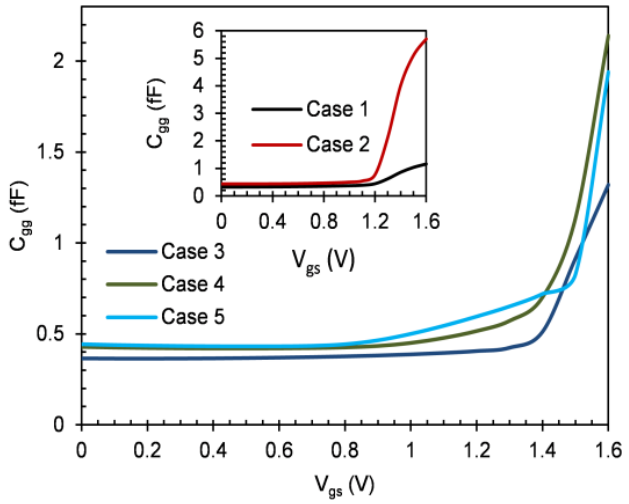

Fig. 4 Gate capacitance as a function of gate voltage for all the cases.

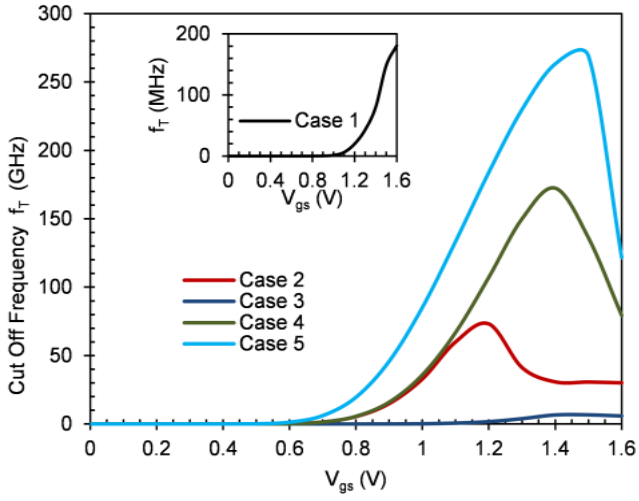

Fig.5 Cut off frequency as a function of gate voltage for all the cases.

Furthermore the Radio frequency figure of merit (RF-FOM) such as cut off frequency and maximum oscillation frequency of the device has been studied for all the cases. Fig. 5 shows the cut off frequency of the device with respect to gate bias variation. The cut off frequency f_T of the device is the frequency at which the short circuit current gain of the device falls to unity. The switching speed of the device depends on the cut off frequency. As clearly shown, the cut off frequency is enhanced by an order of 1.5 KHz in case 5 as compared to case 1 or with the application of Hetero dielectric the cut off frequency is enhanced tremendously, which results in higher switching speed of the device.

F_{max} is the highest frequency at which the power gain is unity. Fig. 6 shows the maximum oscillation frequency is enhanced to an order of 10^{10}Hz from 10^7Hz with the application of hetero gate dielectric [16, 17].

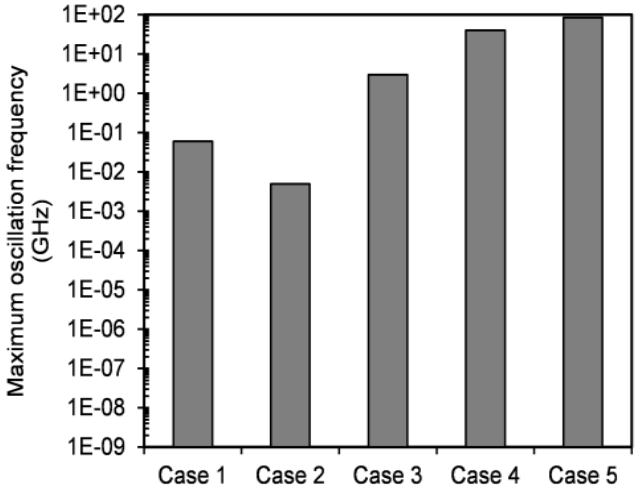

Fig. 6 Maximum oscillation frequency for all the cases.

4 CONCLUSION

In this work, the small signal parameters and RF performance of HD-GAA-TFET has been studied using TCAD device simulations. To study the impact of HD, various combinations of high-k has been studied. With the implementation of HD superior benefits of TFET are obtained. The parasitic capacitances are decreased and the cutoff frequency and the maximum oscillation frequency is manifold increased (better RF performance), which results in increase in switching speed. So the HD TFET can find applications in high-switching-speed electronics.

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