Impact of High-*k* gate oxide on Intrinsic Device Performance of Junctionless Transistor

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ABSTRACT

In this paper, comparative analysis of intrinsic device performance parameters of bulk planar junctionless transistor (BPJLT) with different gate oxide material has been carried out by using two dimensional Cogenda Visual TCAD simulator. The process parameters considered in the analysis are physical gate length (L_G) and gate oxide materials namely SiO_2, Si_3N_4, and HfO_2. It has been found that, high-*k* gate oxide material shows better impact on electrical parameters like on-state drive current (I_{ON}), sub-threshold slope (SS) and drain induced barrier lowering (DIBL) of the device. In addition to this, analog performance parameters like transconductance (g_m) and transconductance generation factor (g_m/I_D) have also been analyzed. It has been observed that, use of high-*k* material helps to reduce gate leakage of the device and scale gate oxide thickness for better channel control.

***Keywords**:* junctionless transistor, high-k material, short channel effects

1 INTRODUCTION

Over the last decade, size of complementary-metal-oxide-semiconductor (CMOS) devices has reduced exponentially due to scaling, which has helped to increase operating speed of circuit and improve the number of transistors on chip making it more compact and ultimately reducing the manufacturing cost. Scaling of metal oxide semiconductor field effect transistor (MOSFET) requires shallow doping at source and drain region. This process has become more complicated when scaling reached to sub 40 nm node, degrading the performance of device [1]. To overcome these drawbacks recently, a novel source-channel and drain-channel junction free transistor structure, called junctionless transistor (JLT), has been proposed and fabricated successfully [2]. JLT has uniform doping concentration over source-channel-drain region. It has many advantages over conventional MOSFETs such as high scalability, simple process flow, low thermal budget, improved performance against short channel effects [2-4]. Operating principle of JLT is different from conventional MOSFET, here conduction takes place at the center of channel. Drain current (I_D) depends on channel doping concentration and the workfunction difference between channel material and gate material keeps the devices in off state [2-6].

Various structures of JLT have been proposed by many reserchers [2-5]. It has been shown that bulk planar JLT (BPJLT) has better electrical properties over other JLT. Further, compatibility in the fabrication process of BPJLT and current CMOS technology [5] is an added advantage. Inspite of these advantages, it has been observed that as physical gate length of JLT reduces to 20 nm node BPJLT suffers from leakage current and short channel effects namely drain induce barrier lowering (DIBL), subthreshold swing (SS). To resolve this problem, high-*k* gate oxide is utilized [8-9]. The goal of this paper is to investigate the performance of BPJLT by using high-*k* material as the gate oxide with the help of two dimensional TCAD simulator tool. The impact of high-*k* gate oxide material shows reduction in DIBL, SS and off stage leakage whereas it improves I_{ON}.

The organization of rest of the paper is as follows, in Section 2 device architecture has been described with simulation setup and parameters used in simulation process, Section 3 discusses about performance of device and results in detail, followed by conclusion in Section 4.

2 DEVICE STRUCTURES AND SIMULATION SETUP

Fig. 1 shows the structure of BPJLT used in simulation. As shown in the figure, the structure has uniform doping along the channel and there is no junction present in the

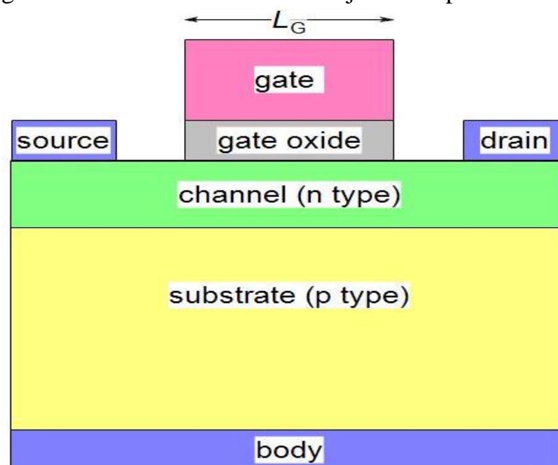

Fig. 1: Structure of BPJLT used in simulation

source-channel and drain-channel region. However, to separate out channel region it has a p-n junction in vertical direction which also helps to deplete the channel from substrate side and make device off successfully [5, 7]. The doping concentration of channel should be high to achieve sufficient I_{ON}. Further it helps to reduce the drain to source series resistance. Doping concentration along substrate is of p type, gate material is of P-poly silicon type, whereas gate oxide thickness of 1nm and gate length varies from 10-30nm.

Here different high-*k* gate oxide materials namely SiO_2, Si_3N_4, and HfO_2 have been used. Further, incorporating high-*k* material reduces threshold voltage (V_T) of device. For the comparison, among various gate oxide materials, V_T of devices has been adjusted at 0.25 V by varying the gate workfunction. Drain-source voltage (V_{DS}) is set at 50 mV and gate-source voltage (V_{GS}) varies from –0.5V to +1V. For simulation purpose Cogenda VTCAD simulator version-1.8.2 [13] has been used with drift diffusion model.

Parameters	Value
Physical gate length (L_G)	Variable
Channel thickness	10nm
Channel doping density	1.5×10^{19} cm^{-3}
Gate oxide Thickness	1nm
Substrate doping density	5×10^{18} cm^{-3}

Table 1: Device parameters used for simulation.

3 RESULTS AND DISCUSSION

For better performance of any transistor, I_{ON} must be high whereas I_{OFF} must remain under control. It has been observed that incorporating high-*k* material as gate oxide, reduces V_T. In addition to this, high-*k* material improves the gate coupling and the device has better I_{ON} and electrical properties[8, 9]. Fig. 2 shows a graph of drain current (I_D) and V_{GS} for n channel BPJLT with various gate oxide materials. Graphs have been plotted at V_{DS}=50mV and L_G=10 nm. For high-*k* gate materials, I_{ON} improves by ~56.44 % whereas I_{OFF} reduces significantly. This is because of better gate coupling and reduction in tunneling current through gate oxide. Fig. 3 shows graph of output characteristics and V_{DS} for n channel BPJLT at V_{GS}=1V. Incorporating high-*k* as gate oxide BPJLT offers more drain current at same V_{DS}.

3.1 Short Channel Effects

DIBL and SS are the important SCE for any transistor used in digital circuits. DIBL should be as minimum as possible. Theoretically SS of the MOSFET limited to 60 mV/dec [1]. Due to narrow channel width, JLT offers low DIBL. Fig. 4 - 6 shows the variation in DIBL, SS and I_{ON}/I_{OFF} ratio as a function of L_G for SiO_2, Si_3N_4 and HfO_2 respectivly. It can be clearly observed from the graph that DIBL and SS in the case of HfO_2 have minimum value amongst all others dielectric materials, whereas I_{ON}/I_{OFF} ratio is larger. The impact of incorporating high-*k* material as a gate oxide on short channel performance of BPJLT is significant when the gate length is below 20 nm. From Fig. 4, DIBL measured for different gate oxide material at L_G=10 nm are as follows: SiO_2 ~190 mV/V, Si_3N_4 ~125 mV/V and HfO_2 ~95 mV/V. Further, it has been observed that for L_G = 20 nm and above variation in DIBL of transistor have not more than ~20 mV/V. Hence the imapct of HfO_2 is significant for short L_G. DIBL of the JLT has been calculated by the following formula [11].

$$\mathrm{DIBL(mV/V)} = \frac{V_{TLin} - V_{TSat}}{0.95} \quad (1)$$

where,

V_{TLin}= linear threshold voltage at V_{DS} = 50 mV

V_{TSat}= saturation threshold voltage at V_{DS} = 1V.

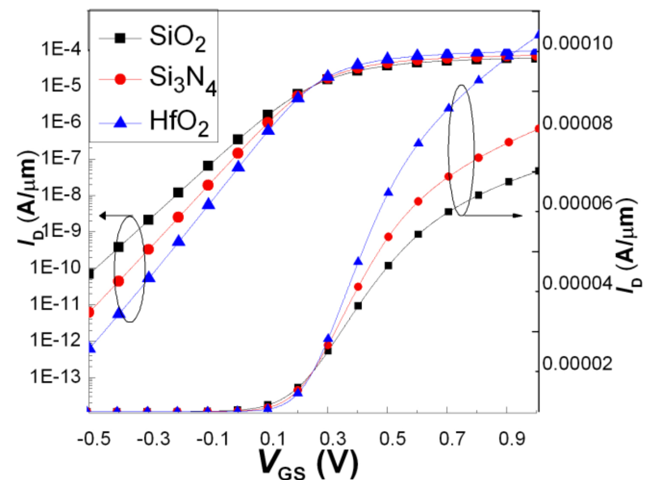

Fig. 2: I_D versus V_{GS} characteristics of BPJLT for SiO_2, Si_3N_4 and HfO_2 at V_{DS} = 50 mV and L_G = 10 nm.

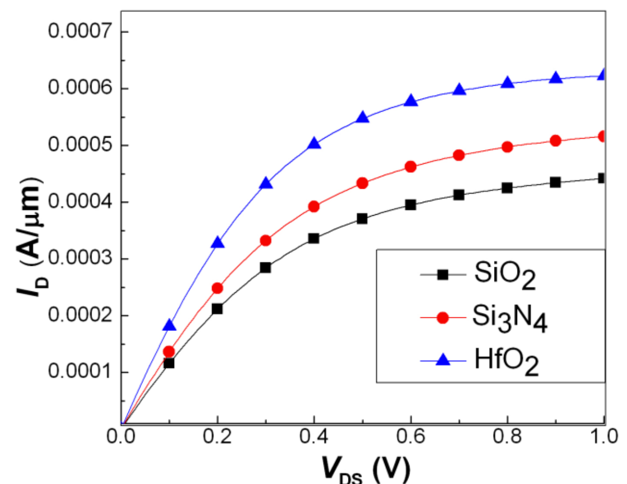

Fig. 3: Variation of I_D for SiO_2, Si_3N_4 and HfO_2 at V_{GS} = 1V and L_G = 10 nm.

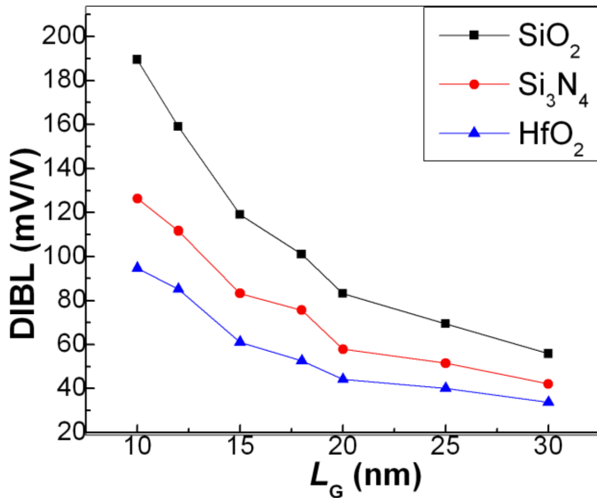

Fig. 4: Variation of DIBL with L_G for SiO_2, Si_3N_4 and HfO_2 as gate oxide material in BPJLT.

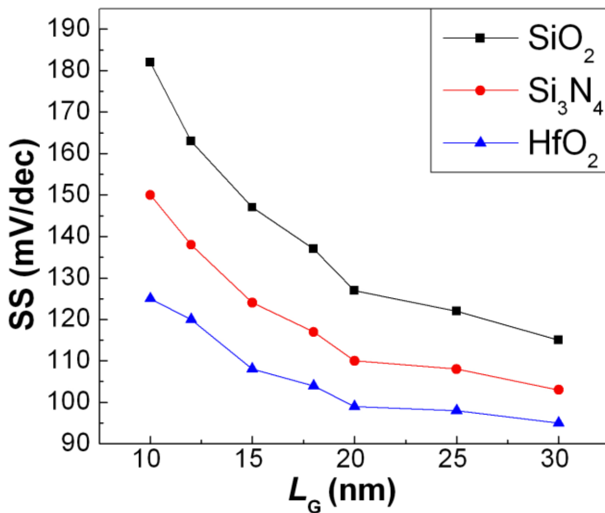

Fig. 5: Variation of SS with L_G for SiO_2, Si_3N_4 and HfO_2 as gate oxide material in BPJLT.

Fig. 5 shows the impact of high-*k* gate oxide on the I_{ON}/I_{OFF} ratio of BPJLT for variable L_G. The value of I_{ON} is extracted when V_{GS} = 1V and V_{DS} = 1V. Similarly I_{OFF} is calculated when V_{GS} = 0V and V_{DS} = 1V. Thus, use of high-*k* gate oxide makes the device a promising candidate for low power digital circuits under 20 nm node.

3.2 Analog Performance

The important analog performance parameters are g_m and g_m/I_D [11] Fig. 7 - 8 shows the variations of g_m and g_m/I_D with V_{GS} for SiO_2, Si_3N_4 and HfO_2 at V_{GS} =1V and L_G =10 nm. At high-*k* gate oxide, g_m of BPJLT demonstrates a higher value. This is because of the maximum I_{ON} provided. The g_m of the device has been calculated as $\delta I_D/\delta V_{GS}$. Unlike conventional MOSFET, BPJLT has maximum g_m/I_D in weak inversion and it reduces in the strong inversion

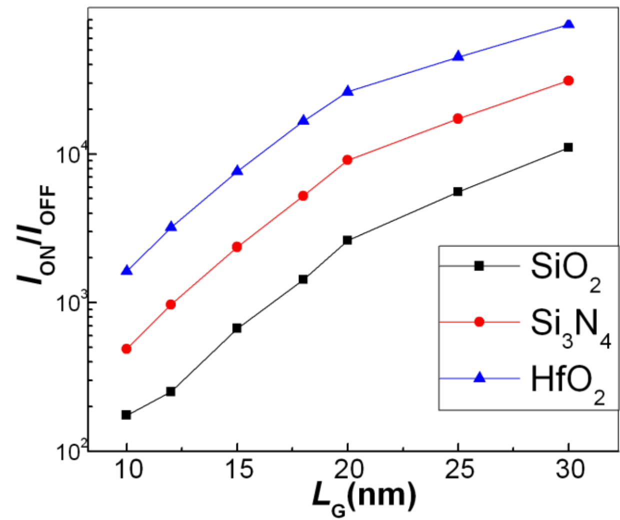

Fig. 6: I_{ON}/I_{OFF} ratio of BPJLT with L_G for SiO_2, Si_3N_4 and HfO_2 as gate oxide material.

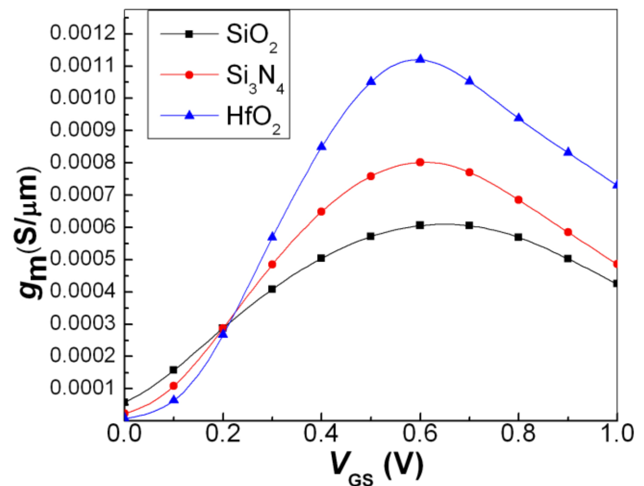

Fig. 7: Variation of g_m with V_{GS} at V_{DS}=1V and L_G = 10 nm for SiO_2, Si_3N_4 and HfO_2 as a gate oxide material in BPJLT

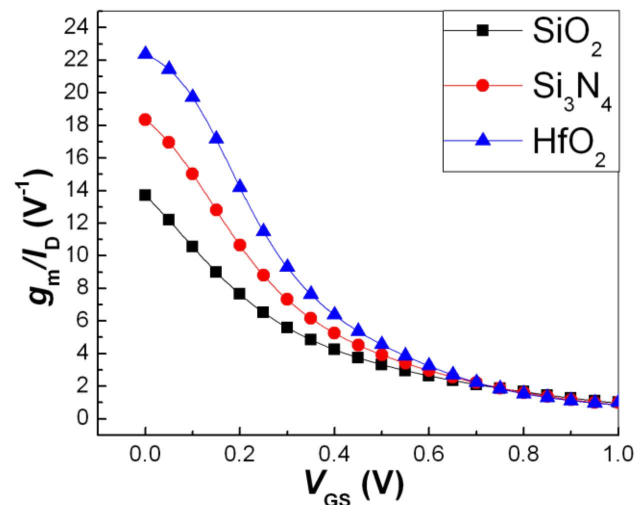

Fig. 8: Variation of g_m/I_D with V_{GS} at V_{DS}=1V and L_G = 10 nm for SiO_2, Si_3N_4 and HfO_2 as a gate oxide material in BPJLT.

regime with increasing I_D [12]. Fig. 8 shows g_m/I_D with different V_{GS}. It is observed that g_m/I_D is maximum for HfO_2 and minimum for SiO_2. Thus, by incorparating high-k gate oxide material, the analog performance of BPJLT improves and the device is suitable for low power analog applications.

4 CONCLUSION

Transfer and output characteristics of BPJLT shows that when HfO_2 is used as gate oxide material, I_{ON} of the device improves by ~56.44 % while I_{OFF} reduces significantly. This is mainly due to strong gate coupling and reduction in tunneling current through gate dielectric material. In addition to this, use of high-k material improves SCE like DIBL, SS and I_{ON}/I_{OFF} ratio at shorter gate length. Furthermore, high-k gate oxide in BPJLT improves the analog performance parameters like g_m and g_m/I_D. Thus, from simulation result it is observed that incorporating HfO_2 gate oxide in BPJLT make promising candidates for low power digital applications.

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