Impact of Gate Oxide Thickness and Channel Thickness on DC Performance of Carbon Nanotube Tunnel FET

Kalyani S. Bhosale, Sayali R. Aher, Harshad S. Borse, Ashish V. Jawake,
Subhash R. Patil and Ganesh C. Patil*

*Department of Electronics and Telecommunication Engineering
JSPMs Rajarshi Shahu College of Engineering
Savitribai Phule Pune University, Pune, India.
Email: ksb9790@gmail.com, pganesh@rscoe.org

ABSTRACT

Carbon nanotube is being considered as one of the promising alternative material to the conventional silicon technology due to its exceptional material properties. In this work the impact of variations in gate oxide thickness ($t_{\rm ox}$), physical gate length ($L_{\rm G}$), CNT diameter and energy gap of a double gate p-i-n carbon nanotube Tunnel FET has been studied on the DC performance parameters namely ON-state current ($I_{\rm ON}$), OFF-state current ($I_{\rm OFF}$) and the static power dissipation ($P_{\rm stat}$). A coupled mode space approach has been used to solve Schrödinger equations with open boundary by means of the non-equilibrium Green's function (NEGF) formalism. A 3D Poisson solver NANOTCAD *ViDES* has been used for simulations.

Keywords: carbon nanotube, tunnel FET, gate oxide thickness, channel thickness, DC performance

1 INTRODUCTION

In the last few decades, due to scaling of MOSFET, smaller and faster transistors have attracted the attention of various research groups [1]. However, the scaling down of conventional complementary-metal-oxide-semiconductor (CMOS) technology is suffering from fundamental limitations mainly scaling of the physical device parameters, supply voltage, increase in the leakage current etc.

To overcome these problems, novel engineering solutions such as improving the device architecture, introducing new materials into the channel region with superior transport properties (SiGe, Ge, etc.), and new gate dielectrics (high-κ) have been suggested [2]-[7]. Tunnel FET (TFET) is one such prominent device which has surpassed CMOS at low voltages [8]. This is mainly because of the current mechanism in TFET *viz* band-to-band-tunneling (BTBT), first observed by Zener [9], where the charge carriers transfer from one energy band into another at a heavily doped pn junction [10]. The interband tunneling in TFET can be switched ON and OFF at once by controlling the band bending near the source-channel junction via gate biasing.

Due to limitations in silicon technology and for enhanced device performance, researchers explored various new carbon material based devices [11]-[15]. Amongst them carbon nanotubes (CNT) have demonstrated the largest on-state drive current ($I_{\rm ON}$) in terms of scaling [8] and are considered as a promising alternative material to the conventional silicon technology by ITRS [1]. CNTs have a direct bandgap [16] thus making BTBT possible in ballistic transport mode.

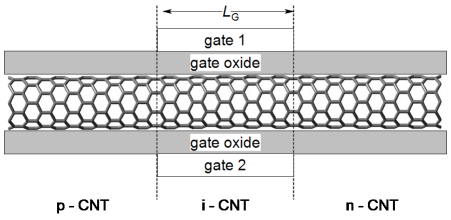

Figure 1: Device structure for double gate p-i-n CNT TFET used in simulations.

In this work a double gate p-i-n carbon nanotube tunnel field effect transistor (DGCNT TFET) has been simulated and a coupled mode space approach has been used [17] to solve Schrödinger equations with open boundary by means of the non-equilibrium Green's function (NEGF) formalism. A 3D Poisson solver NANOTCAD *ViDES* [18] has been used in order to study the impact of variations in gate oxide thickness ($t_{\rm ox}$), physical gate length ($L_{\rm G}$), CNT diameter and energy gap of the DGCNT TFET on ON-state current ($I_{\rm ON}$), OFF-state current ($I_{\rm OFF}$) and the static power dissipation ($P_{\rm stat}$) of the device. A p_z-orbit atomistic nearest tight-binding method has been used to model the band structure of the CNT channel with a hopping parameter of 2.7eV. The simulation has been carried out at a temperature of 300K.

The organization of rest of the paper is as follows, Section 2 presents the device structure and the simulation methodology used in this work. Section 3 analyzes the DC performance of the simulated device. Finally the conclusion is given in Section 4.

Parameter	Unit	Value
L_G	nm	variable 2 to 5
Gate oxide thickness (t_{ox})	nm	variable 2 to 5
Molar fraction used for Source/Drain doping	–	5×10^{-3}

Table 1: Device Parameters

2 DEVICE STRUCTURE AND SIMULATION SETUP

The device structure and the device parameters used in the simulation are shown in Figure 1 and Table 1 respectively.

A (13,0) CNT has been considered for simulation purpose whose channel length L_G is varied from 2 nm to 5 nm, by keeping constant source/drain extension length of 5 nm for different gate oxide thicknesses. Silicon dioxide has been used as the gate dielectric material. Four types of zigzag CNTs namely - (11,0) CNT, (13,0) CNT, (17,0) CNT and (19,0) CNT have been simulated to observe the variation of I_{ON} and I_{OFF} with respect to energy gap and diameter of the CNT. The I_{OFF} is defined as the current obtained when $V_{GS} = 0$ V and $V_{DS} = 0.3$ V whereas I_{ON} is defined as the current obtained when $V_{GS} = 1$ V and $V_{DS} = 0.3$ V.

3 RESULTS AND DISCUSSION

Figure 2-3 shows the variation of I_{ON} and I_{OFF} of DGCNT TFET as a function of L_G for different oxide thicknesses.

From Figure 2 it can be seen that, since reduction in L_G causes lowering of the channel barrier [19], the I_{ON}

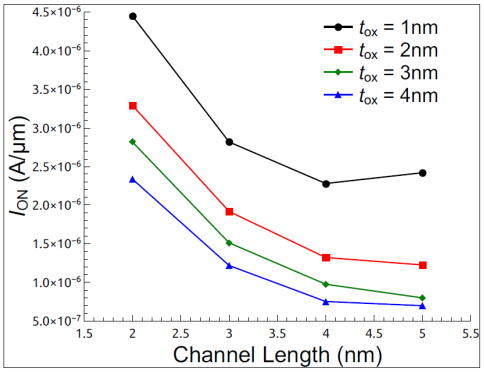

Figure 2: Variation of I_{ON} with L_G of (13,0)CNT DGCNT TFET for different t_{ox} at $V_{DS} = 0.3$ V and $V_{GS} = 1$ V.

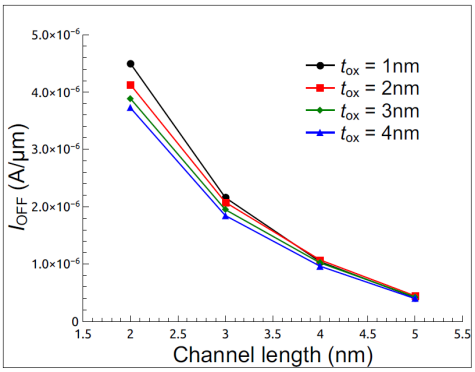

Figure 3: Variation of I_{OFF} with L_G of (13,0)CNT DGCNT TFET for different t_{ox} at $V_{DS} = 0.3$ V and $V_{GS} = 1$ V.

of the device improves. Further, from Figure 3 it can be seen that, at lower L_G values because of the direct tunneling from source to drain, I_{OFF} of the device increases. In addition it is observed that, as t_{ox} is increased, I_{ON} and I_{OFF} for a particular value of L_G decreases.

For $L_G = 3$ nm, when V_{GS} was swept from 0 V to 1 V and $V_{DS} = 0.3$ V, the value obtained for I_{ON} was 2.8185×10^{-6} for t_{ox} of 1 nm. This current was reduced to 1.21997×10^{-6} for t_{ox} of 4 nm. Thus, I_{ON} has been reduced by almost 56% for the variation of t_{ox}. Similarly, for the same L_G and voltage values, we observed 14.5% reduction in I_{OFF} when t_{ox} was varied from 1 nm to 4 nm.

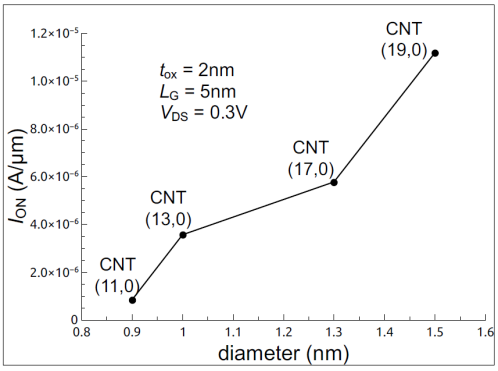

Figure 4: I_{ON} as a function of CNT diameter for $L_G = 5$ nm DGCNT TFET. $t_{ox} = 2$ nm, $V_{DS} = 0.3$ V and $V_{GS} = 1$ V.

The diameter of the CNT depends on the chiral vectors *(n,m)* of the CNT. With increase in the chiralty of the CNT the diameter also increases which in turn affects the conductance of the nanotube, it's density, lattice structure, and other properties. Thus, the conductivity of CNT is a function of their chirality, the degree of twist as well as their diameter.

From Figure 4 it can be seen that, increasing CNT diameter improves I_{ON} of the DGCNT TFET. The main reason for the improvement in I_{ON} of the device is that, since quantized states for each atom ring are closer in energy, the electron transport enhances by increasing the diameter of the CNT [19]. Therefore, because of increase in electron transport I_{ON} of the DGCNT TFET improves.

Figure 5 shows variation of the I_{OFF} with the diameter of the CNT. For higher CNT diameter values, as compared to lower CNT diameter values, the valence band edge of channel is closer to the conduction band edge of the source at the same gate field [20]. This causes tunneling between the source and the channel giving rise to the leakage current. Thus, CNTs with a larger diameter demonstrate a higher I_{OFF}.

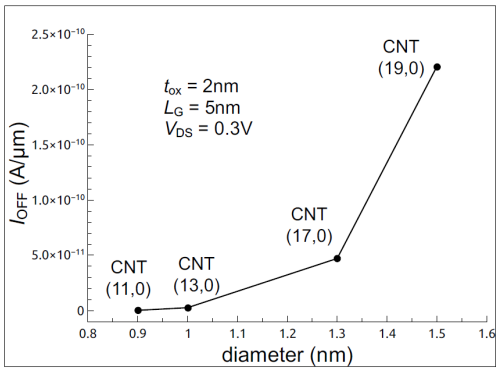

Figure 5: I_{OFF} as a function of CNT diameter for L_G = 5 nm DGCNT TFET. t_{ox} = 2 nm, V_{DS} = 0.3 V and V_{GS} = 1 V.

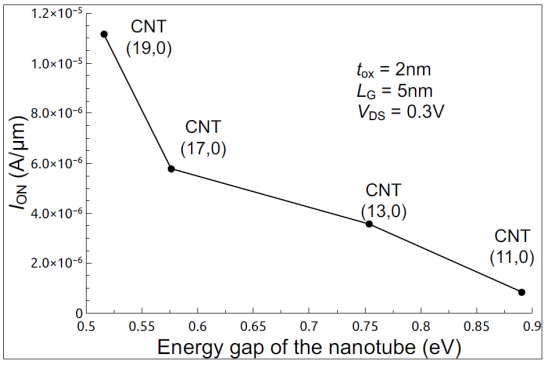

Figure 6: I_{ON} as a function of energy gap of CNT for L_G = 5 nm DG-CNT-TFET. t_{ox} = 2 nm, V_{DS} = 0.3 V and V_{GS} = 1 V.

From Figure 6-7 it can be seen that, increasing the energy gap of CNT, I_{ON} and I_{OFF} of DGCNT TFET reduces. Since the band gap varies inversely with the

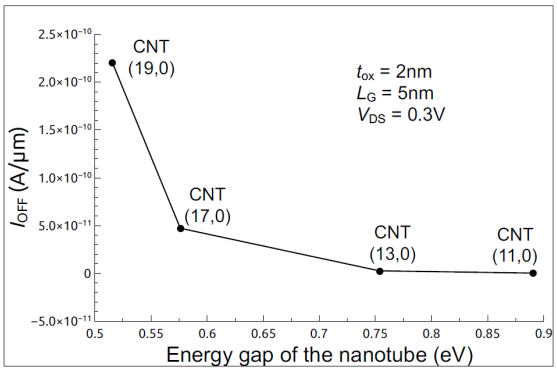

Figure 7: I_{OFF} as a function of energy gap of CNT for L_G = 5 nm DG-CNT-TFET. t_{ox} = 2 nm, V_{DS}= 0.3 V and V_{GS} = 1 V.

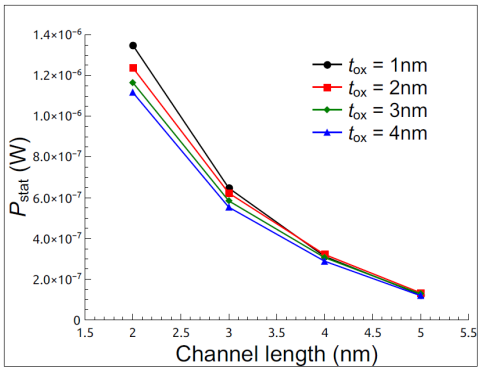

Figure 8: Variation of P_{stat} with L_G of (13,0)CNT DGCNT TFET for different t_{ox} at V_{DS} = 0.3 V and V_{GS} = 1 V.

diameter of the tube, as the energy gap of the CNT increases we observe decrease in the I_{ON} and I_{OFF}.

Figure 8 shows the variation of the static power dissipation (P_{stat}) with respect to L_G. It can be seen that, P_{stat} decreases with increase in L_G. This is mainly because of the reduction in I_{OFF}. For L_G = 3 nm, when V_{GS} was swept from 0 V to 1 V and V_{DS} = 0.3 V, P_{stat} decreased by 14.5% showing an improvement in the device performance when t_{ox} was varied from 1 nm to 4 nm.

4 CONCLUSION

In this paper, the effect of varying t_{ox}, L_G, CNT diameter and energy gap of the p-i-n DGCNT TFET on the DC performance parameters namely I_{ON}, I_{OFF} and P_{stat} have been studied. It has been observed that, the drain current varies inversely with t_{ox}, L_G and the energy gap of the p-i-n DGCNT TFET. In addition to this, the drain current is directly proportional to the diameter of the p-i-n DGCNT TFET. Thus, at low operating

voltages, strong quantum effects like BTBT is possible in CNTs making them one of the strong contender in the race of novel devices for digital applications.

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