Advanced Packaging for Next Generation Imaging and Sensor Devices

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ABSTRACT

Quilt Packaging® (QP) is a unique and versatile edge-interconnect technology that utilizes "nodule" structures that extend out from the vertical facet along the edges of chips to allow for interchip mechanical alignment and communication. QP has demonstrated world-record chip-to-chip interconnect performance, reduces system size, weight, and power (SWaP) requirements, and enables entirely new system designs. Quilt Packaging has been demonstrated in Si, GaAs, InP, GaSb, and more. The QP interconnect structures or "nodules" can be customized to enable precision alignment, dense I/O pitch (less than 10 um), and extremely wide bandwidth. They can also be implemented to enable 3D and curved multichip assemblies. When utilized for electrical I/O, QP nodules perform as if they were on-chip interconnects even though they run off-chip, having demonstrated less than 1 dB of insertion loss across the entire bandwidth from 50 MHz to 220 GHz.

Keywords: MMIC packaging; sensor array; imaging array; interconnects; system-in-package; Quilt Packaging

1 INTRODUCTION

Planar and/or non-planar multi-chip sensing and imaging arrays can benefit from decreased system and packaging complexity, reduced manufacturing costs and better performance. Issues such as design complexity, size weight and power (SWaP), and manufacturability can negatively affect both system cost and performance. Primary among the cost drivers in producing large format arrays is wafer yield at the IC level. As the area or "footprint" of an array increases, the likelihood that it will be free of defects decreases. Defects can leave the array inoperable, or at best, poorly performing. Efforts to combine smaller, higher-yielding (and thus lower-cost) chips into large arrays has had limited success. Issues such as chip-to-chip gap size and alignment accuracy at the sensor chip packaging and interconnect level introduce problems with missing pixel clusters or rows in the combined array.

In addition, existing chip-level packaging and interconnect approaches such as wirebonding, ribbon bonding, and flip-chip are becoming less-viable options for high-frequency, high-bandwidth applications. For wire and ribbon bonding, system speeds are limited due to effective impedances created by the wires or ribbons themselves at high frequencies. These impedances cause the wire or ribbon to behave as a filter as well, thus limiting the available bandwidth of the interconnection. Typical insertion loss metrics for wirebonds at 40 GHz are in the 2 dB range [1] per bond transition, and even though flip-chip offers an improvement, bumps still contribute significant insertion loss (0.68 dB per bump) at 40 GHz [2]. These approaches have been extended to higher frequencies [3-5]. To decrease insertion loss in the millimeter-wave range, matching or tuning networks are often used. While often succeeding at decreasing losses, these networks add additional complexity, SWaP and cost to the system as well restricting it to a narrow operational frequency band, limiting its usefulness in a variety of sensor array applications.

Quilt Packaging (QP) is an innovative chip-to-chip packaging interconnect technology that resolves or mitigates these longstanding issues. In this paper we present an overview of Quilt Packaging, explore the fabrication and assembly of QP structures and chips, discuss various large format array and high bandwidth applications for QP, as well as the thermal, mechanical, and process reliability of QP.

2 QUILT PACKAGING OVERVIEW

Quilt Packaging is a unique and versatile edge-interconnect technology [6-11] that utilizes "nodule" structures that extend out from the vertical facet along the edges of chips to allow for inter-chip alignment and communication (Fig. 1). QP has demonstrated world-record chip-to-chip interconnect performance, and enables entirely new system designs [7,8,10]. Quilt Packaging has tremendous heterogeneous integration capability, with multi-chip quilts of disparate materials and process technologies possible, including but not limited to materials such as Si, GaAs, InP, SiGe, GaN, SiC, and fused silica, illustrating its process flexibility. The QP interconnect structures, or "nodules," can be customized to enable precision alignment, dense I/O pitch, extremely low-loss microwave transmission [12,13], and high-power current-handling capability. They can also be implemented to enable 3D and curved multichip assemblies.

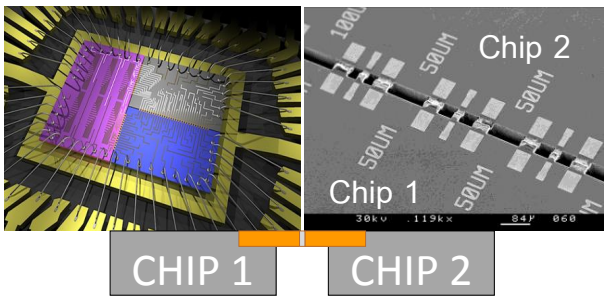

Figure 1. Graphic concept of Quilt Packaging (top left); SEM micrograph of QP interconnection nodule (top right); Cross-sectional concept image of QP interconnection (bottom).

QP has demonstrated ultra-wide bandwidth performance with chip-to-chip insertion loss of less than 1 dB from 50 MHz up to 220 GHz [13]. QP also offers a potentially much higher interconnect density along the die edges, capable of I/O pitches on the chip edge of less than 10 um with sub-micron chip-to-chip alignment. The original focus of QP technology was on Si; recent works has expanded into III-Vs and other compound semiconductor materials. Indiana Integrated Circuits, LLC, multiple government agencies and prime contractors, and the University of Notre Dame have been advancing the technology readiness level of QP for multiple applications, and have demonstrated a path to scale-up with RTI International's Electronics and Applied Physics Division for medium-volume production.

3 FABRICATION AND ASSEMBLY

Quilt Packaging technology has been in development for silicon-based applications for several years, including large-format array integration and microwave applications. Recent work has also seen processes developed for QP on GaAs, InP and GaSb substrates. QP can also be implemented in SiC, GaN and more.

3.1 Chip Fabrication.

Fabrication of QP interconnects on Si-based and III-V-based material substrates are briefly discussed in this section. To fabricate chips with QP nodules, conventional photolithography is used to define the nodule features, which are then etched to a depth of 25-35 microns into the wafer using Bosch deep reactive ion etching (for Si) or a chlorine-based inductively coupled plasma etching (for III-V materials). After the nodules shapes are defined, a seed layer, Ti/Cu is deposited and the nodules are filled using a Cu electroplating step. Electroplating overburden is removed with a chemical mechanical polishing (CMP) step. A top-level metal redistribution layer (RDL) is then patterned and deposited after the nodule process steps. Finally, the die on the wafer are singulated by a combination of deep etching and then backside grinding. The final separation and back grinding process can be adjusted for substrates of varying final thicknesses, depending on the material process and application. The typical QP fabrication is shown in Fig. 2.

Unlike Si DRIE, bulk micromachining of III-V is a much less mature process. A combination of process gas flow, RF power, etch mask material/thickness, temperature, wafer thickness and feature geometry impact the ability to fabricate MEMs-like features in III-V materials such as GaAs and InP with submicron precision. Promising results have been achieved in the fabrication of QP chips in GaAs and InP.

3.2 Quilt Assembly

Once die are singulated, and individual Quilt Packaging chips are available, a cleaning step based on acetone, N-methyl-2-pyrrollidone (NMP) or similar solution is employed to remove etch residue and/or mask residue from the chip. Immersion tin plating (Technic matte Sn) or a solder plating technique can be utilized to apply solder metallization to the nodules. A flip-chip die bonder with a modified custom stage can be used to align and reflow the chips. After reflow, the 2-chip quilt was mounted onto an appropriate package.

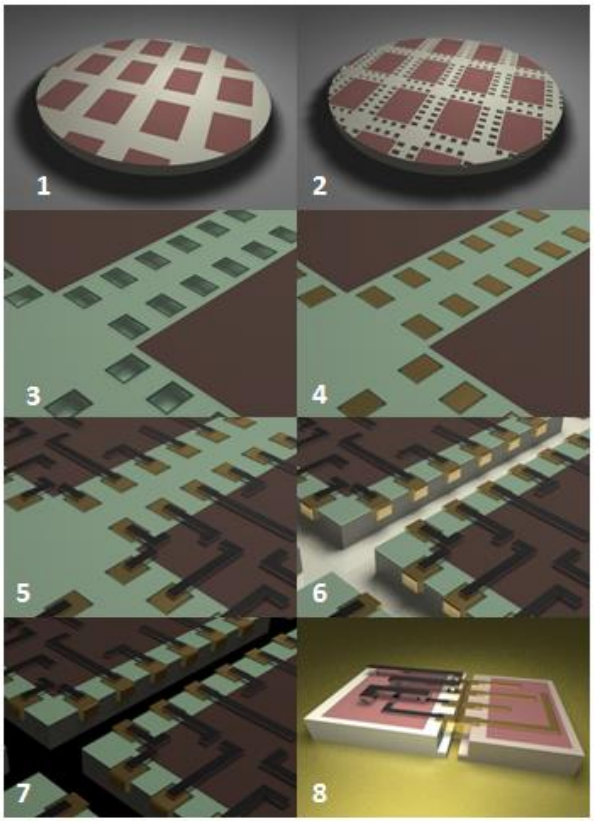

Figure 2. QP Fabrication Flow: (1) FEOL Complete; (2) Nodule Etch; (3) Seed Layer Deposition; (4) Copper Fill Plating, CMP; (5) RDL Metallization; (6) Separation Etch; (7) Backside Grind Singulation; (8) Quilt Assembly

4 LARGE ARRAY APPLICATIONS

Quilt Packaging can be used to assemble together smaller, high-yielding, chips into a large array that would otherwise be cost-prohibitive to manufacture (Fig. 3). This enables the assembly of multiple chips into a very large quilted "meta-chip" that can be used for the next generation of large sensor and imaging arrays.

Due to the simple, yet extremely precise, nature of the QP fabrication process, sub-micron chip-to-chip alignment and chip-to-chip gaps of < 10 µm are achievable when using QP for mechanical alignment, resulting in an effectively *seamless* tiled array. This extremely tight alignment and small gap enable smaller-footprint, higher-yielding die to be tiled into seamless, arbitrarily large arrays as a single large-area chip. Advances in the control circuitry for individual sensor pixels enables scaling of multiple die into larger format arrays without introducing addressing or power delivery problems. Due to QP's

fabrication method, chips are no longer constrained to square or rectangular shapes, and can be fabricated in hexagonal and other geometries in two or three dimensions, such as a curved hemispheric array, optimized for a particular application. Figure 3 shows the various 2D and 3D large format array configurations that are possible with QP.

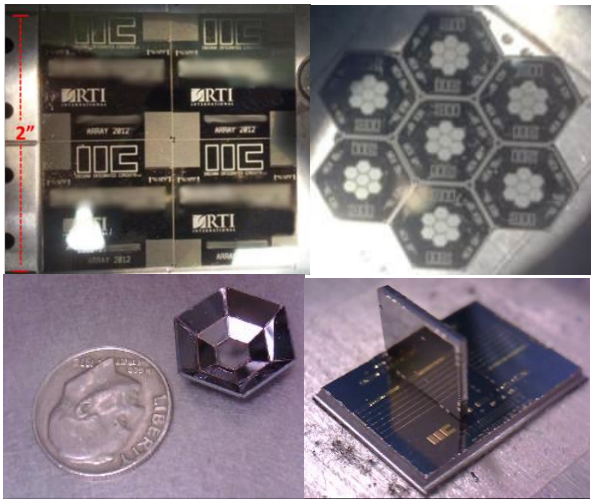

Figure 3. (Upper left) 2x2 quilted array of 1-inch chips; (Upper right) 7-chip hexagonal array quilt; (bottom left) curved hemispheric 3D QP assembly; (bottom right) orthogonal 3D-QP

5 RF MICROWAVE PERFORMANCE

QP interconnects in GaAs-based chipsets have demonstrated measured insertion loss below 1 dB at 110 GHz and less than 2.2 dB at 220 GHz [9]. They have also been demonstrated to have a chip-to-chip insertion loss of less than 0.1 dB from 50 MHz through 100 GHz, and less than 1 dB (~0.6 dB) insertion loss all the way up to 220 GHz in a heterogeneous Si-GaAs system [10]. Figure 4 shows the measured heterogeneous Si-GaAs insertion losses from DC up to 220 GHz.

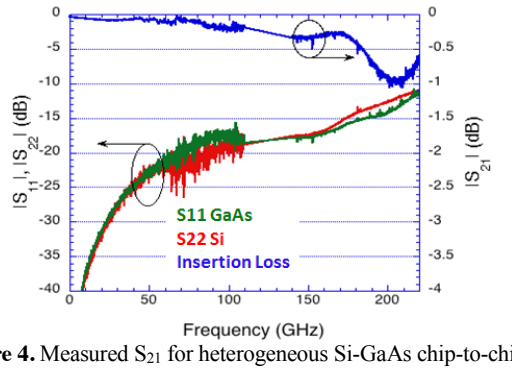

Figure 4. Measured S_{21} for heterogeneous Si-GaAs chip-to-chip interconnects. The measured insertion loss is less than 0.3 dB from 50 MHz up to 110 GHz, with a maximum insertion loss of less than 1 dB at up to 220 GHz.

The method of solder application using for the measured quilts resulted in excess solder at the nodule interface and solder wetting into the transmission line patterns. This excess solder not only affected the results at the chip-to-chip interface but also created further differences between the on-chip calibration structures and the nodule test pads, making the de-embedding more challenging. A further optimization of the assembly process using either immersion tin plating or solder plating on the nodules will improve the microwave results and assembly yield. It is anticipated that further improvements to the solder application and reflow process will result in improved and repeatable insertion loss performance.

6 RELIABILITY

6.1 Sample Mounting

Preliminary reliability testing of QP chipsets is currently underway. After reflow, the quilted chipsets used for reliability testing were mounted in standard ceramic quad flat package (QFP) with Epo-Tek H31 conductive die attach adhesive. The ceramic package was then secured to the test board. Prior to cycling, QP interconnects were tested for electrical continuity and visually inspected for defects using optical micrographs and SEMs.

6.2 Thermal Shock

Heterogeneous QP chipsets (InP-Si and Si-GaAs quilts) were then submitted to over 750 cycles of -40° to 140° C thermal shock, with a 15-minute dwell time at each peak, and a 3-second transition. Multiple homogeneous Si-Si chipsets were submitted to 500 cycles under the same parameters. Figure 4 shows the temperature test parameter over time for a single period. After the set amount of cycles, the samples were removed and re-examined. No electrical opens or increases in resistance were observed, nor were any structural defects identified by visual inspection. Additional long-term thermal cycle and shock testing, as well as other reliability tests of both heterogeneous and homogeneous quilts are ongoing.

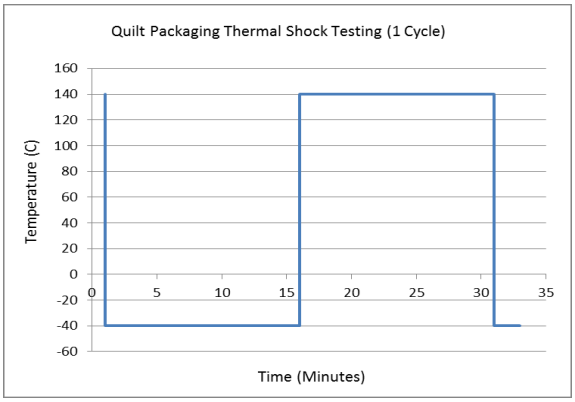

Figure 5. Thermal shock temperature test parameter for reliability testing across QP nodules.

6.2 Other Reliability Testing

Si-Si QP samples are currently subjected to JEDEC standard reliability testing for high temperature storage life (JESD22-A103D) and mechanical shock (JESD22-B104). The samples subjected to high temperature storage life condition (125C for 100 hours) showed no electrical or mechanical degradation across the nodule interconnects. Likewise, QP samples subjected to mechanical shock testing (3' and 6' feet drop across the x, y, and z axes) exhibited no electrical or mechanical degradation across the nodule interconnects. These tests are ongoing.

7 CONCLUSION

Quilt Packaging is a chip-to-chip packaging approach that enables new designs and architectures for the next generation of large format imaging and sensing devices. QP has been demonstrated in Si, GaAs, InP, and GaSb, but can also be implemented in any material that allows bulk micromachining. QP interconnect structures or "nodules" can be customized to enable precision alignment, dense I/O pitch (less than 10 um), and extremely wide bandwidth (less than 1 dB insertion loss from DC up to 220 GHz). Likewise, the chip geometry can also be customized to allow for non-rectangular arrays such as hexagonal "honeycomb" arrays as well as enable 3D and curved multichip assemblies. Preliminary thermal shock testing is performed on the multiple QP samples of various materials, with the electrical and mechanical integrity of the reflowed QP interconnects maintained after more than 500 cycles at a range of -40 to 140 C.

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