A novel dual-*k* spacer double gate junctionless transistor for digital integrated circuits

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ABSTRACT

In this paper, for the first time a novel dual-*k* spacer double gate junction-less transistor (DK-DGJLT) has been proposed. In addition to this, comparative analysis of DK-DGJLT and single-*k* spacer double gate junction-less transistor (SK-DGJLT) has been carried out. The spacer material used in SK-DGJLT is silicon nitride (Si_3N_4) whereas the spacer materials used in DK-DGJLT are Si_3N_4 and hafnium oxide (HfO_2). It has been found that, in comparison to SK-DGJLT, sub-threshold slope (SS), drain induced barrier lowering (DIBL) and off-state leakage current (I_{OFF}) in the case of proposed DK-DGJLT are reduced by ~5%, ~25% and ~25% respectively over the SK-DGJLT device. Furthermore, I_{ON}/I_{OFF} in the case of proposed DK-DGJLT has been improved by ~25% over the SK-DGJLT. This clearly indicates that, the proposed DK-DGJLT is the promising device for nanoscale low-power digital integrated circuits.

Keywords- junctionless transistor, dual-k, double gate, short channel effects.

1 INTRODUCTION

Due to manufacturing advantages over other technologies, CMOS technology has been widely used in last two decades. Metal oxide semiconductor field effect transistor (MOSFET) contains two semiconductor junctions i.e. junction between drain-to-channel and source-to-channel interfaces. In the last decade considerable efforts have been carried out by the researchers in order to reduce the size of MOSFET. However, due to requirement of ultra steep doping profile, when device scales down in sub-20 nm regime, conventional MOSFET has fabrication limitations. To overcome this problem, junctionless transistor (JLT) has been invented by J. P. Colinge [1] which requires uniform doping concentration. In addition to this, JLT has many advantages over conventional MOSFET like, bulk conduction instead of surface conduction [2], improved short channel effects, less sensitive to thermal budget. Further, the JLT fabrication process [3], [4] is simple as compared to CMOS fabrication process.

Since inception of JLT, tremendous effort have been made to develop different structures [5], [6]. Further, it has been proved by researchers that, double gate JLT (DGJLT) [7], [8] has better performance over single gate JLT in performance parameters like better gate control, DIBL and SS [9], [10] and is a potential candidate for low power applications [11]. Although in the literature it has been shown that, the addition of spacers reduces off-state leakage current (I_{OFF}), the concept of dual-*k* spacer has not been studied in DGJLT [12], [13]. In this paper, for the first time, a novel dual-*k* spacer double gate junctionless transistor (DK-DGJLT) has been proposed and comparative analysis of DK-DGJLT and single-*k* DGJLT (SK-DGJLT) has been carried out with extensive simulation. SK-DGJLT uses Si_3N_4 as dielectric whereas the proposed DK-DGJLT uses Si_3N_4 and HfO_2 as dielectric materials. Comparison of SK-DGJLT and proposed DK-DGJLT has been carried out on basis of performance parameter like DIBL, SS, I_{OFF} and I_{ON}/I_{OFF}.

The organization of rest of the paper is as follows, Section 2 discusses about the device structures and relevant device parameters of SK-DGJLT and the proposed DK-DGJLT used in the simulations. Section 3 presents detailed simulation results and discussions of performance parameters. Finally the conclusion is given in Section 4.

2 DEVICE STRUCTURES AND SIMULATION SETUP

Fig. 1-2 shows the SK-DGJLT and the proposed DK-DGJLT n-channel MOSFETs used in the two dimensional TCAD simulator. From figures it can be observed that, both devices do not have p-n junction in its source-to-channel and drain-to-channel interfaces. Further, the devices have uniform donor doping with concentration of 1.2 x 10^{19} cm^{-3} [14]. P^+ poly-silicon material has been used as gate material in both the devices. Gate oxide material in both the devices used is silicon oxide (SiO_2) having a thickness (T_{OX}) of 1 nm. The device is of silicon (Si) with a channel thickness (T_{Si}) of 10 nm. Parameters used for SK-DGJLT and proposed DK-DGJLT are listed in Table 1.

Si_3N_4 has been used as spacer dielectric material in SK-DGJLT whereas Si_3N_4 and HfO_2 [15], [16] have been used as spacer dielectric in DK-DGJLT. The spacers used in SK-DGJLT are of size ½ gate length (L_G) while the spacers used in DK-DGJLT are of size ¼ L_G each.

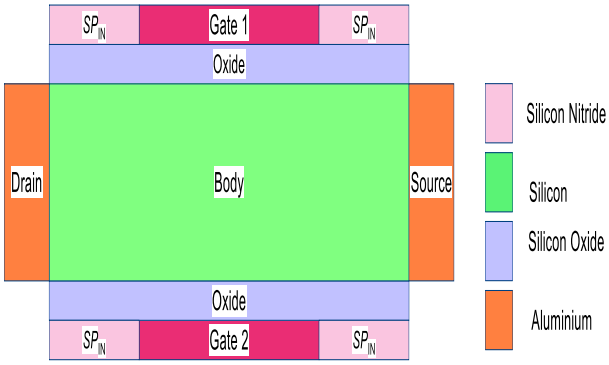

Fig.1. Device architecture for SK-DGJLT

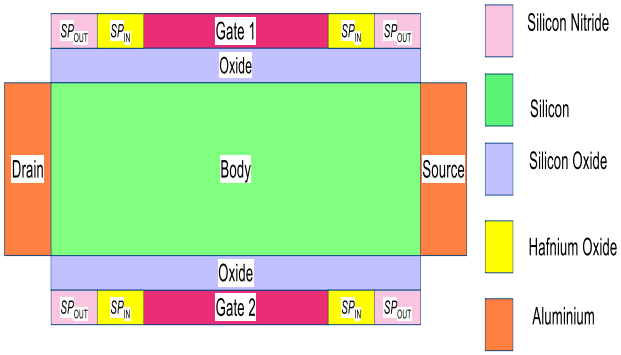

Fig.2. Proposed device architecture for DK-DGJLT

TABLE 1. DEVICE PARAMETRS USED IN SIMULULATIONS

Parameters	SK-DGJLT	DK-DGJLT
Channel length (L_G)	variable	variable
Doping concentration (N_D)	1.2 x 10^{19} cm^{-3}	1.2 x 10^{19} cm^{-3}
Channel thickness (T_{Si})	10 nm	10 nm
Gate oxide thickness (T_{OX})	1 nm	1 nm
Inner spacer (SP_{IN})	½ L_G	¼ L_G
Outer spacer (SP_{OUT})	-	¼ L_G

For fair comparison, threshold voltage (V_T) of both SK-DGJLT and the proposed DK-DGJLT has been adjusted to 0.25 V

The dielectric constant of Si_3N_4 is 7.5 whereas dielectric constant of HfO_2 is 22. HfO_2 has been used as inner spacer material (SP_{IN}) in case of proposed DK-DGJLT because dielectric constant of HfO_2 is higher than Si_3N_4. Aluminum has been used as source/drain contact material in SK-DGJLT and proposed DK-DGJLT devices.

3 SIMULATION RESULTS AND DISCUSION

Constant current method has been used and work functions of SK-DGJLT and proposed DK-DGJLT have been adjusted. Both SK-DGJLT and DK-DGJLT structures have been simulated using Cogenda Visual TCAD two dimensional drift diffusion models.

Fig. 3 shows the transfer characteristics of drain current (I_D) vs gate to source voltage (V_{GS}) characteristics of SK-DGJLT and proposed DK-DGJLT at a drain to source voltage (V_{DS}) of 50 mV for L_G = 20 nm. From Fig. 3 it can be clearly seen that, in the case of proposed DK-DGJLT there is not much improvement in I_{ON} whereas in comparison to SK-DGJLT, I_{OFF} reduces.

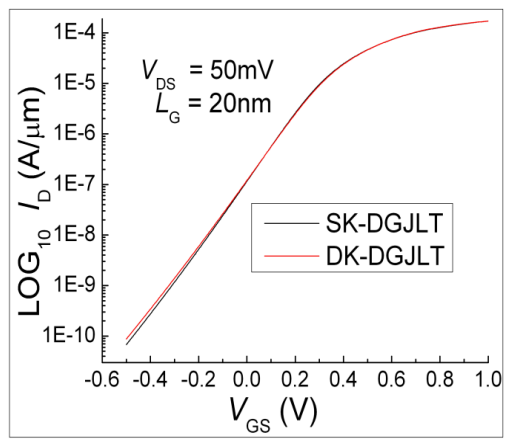

Fig.3. Log I_D Vs V_{GS} characteristics of SK-DGJLT and proposed DK-DGJLT for L_G = 20 nm and V_{DS} = 50mV at N_D = 1.2 x 10 -19 cm^{-3}

Fig. 4 shows I_D - V_{DS} characteristics of the proposed SK-DGJLT and DK-DGJLT devices at V_{GS} = 50 mV and L_G = 20 nm. From the Fig. 4 it has been found that the proposed DK-DGJLT characteristics are better than SK-DGJLT.

Fig 5 shows DIBL variation with L_G [17] for proposed SK-DGJLT and DK-DGJLT.

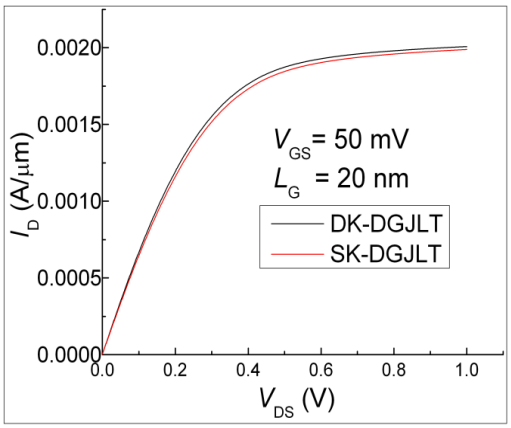

Fig.4. I_D Vs V_{DS} characteristics of SK-DGJLT and proposed DK-DGJLT for L_G = 20 nm and V_{GS} =50mV at N_D= 1.2 x 10 -19 cm^{-3}

DIBL has been calculated as follows,

$$\text{DIBL(mV/V)} = \frac{V_{\text{TLin}} - V_{\text{TSat}}}{0.95} \quad (1)$$

where ,

V_{TLin} = Linear threshold voltage adjusted to 0.25 V at V_{DS}= 50 mV by using work function engineering

V_{TSat} = Saturation threshold voltage at V_{DS} = 1 V.

From Fig. 5 it can be observed that, in comparison to SK-DGJLT, DIBL in the case of proposed DK-DGJLT reduces.

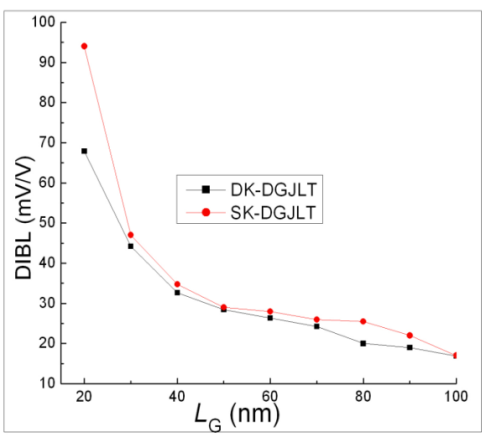

Fig.5. Variation of DIBL of proposed DK-DGJLT and SK-DGJLT with L_G at N_D=1.2 x10^{-19} cm^{-3}.

Fig 6 shows SS variation with L_G for the proposed SK-DGJLT and DK-DGJLT. SS has been calculated by varying V_{GS} for 1 decade change in I_D in sub-threshold region [18], [19]. It has been found that proposed DK-DGJLT has less SS than SK-DGJLT. The reduction in SS of proposed DK-DGJLT shows that, switching time in the case of proposed DK-DGJLT is lower as compared to SK-DGJLT.

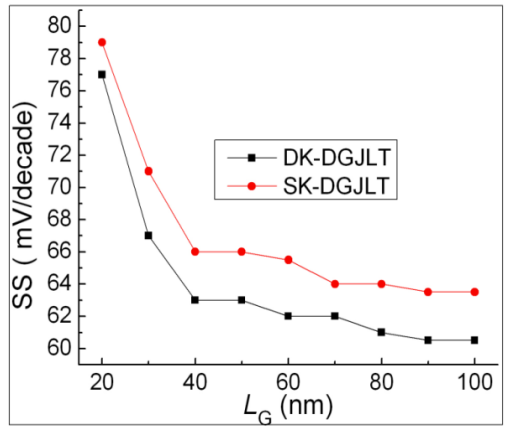

Fig.6. Variation of SS of proposed DK-DGJLT and SK-DGJLT with L_G at N_D= 1.2 x 10^{-19} cm^{-3}.

Fig 7 shows I_{ON}/I_{OFF} ratio variation with L_G for the proposed SK-DGJLT and DK-DGJLT devices. I_{OFF} current is extracted when V_{GS} is 0V and V_{DS} is 1V while I_{ON} current is extracted when V_{GS} and V_{DS} both are at 1V. Although I_{ON} in the case of proposed SK-DGJLT and DK-DGJLT devices is almost equal, the significant reduction in I_{OFF} of the proposed DK-DGJLT device leads to the significant improvement in I_{ON}/I_{OFF} ratio of the proposed DK-DGJLT device.

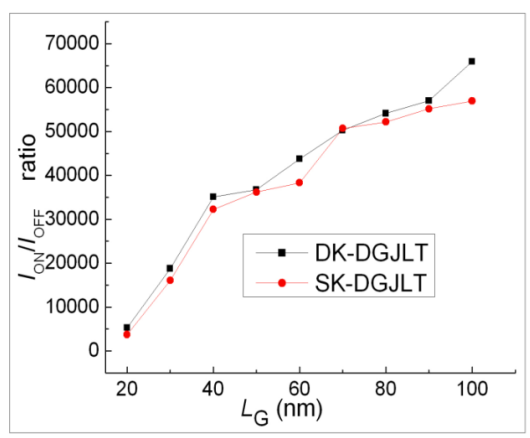

Fig.7. Variation of I_{ON}/I_{OFF} ratio of proposed DK-DGJLT and SK-DGJLT with L_G at N_D = 1.2 x 10^{-19} cm^{-3}.

4 CONCLUSION

From the simulation results it has been found that, in comparison to SK-DGJLT the proposed DK-DGJLT is a promising device for digital integrated circuits. Further SS, DIBL and I_{OFF} in the case of proposed DK-DGJLT are reduced by ~5, ~25% and ~25 % respectively over the SK-DGJLT. This improvement in SS, DIBL and I_{OFF} is mainly because of addition of high-*k* spacer near gate electrode in the proposed DK-DGJLT device which enhances depletion due to fringing electric field. Because of this parasitic resistance below the high-*k* spacers reduces which leads to improvement in SS, DIBL and I_{OFF} of the proposed DK-DGJLT device. This improvement in I_{OFF} can be utilized by using higher work function gate metal which will be useful to increase I_{ON} of the device. Further, it has been found that in comparison to SK-DGJLT, I_{ON}/I_{OFF} ratio in the case of proposed DK-DGJLT device improves by ~25%. Reduction in SS improves switching time of device whereas reduction in leakage current improves static power dissipation. Due to these improvements, DK-DGJLT can be potential candidate for nanoscale low power and high speed digital applications.

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