A Novel GaAs-on-Si MOSFET for Analog Integrated Circuits

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ABSTRACT

Over the last decades silicon (Si) has proven its superiority in the semiconductor world. However, since on-state drive current (I_{ON}) of metal oxide semiconductor field effect transistor(MOSFET) depends upon the channel mobility, more attention has to be given on high electron mobility channel materials such as GaAs, InGaAs, InP etc. Further, to combine the properties of Si with GaAs attributes namely higher electron mobility and switching speed, we tried to combine properties of Si and GaAs materials in a novel device named as GaAs-on-Si MOSFET. Further, the comparative analysis of GaAs-on-Si, Si and GaAs MOSFETs has been carried out by using the Cogenda Visual TCAD tool. It has been observed that I_{ON} in the case of proposed device is improved by ~40% and ~5% respectively over the Si and GaAs MOSFETs.

Keywords: GaAs-on-Si MOSFET, analog figures of merit, short channel effects, gate capacitance, unity gain frequency.

1 INTRODUCTION

Since from the beginning of semiconductor world, Si has travelled its journey with advantages of small mass, good carrier capability, low cost, maximum wafer diameter etc.[1]. As per International technology roadmap for semiconductor (ITRS) 2013, more attention has been given for improving electron mobility in the channel region [2,3].For that purpose, semiconductor with higher electron mobility has attracted researchers to improve I_{ON}. These materials mainly includes III-V semiconductors such as GaAs, InGaAs, InP etc. However cost of fabrication for such materials is higher than Si [4].

To combine properties of Si with GaAs attributes namely higher electron mobility and switching speed, we tried to combine properties of Si and GaAs materials (see Table 1) in a novel device named as GaAs-on-Si MOSFET. In this paper GaAs-on-Si MOSFET has been proposed with GaAs as a channel material while substrate is made up of Si. Conventional planar structure has been used for simplicity. Further a fabrication flow has been proposed for fabrication purpose. In adition to this, digital and analog parameters also have been analysed for a proposed strucutre. Rest of the paper has been arranged in four sections. Section 2 discusses about device structure and fabrication process while section 3 focuses on simulation process as well as results and finally section 4 concludes a proposed work.

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Properties	Silicon	GaAs
Bandgap (eV)	1.12	1.42
Electron Mobility (cm^2/v-s)	1450	9200
Hole Mobility(cm^2/v-s)	480	400
Intrinsic carrier Concentration (cm^{-3})	$1.45x10^{10}$	$1.79x10^{6}$
Saturation Velocity (cm/sec)	$1x10^{7}$	$1.2x10^{7}$
Dielectric Constant	11.9	13.1
Thermal Conductivity (W/cm-^{0}C)	1.5	0.46

Table1. Electrical Properties of Si and GaAs materials

2 DEVICE STRUCTURE

Cogenda visual TCAD has been used to simulate the device structure shown in Fig. 2. Conventional planar MOSFET structure has been chosen due to its less complex and well understood process. Rather chosing a complete Si body, we devide body into two parts as a channel and substrate. Channel is made up of GaAs while substrate is made up of Si for better carrier capability.

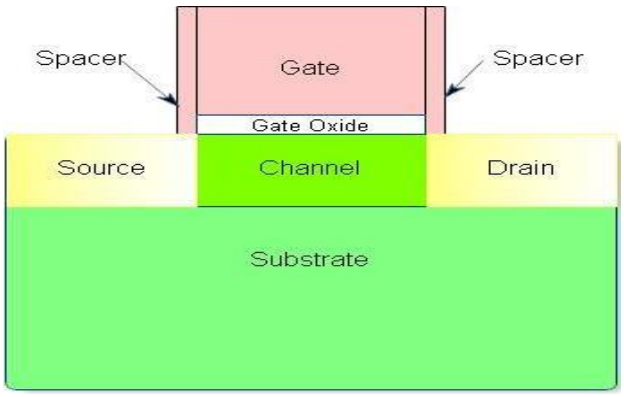

Fig.1 Proposed GaAs-on-Si Device Structure

Device parameters for proposed device has been shown in Table 2. Source and Drain have been formed through

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gaussian doping on a GaAs channel. Channel and Substrate region have been uniformly doped. Nitride material has been used to form spacers.

Parameter	Unit	GaAs-on-Si MOSFET	Simple GaAs or Si MOSFET
Physical gate length (L_G)	nm	200	200
Gate oxide thickness	nm	4	4
Source/Drain Doping	cm^{-3}	1×10^{20}	1×10^{20}
Channel doping	cm^{-3}	5×10^{16}	5×10^{16}
Substrate doping	cm^{-3}	5×10^{16}	5×10^{16}

Table 2. Device parameters used in simulation

2.1 Fabrication Process Flow

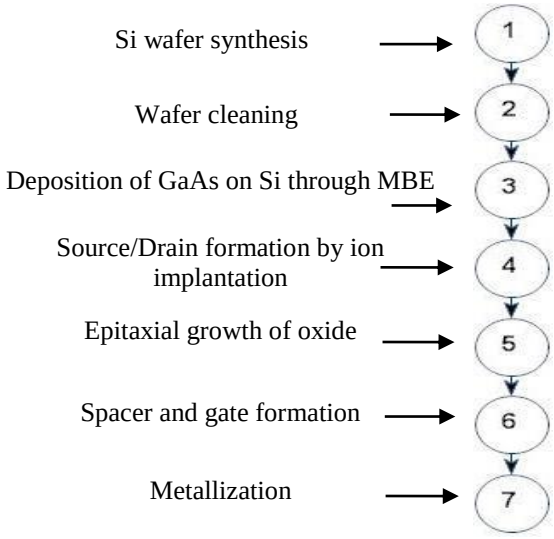

Fig.2 Fabrication Process Flow for GaAs-on-Si MOSFET

Fabrication is the most crucial process in microelectronics. It affects device performances for small changes in the process. The fabrication process flow for proposed GaAs-on-Si MOSFET is shown in Fig.2.

Fabrication process starts with Si wafer synthesis. Neat and clean area with constant environmental conditions should be maintained to avoid any manufacturing errors. Si wafer has been formed through conventional process. Thereafter wafer is cleaned to remove pores as well as to reduce traps on a wafer. Various methods have been proposed to deposit GaAs material on Si [5-9].

Further, a simple molecular beam epitaxial process has been selected to deposit GaAs on Si. Deposition of GaAs on Si may form island pattern on Si, to avoid this double deposition method is used. Thereafter source / drain has been formed through ion implantation process. n-type dopant material has been implanted on channel which is made up of GaAs. Due to lattice mismatch, there are formation of traps which increases interfacial trap density for higher voltages. A thin oxide layer has been deposited epitaxially on channel to form gate oxide. Gate is formed by n-type poly Si material. To avoid hot electron effect as well as to reduce gate induced drain leakage, spacer has been implanted on both sides of gate. Fabrication process ends with the formation of contacts at required terminals through metallization. In this way proposed novel GaAs-on-Si can be fabricated.

3 RESULTS AND DISCUSSION

For the first time GaAs-on-Si MOSFET has been designed with depositing GaAs directly on Si material. Conventional planar structure has been chosen due to its simple method of fabrication. By applying gate bias ranging from -0.5V to 1V, with a constant drain voltage of 50 mV, a channel has been formed between drain and source. Electrons from source are travelling towards drain, thus drain current has been generated from drain towards source.

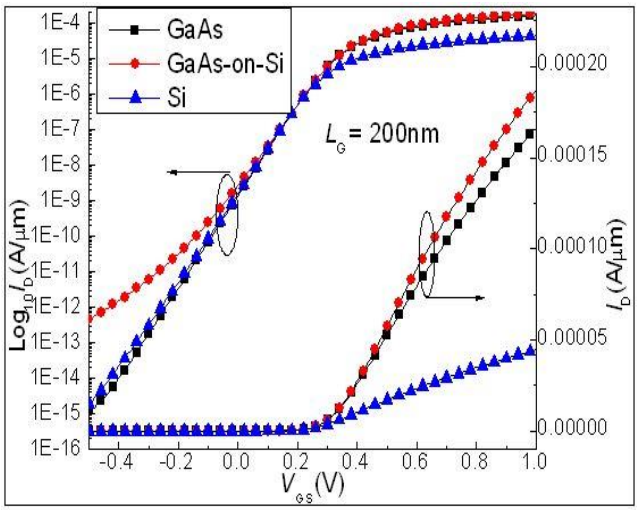

Fig.3 I_D vs V_{GS} characterstics of GaAs, GaAs-on-Si and Si MOSFETs at V_{DS}= 50mV.

Fig. 3 Shows I_D vs V_{GS} characterstics comparison for GaAs, GaAs-on-Si and Si n channel MOSFETs in which GaAs-on-Si has highest I_{ON} as compared to simple Si or GaAs MOSFET. This is mainly due to higher electron mobility in a channel region made up of GaAs material. However more leakage has been found out from logarithmic curve which affects digital performance parameters. This leakage is mainly due to mismatch found at the interface of GaAs and Si. It has been found that, despite having higher leakage in the proposed GaAs-on-Si MOSFET, I_{ON} in the case of proposed device is improved by ~40% and ~5% respectively over the Si and GaAs MOSFETs. Threshold voltage has been adjusted for better comparison at 0.2 V through work function enginnering.

Simple drift-diffusion mobility models have been used for device simulation.

3.1 Digital Performance

Instead of having more leakage, due to higher current the digital performance parameters such as subthreshold slope (SS), drain induced barrier lowering (DIBL) have been analysed and listed in Table 3.

Parameter	GaAs	GaAs-on-Si	Si
I_{ON} (A)	371×10^{-6}	391×10^{-6}	276×10^{-6}
I_{OFF} (A)	2.49×10^{-9}	6.39×10^{-7}	2.66×10^{-9}
DIBL (mV/V)	22.1	212.6	21.1
SS (mV/ Dec)	79	190	81

Table 3 Comparison of I_{ON}, I_{OFF}, DIBL and SS for GaAs, GaAs-on-Si, Si MOSFET

I_{ON} and I_{OFF} has been calculated at V_{DS} = 1V for V_{GS} = 1V and 0V respectively. It has been found that I_{ON} and I_{OFF} both are higher for GaAs-on-Si MOSFET as compared to Si and GaAs MOSFET. Further DIBL and SS have also been found to be more. DIBL is calculated as per formula given in [10].

3.2 Analog Performance

Increase in $I_{ON,}$ has attracted more attention to simulate proposed device to find analog performance parameters. These analog parameters include gate capacitance (C_{GG}), transconductance (G_M), unity gain frequency, G_M/I_D ratio etc. C_{GG} has been extracted and compared with change in gate voltage as shown in Fig.4. It has been found that for variable V_{GS} from 0V to 1V, C_{GG} has lowest capacitance value for GaAs-on-Si MOSFET than GaAs and Si. This is mainly due to n-type doping behaviour of Si at interface between GaAs and Si which reduces insulating area responsible for gate capacitance formation. Lower capacitance has strengthen device for high frequency applicaion.

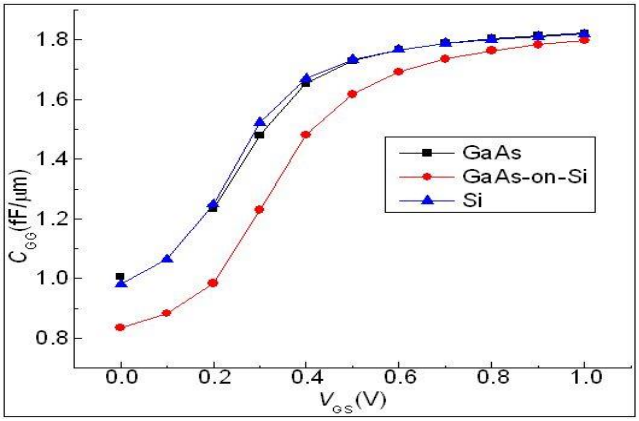

Fig.4. Variation of C_{GG} with V_{GS} for GaAs, GaAs-on-Si and Si MOSFETs for L_G = 200nm

Higher gate transconductance in GaAs-on-Si MOSFET has proved its better suitability for analog applications than simple GaAs and Si which leads to less output resistance. Fig.5 shows variation of transconductance with V_{GS} for GaAs, GaAs-on-Si, Si MOSFET. Improvement in G_M is because of higher mobility of GaAs in channel region.

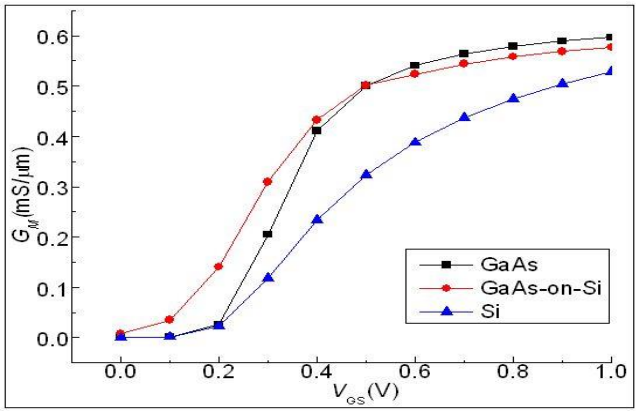

Fig 5. Variation of transconductance with V_{GS} for GaAs, GaAs-on-Si and Si MOSFETs for L_G=200nm

At higher voltages, increase in interfacial trap density lowers G_M below simple GaAs MOSFET while proposed device still having higher performance than conventional Si MOSFET.

Fig.6 shows variation in unity gain frequency with respect to different gate voltages for GaAs, GaAs-on-Si and Si MOSFET. This unity gain frequency has been calculated by following formula

$$\text{Unity Gain Frequency } (F_T) = \frac{G_M}{2\pi C_{GG}}$$

Due to higher gate transconductance as well as lower gate capacitance unity gain frequency has also been improved in a proposed device. However traps in the channel region at interface affects the unity gain frequency.

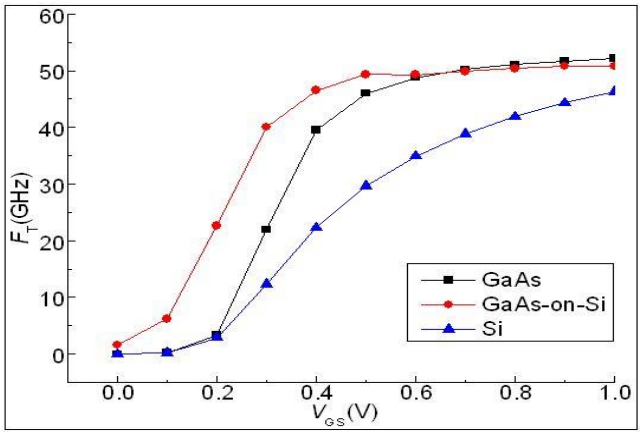

Fig.6 Variation of unity gain frequency with V_{GS} for GaAs, GaAs-on-Si and Si MOSFETs for L_G=200nm

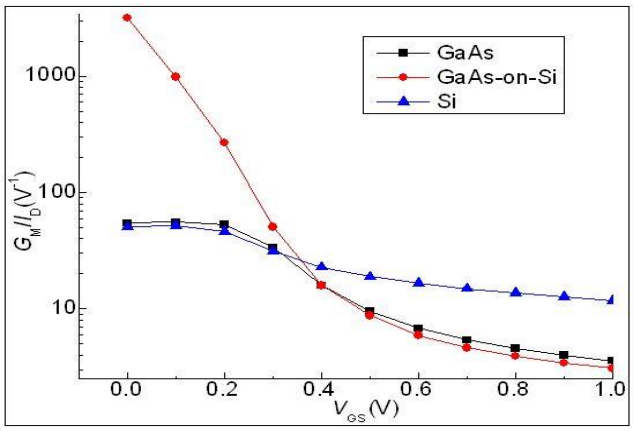

Fig 7. Variation of G_M/I_D with V_{GS} for GaAs, GaAs-on-Si and Si MOSFETs for L_G=200nm

From Fig. 7 it can be shown that, for a proposed device G_M/I_D ratio has been increases in weak inversion region while reduces in strong inversion region. This behaviour shows that the proposed GaAs-on-Si MOSFET is the promising device for low power analog application of a MOSFET [10].

4 CONCLUSION

In the proposed GaAs-on-Si MOSFET, the presence of GaAs channel improves the electron mobility of the proposed device which results in an improvement in drain current of the MOSFET. Further, due to higher doping in the channel the increased inversion layer thickness reduces the gate capacitance. Furthermore, the significant improvement in G_M , G_M/I_D, and F_T over the Si and GaAs MOSFETs, shows the superiority of the proposed GaAs-on-Si for analog integrated circuits. Further, the improved G_M/I_D in weak inversion region and the reduced G_M/I_D in strong inversion region shows the suitability of the proposed device for low-power designs.However, due to higher doping at the channel-substrate interface, the short channel effects in the proposed device also increases. Thus lower fabrication cost, improvement in I_{ON}, significant improvement in G_M, G_M/I_D and F_T in the proposed GaAs-on-Si MOSFET shows its suitability for low-power analog integrated circuits.

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