Degradation Mechanisms in Electric Double Layer Capacitors Subjected to Voltage and Temperature Stress Testing

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ABSTRACT

To ensure that EDLCs are capable of satisfying reliability requirements, original equipment manufacturers (OEMs) need to be able to test and screen samples from several suppliers. In order to accomplish this, the screening test conditions would need to accelerate EDLC degradation without over-stressing them. In this paper commercially available EDLC samples from different manufacturers were subjected to voltage and temperature step stress testing. Each sample's capacitance and DC (internal) resistance were monitored. The variation of these electrical parameters with the applied stress levels is used to identify margins outside the rated temperatures and voltages, within which accelerated testing can be performed. We also identify the failure modes associated with increasing and voltage and temperature stresses. The underlying failure mechanisms associated with the observed failure modes are also determined through post-test failure analyses.

Keywords: Supercapacitors, screening, reliability exfoliation, SEI.

1 INTRODUCTION

Unlike other commonly used capacitor technologies, electric double layer capacitors (EDLCs) do not derive their capacitive energy storage properties from a conventional dielectric, as shown in Figure 1. Commercially used EDLCs use graphitic carbon deposited on aluminum or copper current collectors as electrodes. These electrodes are wound together with a separator soaked in an electrolyte containing ionic salts. Upon application of an external potential (during charging), the salt dissociates into its constituent anions and cations, and each of these species forms a double layer at the oppositely charged electrode. The charged species are held in place by electrostatic forces of attraction. The work done in separating these charges can be recovered when the externally applied potential is removed and replaced with a load. Unlike Li-ion batteries, the charge carriers do not diffuse into the electrodes in EDLCs. Hence these carriers have greater mobilities. Consequently, EDLCs have higher power densities compared to Li ion batteries.

Due to their high power densities, EDLCs are used to supplement high energy density power sources (such as lithium ion batteries and fuel cells) in applications such as automotive kinetic energy recovery systems. At the other end of the spectrum, EDLCs are also used in data storage technologies such as redundant array of independent disks (RAID). Such applications demand high reliability from the EDLCs used. Original equipment manufacturers (OEMs) can choose from several different manufacturers. However, in order to choose a supplier, OEMs must be able to screen samples from several different suppliers in a short period of time by using accelerated tests.

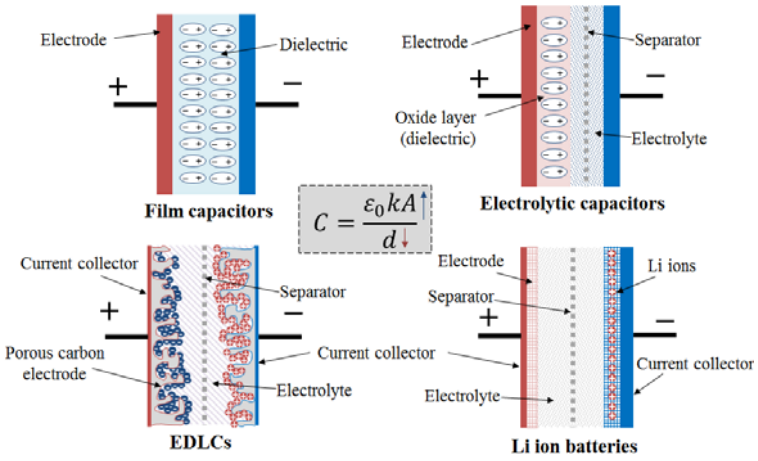

Figure 1: Charge storage in various energy storage technologies

EDLCs have usable lives of well over 100,000 cycles [1]. They are also known to be fairly robust under temperature ageing and thermal shock conditions [2]. Hence in order to accelerate test times, in this paper, we use progressively increasing voltage and temperature stresses. We then identify the associated failure modes seen in EDLCs. Based on results and trends from the stress tests and, we recommend voltage and temperature conditions within which accelerated testing can be performed. Such guidelines are currently unavailable.

We validate the suggestions by identifying the underlying failure mechanisms. This is achieved by performing material level analyses on deconstructed, tested and untested samples. Fourier transformed infrared spectroscopy (FTIR) was used to analyze the electrolytes, and scanning electron microscopy was (SEM) was used to analyze the electrode material. We describe how the reaction of the electrode and electrolyte could lead to formation of resistive films and degrade the structural integrity of the electrodes. These mechanisms irreversibly affect the electrical performance of EDLCs.

2 TEST DESIGN

Seven samples from six different manufacturers were subjected to voltage and temperature step stress testing. The samples along with their electrical ratings are shown in Figure 2. Temperature ratings are shown in Table 1.

The two parameters which were periodically measured for each sample over the course of the test were capacitance (C) and DC resistance (DCR). The equipment that was used in our study included the Arbin BT-2000 (battery tester, for electrical characterization) the Agilent N6705B (DC power analyzer, for voltage stressing) and a Yamato DVS402 (constant temperature oven for temperature stress testing).

Figure 2: Samples used in the study

2.1 Measurement of Capacitance and DCR

Capacitance (C) and DCR measurements were made in accordance with the standards IEC 62391-1 and JIS 5160-1. For each measurement, the samples were first charged up to their rated voltages, and held there for 30 minutes. They were then discharged with currents I_D, which were calculated based on the capacitance and voltage ratings of the sample as described in the IEC standard. The currents used to discharge the samples for DCR measurements (DC resistance method) were 10 times larger than the currents used for capacitance measurements as shown in Table 1.

Sample	Discharge Currents, I_D (A)		Rated Temp (°C)
	Constant Current	DC Resistance	
A	0.004	0.04	70
B	0.002	0.02	70
C	0.005	0.05	65
D	0.002	0.02	70
E	3.500	35.00	60
F	0.009	0.09	60
G	0.010	0.10	70

Table 1: Discharge currents used during measurement of electrical parameters of test samples

A sample charge-discharge curve for capacitance and DCR measurements is shown in Figure 3. Based on the constant current (capacitance) discharge profile, the time t_2-t_1 taken for the capacitor to discharge from 80% of its rated voltage (U_1) to 20% of its rated voltage (U_2) can be calculated, and then used to measure the capacitance C as shown in equation 1. Similarly, the ohmic potential drop (ΔU) at the beginning of discharge can be used to calculate the DC Resistance (R_{DC}) as shown in equation 2.

$$C = \frac{I_D \times (t_2 - t_1)}{U_1 - U_2} \quad (1)$$

$$R_{DC} = \frac{\Delta U}{I_D} \quad (2)$$

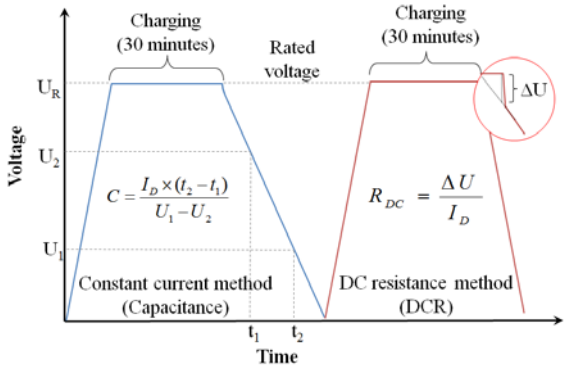

Figure 3: Sample charge discharge curve used for C and DCR measurements

2.2 Step Stress Test Methodology

All samples were first characterized at room temperature, before being stressed. Two sets of step stress tests were performed; one each subjected to temperature and voltage stresses. One sample of each type was included in each test. For the temperature step stress test, samples were first heated to their maximum rated temperatures. They were then held there for an hour, before being cooled down to room temperature. Following the cool-down, capacitance and DCR were measured at room temperature. The process was repeated with the temperature set point being raised by 10°C each time, until the capacitors were stressed at a maximum temperature of 150°C. The capacitors were not biased during temperature stress test.

Similarly, for voltage step stress testing, the samples were charged up to their rated voltages, and held there for 30 minutes. They were then discharged completely. Capacitance and DCR were then measured at room temperature. The process was repeated by charging the samples to a voltage level that was 0.5 V higher than the previous set point. The voltage stress tests were performed at room temperature. Samples E and G could not be included in the voltage test, as their test requirements exceeded the instrumentation capability.

3 RESULTS AND DISCUSSION

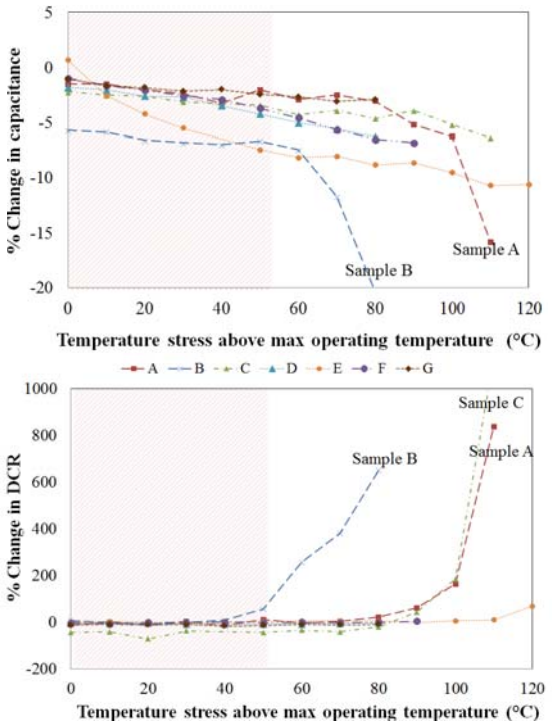

Figure 4: Capacitance variation (above) and DCR variation (below) for temperature step stress tests

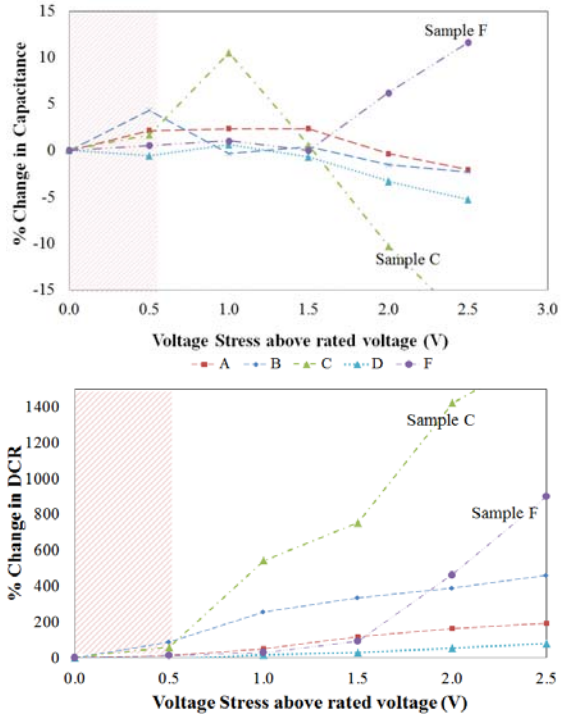

Figure 5: Capacitance variation (above) and DCR variation (below) for voltage step stress tests

Figure 4 depicts the results from the temperature step stress tests. It is seen that both capacitance and DCR either remain relatively constant, or degrade very gradually as the samples are stressed at temperature levels within 50°C of their rated temperatures. However, as the samples continued to be stressed at higher temperatures, a marked decrease in capacitance and increase in DCR could be seen in some samples.

In the voltage stress tests, the capacitance of samples initially increased with voltage stressing (Figure 5). However, with further increase in voltage stress levels, the capacitance of most samples decreased, with the only exception being sample F. The DCR trends for voltage stress tests resembled those seen in the temperature step stress test.

With regard to capacitance degradation, it is clearly evident from our results that voltage and temperature stresses induce different failure mechanisms within the EDLCs. A decrease in capacitance often seems to be accompanied by an increase in DCR. This correlation could imply that the underlying mechanisms behind this behavior be coupled. However, since there are cases where a significant drop in capacitance is not accompanied by a large increase in DCR (sample E under temperature stressing, and sample D under voltage stressing), the two degradation mechanisms could be distinct.

The failure modes in both sets of stress tests were increase in DCR and decrease in capacitance. A change in the degradation trends is seen when samples are subjected to temperatures more than 50°C above their rated temperature. Similarly, subjecting samples to voltage stresses more than 0.5V above their rated voltages causes the degradation to accelerate rapidly. Hence, while designing accelerated tests, OEMs should try to stay within these limits (indicated by the shaded regions in Figure 4 and Figure 5).

4 FAILURE ANALYSIS

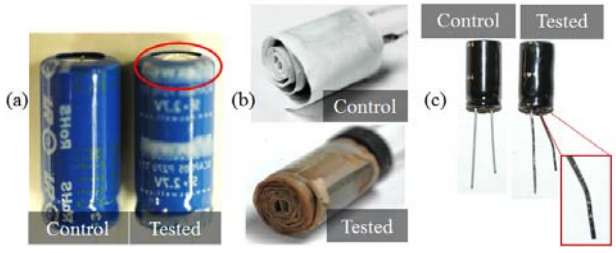

Figure 6: Visual inspection of tested samples showing (a) bulging of can (b) separator degradation (c) lead corrosion

Figure 6 shows the physical changes observed in tested samples. Bulging and corrosion of leads were seen on most samples; more prominently so on samples subjected to thermal stressing. Both these changes indicate that samples experienced a loss of electrolyte, either due to side reactions occurring within the EDLC, or leakage through the seal. This implies that there was a reduction in the number of active charge carriers, which could lead to a decrease in

capacitance. Removal of the external metallic can (packaging) off some samples revealed degraded separators, showing signs of oxidation. This degradation could affect ion mobilities, as the porosity of the separator may have been altered. This would be reflected as an increase in DCR, as seen in our results.

Strips of the electrode assembly from samples subjected to temperature and voltage step stress testing were removed, and washed in distilled deionized water to remove the salts from the electrolyte. They were then examined under the scanning electron microscope. It was seen that in the temperature stress tested samples' electrodes, the electrode material agglomerated in some regions (Figure 7). In the voltage tested samples, the electrodes showed signs of exfoliation and cracking. These were visible at fairly low magnifications as shown in Figure 8. FTIR analysis was also performed on EDLC electrolytes, and it was seen that all samples except B used propylene carbonate (PC) as a primary solvent. Sample B used Acetonitrile (AN).

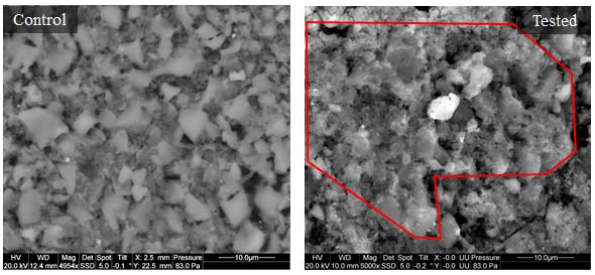

Figure 7: SEM micrographs showing active material agglomeration in electrodes of temperature tested sample

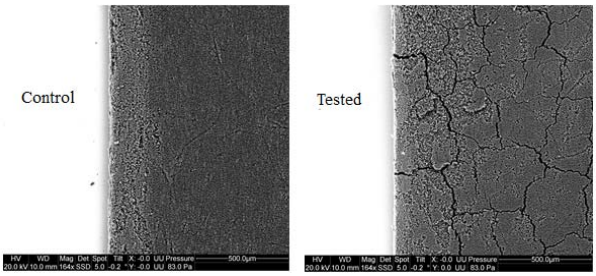

Figure 8: Electrode exfoliation in voltage tested sample

5 FAILURE MECHANISMS

During solvation of the EDLC salts in PC, the dissociated ions from the salt are surrounded by PC molecules to form a sphere known as solvation sheath (more information in [3]). These solvation sheaths are significantly bulkier than the original ions, which are represented as X^+ in Figure 9. When an external potential is applied to the EDLC, such as the voltage stresses in our test, the solvation sheaths, as a whole, are driven through the porous carbon electrode. The electrodes would experience greater stresses with increasing electric field strengths that result from greater voltage stresses. As a result, the electrode is prone to cracking and exfoliation, as seen in Figure 8. This would also be reflected as an increase in capacitance due to the increased surface area available for double layer formation. In designing accelerated tests, excessive exfoliation would represent an overstress.

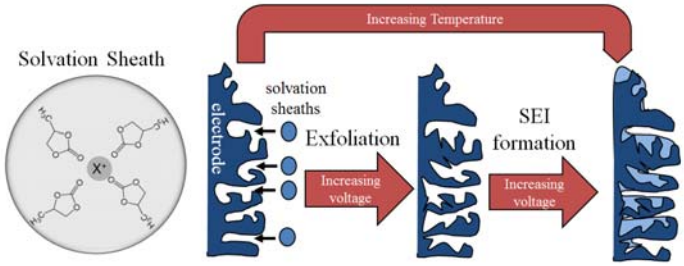

Figure 9: Degradation mechanisms in EDLC electrodes

Continuous increase in the voltage stress applied would lead to decomposition and reduction of the electrolyte with the electrode material. This would lead to formation of a new resistive layer on the electrode referred to as a solid electrolyte interphase (SEI). Thermodynamically, SEI formation would also be favorable at elevated temperatures, and hence the similarity in results from both our tests. The agglomeration seen in Figure 7 could be an SEI layer. Since SEI formation by decomposition of PC is known to be accompanied by gas generation [4], we would see bulging in tested samples. The increased pressure within the EDLCs could cause the electrolyte leakage seen in our tests. SEI formation also consumes active charge carriers and causes reduction of the surface area of the electrode, both of which would lead to a loss of capacitance. The resistive nature of SEI would also cause increased DCR of EDLCs.

6 CONCLUSIONS

When designing accelerated tests for EDLCs, temperature stresses should be limited to a maximum of 50°C over the rated temperature. Similarly, for voltage stress tests, the stress levels should be limited to 500mV over the rated voltage. Commonly observed failure modes under these stress conditions is an increase in DC resistance and a loss of capacitance. These failure modes can be explained by formation of resistive SEI layers which leads to a loss of both active charge carriers as well as surface area available for double layer formation. A temporary increase in capacitance may be obtained due to the exfoliation of carbon electrodes by solvation sheaths under voltage stresses.

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