

# Advancements in Microelectronics-Grade Carbon Nanotube Materials for NRAM<sup>®</sup> Device Manufacture and Analysis of Carbon Nanotube Mass in End User Devices

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## ABSTRACT

Providing materials for use in semiconductor manufacturing is challenging due to the extreme quality levels required for low metal ion and defect levels. This challenge is much greater for suppliers of materials containing long, high-aspect-ratio nanostructures such as carbon nanotubes (CNTs) that are deposited by spin coating. In addition, safeguards and practices for minimizing environmental and exposure impacts of CNTs in manufacturing and in end devices are key to enabling commercial use. This paper will review the quality improvements made by Brewer Science in the development of its third-generation CNT formulation with 10 times the CNT concentration of previous materials and their integration into a 4-MB nanotube memory device. The paper's primary focus is on providing a review of safeguards, controls, impacts, and potential quantities of CNT materials in end use devices.

**Keywords:** carbon nanotubes, electronics grade, nanotube, memory, embedded, environmental, impact

## 1 INTRODUCTION

Developing materials for advanced node manufacturing is a challenge due to the stringent requirements for trace metal ion concentrations, defects, and coating quality [1]. CNT formulations are especially challenging because they are difficult to disperse and are typically contaminated with catalyst metals. Brewer Science's third generation of material for CNT memory manufacture has a CNT concentration 10 times greater than previous materials and meets a much more stringent metal ion concentration level specification that is one-fifth the previous specification level; the material is also a surfactant-free, room-temperature-stable formulation. Increasing CNT concentration is critical to providing CNT memory device manufacturers with reduced material consumption and process cycle time, but higher CNT concentrations increase the difficulty of achieving both shelf life stability and metal ion purity levels. The materials were characterized using analytical tests and on-wafer validation for CMOS applications. Zeta potential and liquid particle counting were used for shelf life and formulation stability studies.

Increased concentrations of CNTs in these new generations of materials greatly reduce the number of coatings and quantity of CNT material required to achieve the targeted fabric thickness for an NRAM<sup>®</sup> device. The

memory cell stack and process for a 130-nm cell size are presented for a 4-MB NRAM<sup>®</sup> device. The memory cell is located in the back-end metal layers of the device [2][3]. NRAM<sup>®</sup> device technology provides the inherent benefit of a storage cell that does not require area on the front-end silicon layers and can be added or stacked during the back-end metal processes. Basic performance data will also be reviewed for a 130-nm cell size with a focus on embedded memory device applications [4]. In a 256-KB volatile memory device using a 30-nm CNT fabric with 350-nm cell size in an embedded microcontroller, 1.40 ng of CNTs remain in the device, encapsulated in SiNx, SiOx, and TiNx layers that are in turn encapsulated in chip passivation and packaging.

This work focuses on the development of electronics-grade CNT formulations for commercialization of CNT memory devices. Development and commercialization of these critical materials are required to empower innovation and tap the potential for NRAM<sup>®</sup> device technologies.

## 2 FORMULATION PROPERTIES

Key parameters used in this optimization were trace metal concentration, CNT size distribution, stability (aggregation affinity), and shelf life. Low trace metal concentration is a basic requirement for any electronic materials, specifically,  $\leq 10$  ppb for 90-nm nodes and dropping to  $\leq 1$  ppb for 45 nm and below.

We have developed and validated a method for metals analysis in CNT dispersions on our Varian 820 inductively coupled plasma mass spectrometer (ICP-MS) with Agilent SPS 3 autosampler. Ions evaluated include Al, Ca, Co, Cr, Cu, Fe, K, Mg, Mn, Mo, Na, Ni, Ti, and Zn. Calibration ranges depend on expected values and ion responses. For our analyses, we used three different ranges (1-100 ppb, 0.5-50 ppb, 0.5-20 ppb) with blanks included in each curve. The calibration curves established yielded coefficients of determination ( $R^2$ ) greater than or equal to 0.9999. Instrument detection limits are less than or equal to 1 ppb for all metal ions tested. Fig. 1 shows the lot history of metal ions in our materials.

In addition to the metals analysis, we had our materials evaluated for on-wafer residual ions using total reflection x-ray fluorescence (TXRF) through a contract laboratory. The TXRF data show that on-wafer concentrations remain below  $1.0 \times 10^{10}$  atoms/cm<sup>2</sup>, values consistent with microelectronics-grade material used in production fabs.

Dispersions of CNTs can have a propensity to aggregate depending on the ionic balance between the particles and the dispersing solvent. Zeta potential is used to provide this

understanding. Samples were sent to the U.S. Army Engineer Research and Development Center (ERDC) where a ZetaSizer Nano-Z (Malvern, Worcestershire, UK) was used to determine the zeta potential of our dispersions. Typically, particles with zeta potentials of less than -30 mV or greater than +30 mV do not have the affinity to aggregate. Particles with voltages between -30 mV and +30 mV tend to aggregate. Fig. 2 shows the distribution of zeta potentials for our material. The figure clearly shows that all of the particles have a zeta potential of less than -30 mV, indicating that the dispersions are stable.

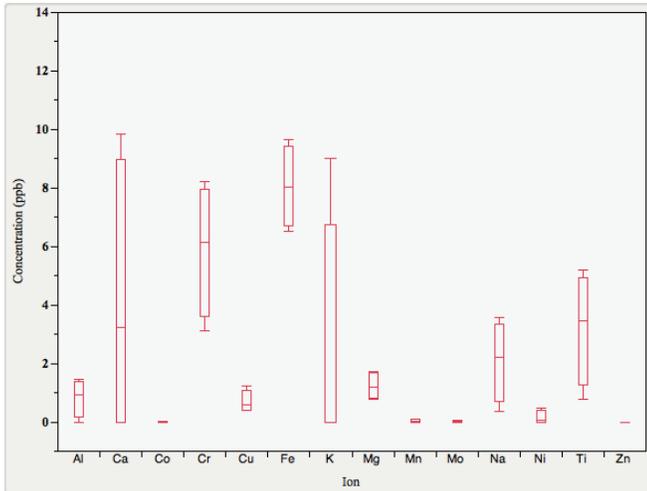


Figure 1. Multi-lot ion analysis of CNT solutions.

The ZetaSizer Nano-Z can also be used to determine the size distribution of particles in the dispersions relative to polystyrene latex spheres. This information can indicate aggregates that form as a function of time by looking for shifts in the distribution. Fig. 3 shows the analysis for particle size distribution within 2 weeks of manufacturing. Shelf life studies are under way using the identified parameters of ions, zeta potential, and size distribution versus time to determine how long the materials stay viable.

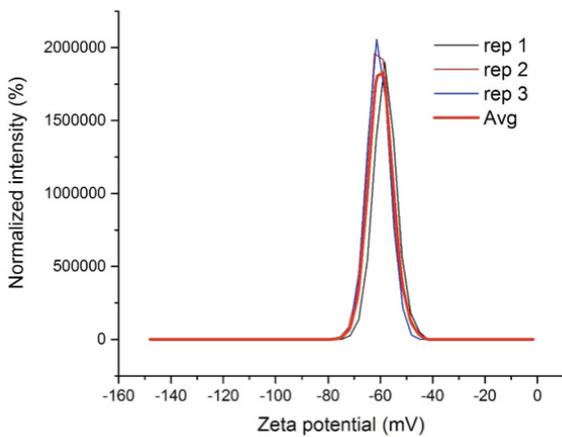


Figure 2. Zeta potential; all potentials are less than -30 mV.

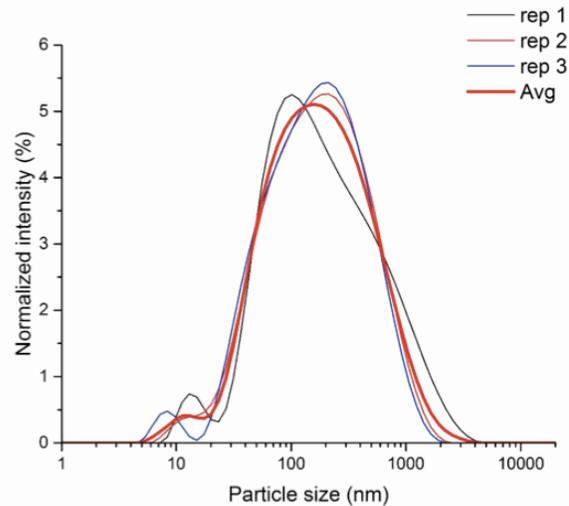


Figure 3. Triplicate scans for particle size distribution.

Atomic force microscopy (AFM) was used to measure CNT length and diameter distribution by diluting the CNT solution by ~50 times and spin coating onto a silicon wafer for testing. Few tubes remain touching, allowing the software to extract the measurements for both length and diameter from the AFM data file. The average CNT diameter was 1.6 nm with a standard deviation of 0.44 nm; range was from 0.65 nm to 2.99 nm. Fig. 4 shows a typical histogram of the CNT length distribution and diameter distribution. Most of the CNTs are 200-500 nm in length, and most are single-walled with some multiwalled.

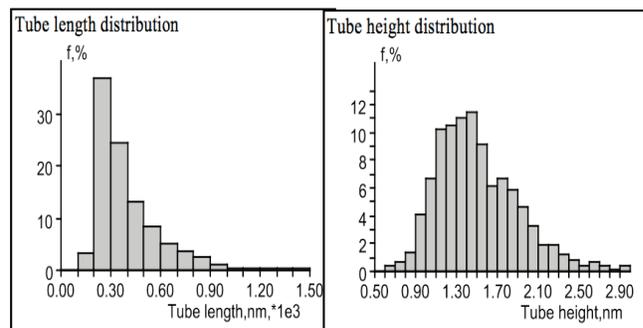


Figure 4. CNT length and diameter distributions by AFM.

### 3 COATING PROCESS AND IMPACTS

CNT formulations are aqueous and require special considerations for spin-coating application [5]. Achieving the target coating thickness of 30 nm requires multiple coat/bake cycles. Increasing the CNT concentration minimizes the number of coating cycles, which reduces material and process costs. The process integration is compatible with back end of line (BEOL) for all layers and process steps, allowing the memory cell itself to be located in the metallization stack and thus making 3-D stacking of the memory structure possible.

Typical parameters for spin-coated films of CNT-based materials are thickness uniformity, roughness, adhesion, and defectivity. Different from nearly any other spin coated material, CNT coatings consist of high-aspect-ratio structures that are up to several nanometers in diameter and hundreds to thousands of nanometers long. Spin coating produces a fabric, as shown in Fig. 5, with coating thickness nominally of 3.8 nm per pass for 200-mm wafers and 7.5 nm per pass for 300-mm wafers. Reaching the target coating thickness of 30 nm takes 8 and 4 coating passes, respectively. Optimization of CNT fabric thickness is critical. A thinner film reduces both process and material costs and improves electrical performance, while a minimum thickness is needed to prevent shorting between the top and bottom electrodes during metal deposition over the porous CNT fabric.

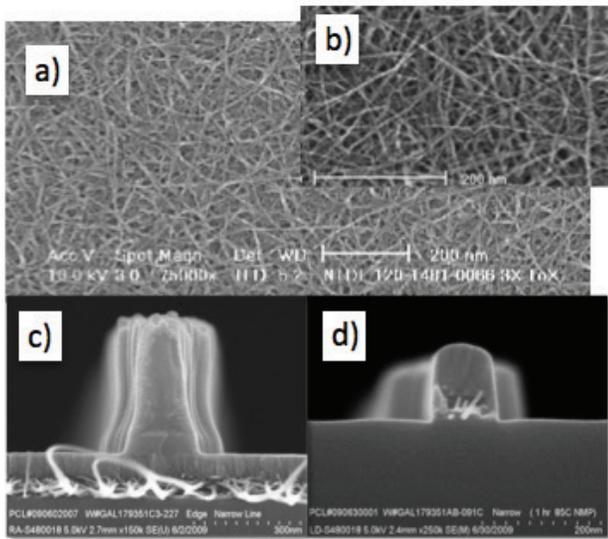


Figure 5. a) and b) CNT coating fabric surface, c) photolithography on CNT/TiN stack, d) after etch and strip.

The coating, edge bead removal (EBR), and backside rinse (BSR) require engineering controls for collection of aqueous waste streams contaminated with CNTs. Under current Environmental Protection Agency rulings, these waste streams must be segregated and collected for appropriate disposal. Currently, this requires incineration or designated hazardous waste disposal sites. Note: The concentration of CNTs in this waste stream is about 5.84 ppm for total of ~120 ml of aqueous waste per coating pass. This is based on 3 ml dispense of CNT solution and 2-mm edge bead plus a total addition of 116 ml of water for pre-wet, EBR, and BSR steps. For a 300-mm wafer, this leaves 3.98 mg of CNTs deposited on the wafer for a 30-nm thick layer.

Once the top metal TiN electrode is applied, traditional BEOL photolithography is conducted to allow etching through both the top metal electrode and subsequently the exposed CNT fabric to produce the memory cells. This

etching is followed by photoresist strip and anneal prior to dielectric deposition (SiN encapsulation) of the memory cells. See Fig. 6 for the simple process flow and stack used to build the CNT memory cell. Fig. 5 shows a CNT memory cell cross section at lithography and etch.

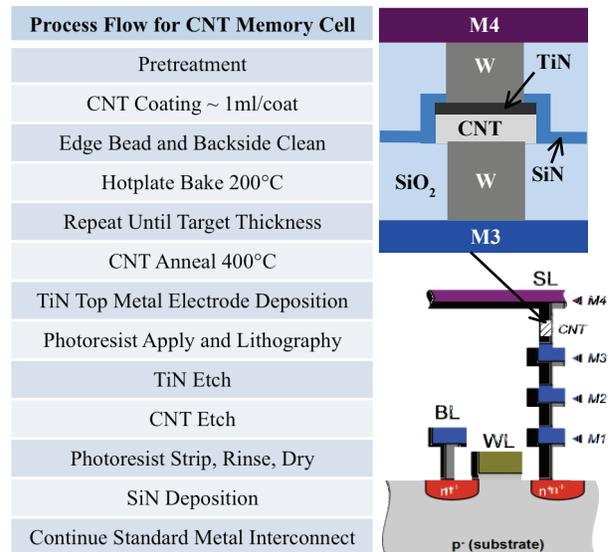


Figure 6. Process flow and CNT memory cell structure and placement within BEOL integration. BL (bit line), WL (word line), SL (source line), and M1-M4 (metal levels).

The chance for CNT exposure to end device users or the environment is minimal once the CNT memory cells are encapsulated. It is incredibly difficult to expose and then tear apart the CNT fabric to free individual nanotubes. It would require multiple etch recipes to remove the surrounding layers. Depending on memory cell density and size, typically less than 1 ng of CNTs is in a single layer of a memory device. See Fig. 7 for the expected CNT mass in a particular device node and memory size. The level of CNT exposure is miniscule at this point and would require deliberate and expensive laboratory or industrial systems to liberate the encapsulated CNTs without destroying them.

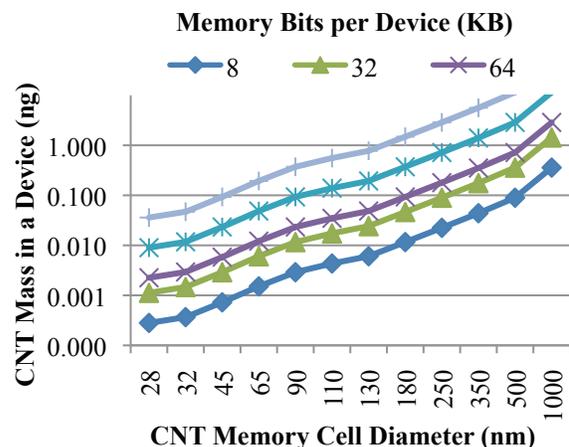


Figure 7. Calculated CNT mass in a memory device.

## 4 CNT RAM ARCHITECTURE

Test chips of a 4-MB CNT RAM device built on 130-nm technology are available from Nantero, Fig 8. Basic cell performance has been reported previously for this device and is summarized in Table I. Fig. 8 shows a cross section of the CNT RAM cell and the switching mechanism. To set the memory cell, 2.5 V is applied to the bit line (connected to bottom metal electrode), while the word source line (connected to the top metal electrode) is held at 0 V. CNTs are pulled down to the bottom electrode, closing many connection paths leading to a low resistance state. To reset the memory cell, a higher voltage (3 V) is applied to the top electrode through the source line, with 0 V at the bottom electrode. CNTs pull away from the bottom electrode, electrically opening many of the pathways leading to high resistance state.

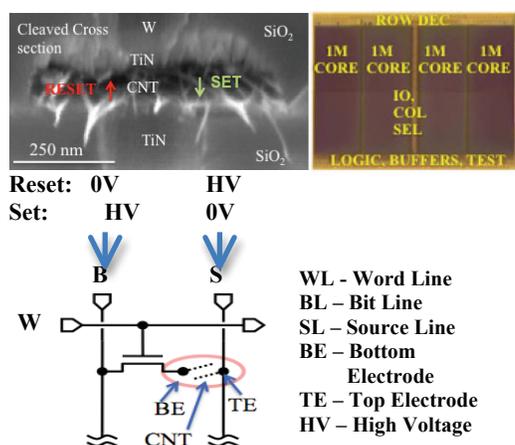


Figure 8. 4-MB CNT RAM device at 130-nm technology.

130-nm 4-MB CNT RAM	Write (-65°C to +165°C)	
	Voltage (at CNT)	Time
Reset	3 V	<3 ns
Set	2.5 V	<3 ns
Window (1V Read)	Typical: >1000x: Off > 100 Mohm / On < 100 kohm	
Endurance	>10 <sup>12</sup> cycles	
Read Disturb	>10 <sup>16</sup> reads: non-destructive	
Retention	>1000 years at 85°C (>10 years at 300°C)	

Table 1. 130-nm 4-MB CNT RAM performance.

## 5 CONCLUSIONS

CNT-enabled RAM memory shows great promise as an alternative memory technology based on device performance, device stack integration, process integration, cost reduction, and the generational material improvements required to be a viable technology. Integration is at BEOL, allowing the memory cell to reside in the metal

interconnects layers instead of requiring space on the active silicon level. Process integration is conducted with traditional equipment and processes, minimizing the need to integrate new types of deposition or processing equipment. The latest generations of spin-applied CNT formulations from Brewer Science, with increased CNT concentration and reduced trace metal contaminants, provide device manufacturers with reduced processing cost due to fewer coatings and reduced material usage per wafer, improving the overall cost for CNT-based memory. These same improvements also reduce CNT waste and potential for exposure impacts.

Future work is focused on migration of the technology to the 28-nm node, requiring optimization of the current and voltage scaling. As a key material provider, work will continue on providing improved CNT formulations to reduce coatings required per layer and coat process times.

## ACKNOWLEDGMENTS

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