

Direct Integration of Ni₂Si/Si Nanograss Heterojunction Array on the Gate Terminal of N-MOSFET Utilizing a CMOS Compatible Top-Down Technique

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ABSTRACT

Herein, we take advantages of direct integration of Ni₂Si/Si nanograss heterojunction array on a MOSFET's gate terminal, utilizing a CMOS compatible top-down technique, to realize a highly sensitive phototransistor. In the proposed technique, using a deep reactive ion etching (D-RIE) process thick poly-silicon (Si) of gate area is converted to array of Si-nanograsses (Si-NGs) through sequential etching/passivation cycles. Afterward, about ~15 nm thin layer of nickel (Ni) was deposited on the surface of Si-nanograsses using an electron beam evaporator. Sample thermal annealing, for nickel-silicide/Si heterojunction formation, and transistor's active area definition were done at 750 °C in argon ambient to directly integrate the prospective heterojunction on the gate terminal. X-ray diffraction (XRD) analysis revealed that only Ni₂Si phase is formed during the annealing process. Also, atomic force microscopy was exploited to investigate uniformity of formed nanostructures all through the array. This technique provides a facile way to accurately control nanostructures' density, height and thickness that would be appealing for technological needs for tuning electrical, optical and mechanical properties of devices based on silicon nanostructures.

Keywords: silicon nanograss, nickel silicide, XRD, direct integration

1 INTRODUCTION

One-dimensional (1D) and quasi one-dimensional nanostructures offer fascinating properties that are not observed in the bulk materials. The use of nanostructures or nanostructured materials represents

a general approach to reduce cost and size as well as improving efficiency in varieties of applications [1-4]. In this framework silicon semiconducting materials have attracted special attentions [1, 3]. Various application ranged from chemical and biological sensors [2-3] to energy conversion and storage devices [4] subscribe to the important role of these materials in the ongoing field of nanotechnology. Furthermore, one of the most studied phenomena in nanostructures is their observable sensitivity to light for photodetection applications. Silicon because of its sensitivity to visible light is of special concern in this field. In these devices photoactive area plays a major role in the detected sensitivity of device. Due to Moor's scaling rule the sensitivity of devices has decreased as most of the die area is taken over by peripheral circuitry and reducing the detecting area. To address the mentioned problem, we introduce direct integration of Ni₂Si/Si nanograss heterojunction array on the gate terminal of a conventional MOSFET as an effective approach for extracting electrical signals from Ni₂Si/Si. In this frame unique features of MOSFET including production of highly controllable electrical signals in one hand and sensitivity of the outpour characteristics of the device to variation of gate electrical field, on the other hand, make this technique eligible for efficient conversion of light to electrical signal. The offered structure has three main features: extreme light absorption, high potential of charge transportation, and large photoactive area. These features are inevitable when one decide to select a material for photovoltaic applications.

2 EXPERIMENTS

2.1 Heterojunctin Formation

An array of Ni-silicide/Si heterojunction has been realized by a multi-step process on N-type silicon

(100) substrates. By means of a reactive ion etching (RIE) system Si-nanograsses are fabricated in an RF plasma (13.56 MHz) environment composed of O_2 , H_2 and SF_6 gasses with sequential etching/passivation cycles. The etching cycle achieved using SF_6 as the inlet gas with a flow of 30 SCCM (standard cubic centimeters) and pressure of 80 mTorr, whereas a mixture of H_2/O_2 gasses with typical value of 100 and 80 SCCM, respectively, with a trace value of SF_6 at pressure of 150 mTorr is used during the passivation cycle. In other words, the passivation cycle is an in-situ mask generation to protect sidewalls of previously formed nanostructures during the etching step. The plasma power is usually set at 130 W and 150 W for the two sub-cycles of etching/passivation with the duration of 10 s and 50 s, respectively. Figure 1 exhibits scanning electron microscope (SEM) images of achieved silicon nanograsses under different conditions. This technique allows an accurate control on nanostructures density, height and thickness that would be appealing for technological needs for tuning electrical, optical and mechanical properties of devices based on silicon nanostructures.

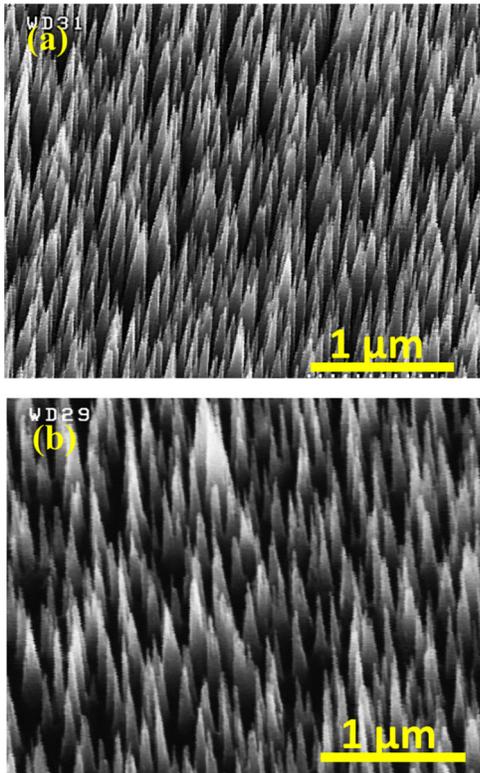


Figure 1: SEM images of array of silicon nanograsses constructed at etching sub-cycle plasma power of (a) 130 W (b) 200 W

Deposition of a thin layer of nickel with an approximate thickness of 15 nm on the surface of Si-nanograsses using an electron beam evaporator is the next step in the construction of the following heterojunction. Afterward, the sample was loaded into an annealing furnace and heated up to 750 °C in argon ambient for 20 minutes. Then the residual nickel on the sample was stripped off with nickel etchant composed of $3C_6H_8O_7: H_2SO_4: 5H_2O$ solution.

2.2 Integration of NG on the Gate Terminal

Wafer cleaning using standard RCA#1 solution is the first step in fabrication of phototransistor. Then sample was inserted into a dry oxide furnace (1100 °C) for the growth of approximately 70 nm silicon dioxide (SiO_2) as the gate dielectric. Subsequently, sample was loaded into a low pressure chemical vapor deposition (LP-CVD) chamber for deposition of a thick layer of polycrystalline silicon (figure 2a). Poly-Si deposition was performed at temperature of 620 °C while silane (SiH_4) serves as silicon agent and hydrogen (H_2) as carrier gas at total pressure of 10 torr. Typical thickness of poly-Si is approximately 800 nm. This silicon layer is exploited to construct Si-nanograss on the gate terminal utilizing the same procedure mentioned above (figure 2b). Indeed, the passivation/etching steps repeated as many cycle as needed to ensure that the whole layer is converted to the desired nanostructures. The SiO_2 layer beneath the poly-Si acts as the etch stop layer in this step. Afterward, a thin layer of nickel was deposited on the surface of the sample and then was patterned to define the gate area by means of standard photolithography processes and Ni etching (figure 2c). Then Si-nanograsses in the surrounding area were etched away by directional SF_6 plasma at pressure of 2.5 torr using RIE machine to assure that nanostructures only exist on the gate terminal (figure 2d). Next step is definition of source, drain and channel regions (figure 2e). After removing oxide layer in the demarcated area through sequential lithography and etching (with buffer HF 10% solution) steps, active regions are determined. Transistor was designed to have channel length and width of 150 μm and 250 μm , respectively. The final step is simultaneous introduction of dopant to the active area and formation of Ni-Silicide at the top of the gate electrode (figure 2f). Both of these events occur in the phosphorous doping furnace at 750 °C in order to add N-type dopants into the active regions and anneal Ni-Si system to form nickel silicide on the gate designated area. At the end of integration

processes, the residue of pristine Ni was etched away. Outline of fabrication steps is depicted in figure 2. SEM image of the obtained heterojunctions on the gate (inset, figure 2f) shows that tip of the nanograsses are a bit round. Thermal annealing at fairly high temperature and dipping in HF solution might cause this phenomenon.

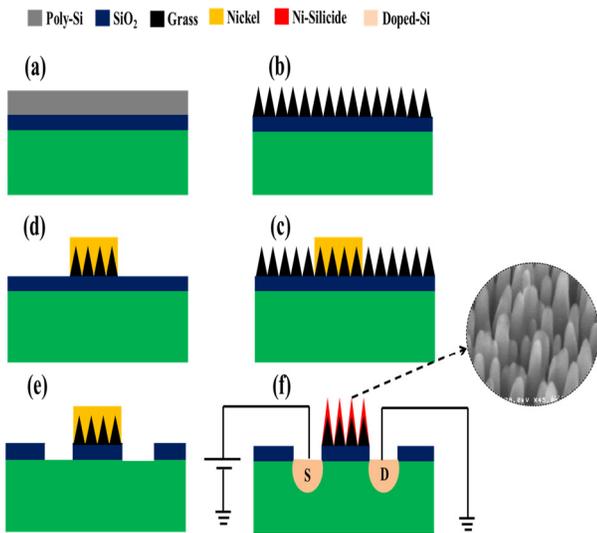


Figure 2: Sequential steps in fabrication of phototransistor. (a) deposition of poly-Si on SiO₂, (b) formation of silicon nanograss using RIE technique, (c) deposition of thin layer of Ni and definition of gate area by photolithography, (d) elimination of Si-nanograsses by SF₆ plasma, (e) oxide removal in source and drain area using buffer HF, (f) simultaneous introduction of dopant to the active area and thermal annealing of Ni-Si system to form Ni₂Si heterojunction.

3 RESULTS AND DISCUSSION

X-ray diffraction (XRD) pattern of the array of heterojunctions is shown in figure 3. Sample was characterized using Philips XPERT PRO system with Cu K_α (λ=0.154060 nm) radiation to identify Ni-silicide phases present. Observed peaks located at 2θ°= 32.48, 42.38 and 48.76 reveal that among most probable stable phases (Ni₂Si, NiSi and NiSi₂) [12] annealing of our Ni-Si binary system at 750 °C concludes formation of Ni₂Si phase. It should be kept in mind that Ni₂Si is the first stable phase form therefor the only phase detected in the XRD spectra is Ni₂Si. The intense peak located at 2θ°= 69.7 is the intrinsic characteristics of silicon substrate.

To investigate geometrical uniformity of as prepared nanograsses all through the array, we performed atomic force microscopy (AFM) analysis on a representative sample.

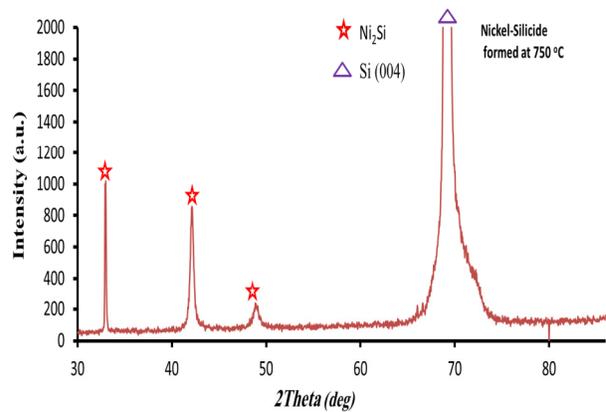


Figure 3: XRD spectra of Ni₂Si/Si heterojunction. The observed peaks correspond to Ni₂Si (marked with red stars) shows construction of nickel silicide. The sharp peak at 2θ=69.7 is due to the crystalline silicon substrate (Si (004)).

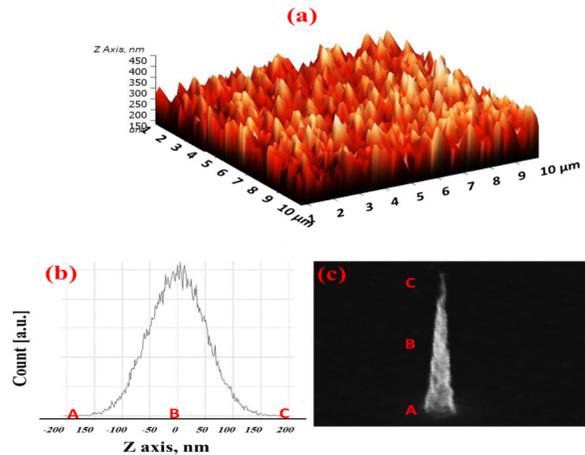


Figure 4: (a) Atomic force microscope image of etched silicon nanograsses, in an array of 10×10 μm². (b) Height histogram, (c) SEM image of a single Si-nanograss. Capital letters (A, B and C) presented to provide a correspondence between Figures 4b and 4c for the sake of comparison.

Three dimensional height profile of the sample and its corresponding height histogram are illustrated in in Figure 4a and 4b, respectively. Resemblance of the sample height histogram and geometry of an individual Si-nanograss implicitly points to the fair uniformity of the constructed structures all through the array. The available uniformity along with precise

control on the density, height and thickness of these nanostructures would be appealing for technological needs for tuning electrical, optical and mechanical properties of devices based on silicon nanostructures.

The optical absorption spectra of an array of heterojunction/SiO₂/Si is presented in figure 5a. This sample absorbs more than 98 % of the incident light with wavelengths around $\lambda=655$ nm. Indeed, effects arising from the low dimensionality including enhanced light scattering, waveguiding effects (light funneling), and larger surface to volume ratio boost optical absorption of the sample decorated with nanostructures

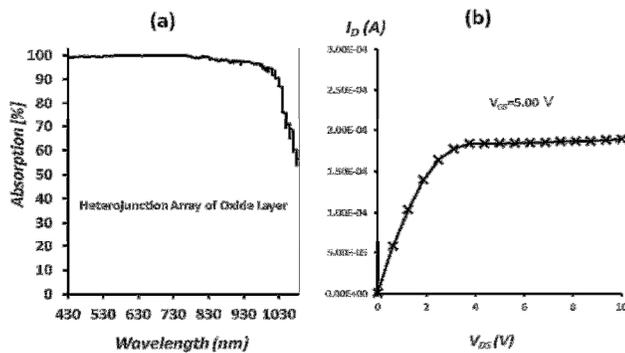


Figure 5: (a) Optical absorption spectra. (b) A typical I_D - V_D curve

Figure 5b shows a typical I_D - V_D curve for the fabricated transistor exhibit classical linear/saturation behavior and justifies that the proposed method leads to realization of reliable transistor which its gate is decorated with nickel silicide/si heterojunction array and is appropriate to be used in photovoltaic applications.

4 CONCLUSION

First, formation of Ni₂Si/Si heterojunction array utilizing two separated process including deep reactive and ion etching of polysilicon and its thermal annealing at 750 oC was presented. Second, direct integration of this heterostructure on the gate terminal of conventional MOSFET was introduced. Based on the observed optical absorption as well as high electrical conductivity of silicide species this device would be a promising candidate for photodetection applications.

References

- [1] M. Taghinejad, H. Taghinejad, M. Abdolahad, and S. Mohajerzadeh, "A nickel-gold bilayer catalyst engineering technique for self-assembled growth of highly ordered silicon nanotubes (SiNT).," *Nano letters*, vol. 13, no. 3, pp. 889–97, Mar. 2013.
- [2] M. Abdolahad, M. Taghinejad, H. Taghinejad, M. Janmaleki S. Mohajerzadeh, *Lab Chip*, 2012, 12, 1183–1190.
- [3] H. Taghinejad, M. Taghinejad, M. Abdolahad, a. Saeidi, and S. Mohajerzadeh, "Fabrication and modeling of high sensitivity humidity sensors based on doped silicon nanowires," *Sensors and Actuators B: Chemical*, vol. 176, pp. 413–419, Jan. 2013.
- [4] W. Wang and P. N. Kumata "Nanostructured Hybrid Silicon / Carbon Nanotube heterostructures: Reversible High-Capacity Lithium-Ion Anodes," vol. 4, no. 4, pp. 2233–2241, 2010.