Smart System Design in Context of Multicriteria Optimization based on Accelerated Ageing Techniques for IC Interconnect Structures

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ABSTRACT

Practical experience from several European R&D projects led authors of this paper to focus on interconnects reliability. Interconnect reliability is considered in reliability estimation context, its application for SiP cost modeling used for smart system design optimization. Above mentioned experience comes from successfully concluded e-CUBES [14], e-BRAINS[15], SE2A [18] and CORONA [19] projects contributing research activities on 3D systems integration and development of design methods. There are also on-going projects like SMAC [17] focused on 3D and smart systems design and PARSIMO [16] contributing development of optimization methods and tools for SiP partitioning. Development of IC fabrication technology is followed by advancements in device assembly and packaging. Reliability issues lead the designers to take into consideration layout, material and properties of interconnects. Clock distribution issues like signal integrity, clock skew and applied solutions like optimized clock tree and interconnect reliability led researchers to focus on 3D integration-related specific issue of interconnect reliability and methods to make it predictable and to keep under control.

Keywords: accelerated ageing, ATMA, MEMS cantilever beam, interconnect reliability, SiP, e-BRAINS, PARSIMO, SMAC, smart system, cost modeling, design optimization.

1 INTRODUCTION

First part of this paper refers to the general problem of investigation on reliability of interconnects implemented as wired connections bonded to contact pads on bare chip dies or by planar metal paths deposited in particular layers of an integrated circuit. Investigation on reliability has been funded by research activities performed in frame of e-BRAINS project which was successfully concluded in February'14. Second part of this paper addresses practical application of research results on reliability modeling for optimization of SiP design in context of cost modeling. It is a key issue of SiP design optimization being developed in frame of on-going PARSIMO project. Interconnects reliability model is being incorporated among other design parameters for cost model of the SiP. Development of design tools applicable for smart systems co-design like MEMS+ by Coventor is practically addressed by ITE, Coventor et.al project partners in frame of SMAC project activities. Interconnect reliability modeling outcome applied for design practice on a sample design of microphone application will be presented in the third part of this paper. The description covers development of MEMS sensing module to be integrated with a dedicated readout and communication modules which undergo excessive co-simulation to address specific issues of the MEMS-ASIC co-design process.

2 ACCELERATED AGEING

Complex chips and novel smart nanosensor systems are developed as 3D structures like SiP or SoC. incorporating several modules and materials forming 3D setup. It can no longer be considered as a pure electrical system, but as a complex, micro-electro-mechanical system with strong thermal feedback introducing mechanical stress and affecting device reliability. Reliability issues to be considered during design process cover various types of defects: scratches, displacements, delamination, fractures, fatigue cracking, void formation etc. The research is ongoing and applies to heterogeneous device structures like SiP, SoC where mechanical stress caused by thermal cycling, heat dissipation, assembly technique etc. distributes inside thin layers of metal interconnects [8]-[12].

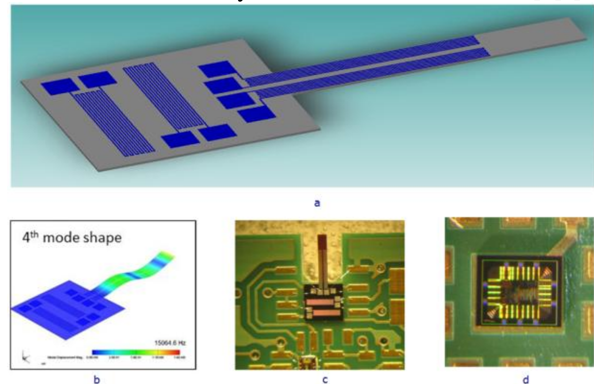

Figure 1. AABS structure: a) CoventorWare design with 4 interconnect strips, b) mechanically excited for vibration, c)assembled on PCB, d) with a dedicated readout ASIC chip.

Modular simulations using PDE solvers and high level model generation for system level simulation [5]-[11] is one of several approaches available. Dedicated silicon cantilever micro-beam structures (AABS – Accelerated Ageing Beam Structures) with metal interconnects on the top of the beam (Figure 1) are dedicated for accelerated thermo-mechanical ageing process (ATMA – Accelerated Thermo-Mechanical Ageing) and have been fabricated in ITE [11]. Several research methods [1]-[[7] are focused on interconnect reliability and are applicable to various types of interconnects (paths, solder balls, TSVs, microbombs), various domains (DC, RF) and materials. Tested interconnection structures have been developed with alumina exposed to periodic deformation hazard imposed by mechanical vibration of the microcantilever (Figure 2).

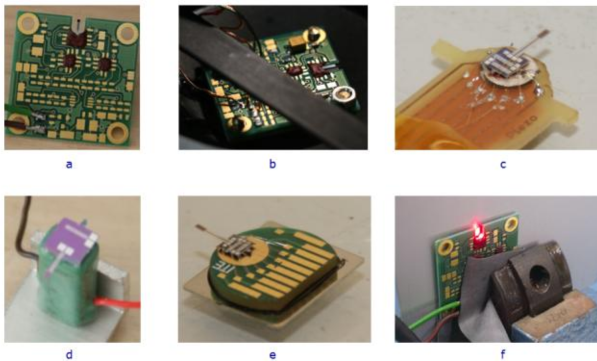

Figure 2. ATMA measurement unit with ASIC on-board (a), and a system setup ready (b). Cantilever beam on piezzo drive (c), and on a piezzostack (d). ATMA system for investigation on bound ageing (e), thermal investigation on measurement setup (f).

Thermal cycling stimulates mechanical stress and deformation of the interconnect (Figure 5). Such a physical feedback results in mechanical stress distribution across the IC structure. The internal, mechanical stress is also caused by assembly technique (wire bonds), materials applied (silicon substrate with aluminium/copper/gold/other interconnects), and device structure affecting distribution of the embedded stress. The most interesting from ATMA research point of view is a mechanical stress distribution within the thin layer of interconnect and stress influence on electrical parameters of interconnects [12]-[13] investigated in short and long-term scale. Interconnect ageing is considered in context of material degradation. In order to strengthen ageing results and make it better detectable, the design has been optimized by application of multi-bend meander geometry of conducting strips. They are placed in the beam region where peak values of the mechanical stress stimulated by external excitation occour (Figure 2a-e).

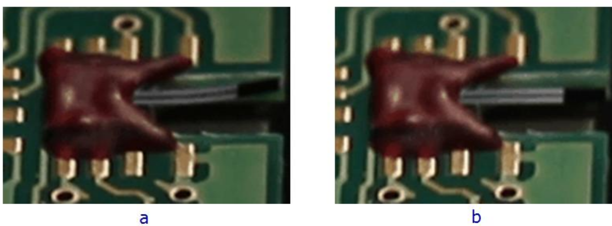

Figure 3. ATMA measurement. AABS bending driven by cantilever temperature: a) T=90C, b) T=25C

AABS modules with cantilever beams have been optimized for several resonant frequencies covering the range of 100Hz-100kHz to address specific requirements for an accelerated thermo-mechanical fatigue of interconnecting material. AABS have been designed, optimized and fabricated for e-BRAINS project in ITE. It was agreed to setup oscillation amplitude sufficient to lead the deposited film of the interconnecting material into the range of plastic deformation. Design optimization iterative works resulted in fixed 4mm length of cantilever, 700µm width and 8µm thickness. The first harmonic mode is located below 2kHz. Metal lines have been formed on the silicon substrate covered by silicon dioxide (SiO_2,) characterized by 100Å thickness. Thickness of metal layer is 1.2µm. The fabricated MEMS structure with cantilever beams and thin-film interconnects has metal strips 10µm width, 50Ω resistance. Laser interferometer measurements by Polytec MSA-500 Micro System Analyzer (Figure 2e) confirmed resonant frequency, coherent with the expected ressonant characteristic predicted. MEMS-based cantilever beam with double metal lines under mechanical-vibration ageing tests lasting 72 hours under mechanical vibration in 2nd resonant mode revealed ±0.25% deviation resistance, but excitation amplitude is too small to lead interconnecting material into plastic deformation region. Manual bending exceeding 2mm relocation of the cantilever tip resulted in ±1.20% reversible change of the resitance. Experiment is ongoing.

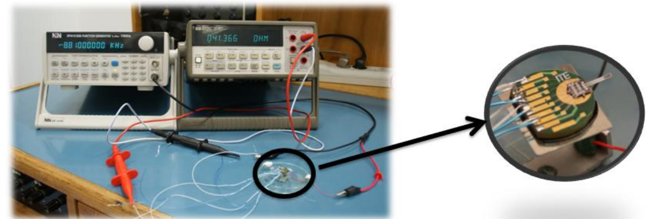

Figure 4. ATMA measurement system running. MEMS-based test structure on piezo-drive mini-shaker under ageing tests

3 COST MODELING

Partitioning and modeling of SIP are key issues with special attention paid on multi-criteria SiP optimization performed on various levels of abstraction: from the design flow, through performance modeling to the design "cost" modeling, estimation and optimization. It is essential to point out, that the "cost" in SiP design context has several meanings from design effort, through compatibility of technologies intended for integration in a form of SiP structure, various performance metrics, module accessibility and a lot of other aspects possible to be included in conditioning, but addressable by the designers in the future or in for specific SiP design process constrains and requirements. The research is ongoing and applies to heterogeneous device structures like SiP, SoC where mechanical stress caused by thermal cycling, heat dissipation, assembly technique etc. distributes inside thin layers of metal interconnects. Several approaches have been presented on functional aspects as well as the influence of integration technology on the system behavior in context of the 3D integration design process of micro systems. The "cost" optimization can be considered on at least two levels of abstraction: individual modules/blocks like MEMS sensors, readout circuitry, data processing units, radio-communication units, amplifiers, antennas, substrates etc. and technologies/solutions like integration, encapsulation where mechanical properties and interconnect reliability plays important role. Whole the novelty being developed in frame of PARSIMO project leads the designers and design-house customers to less complex, and faster design process resulting in reduced time to market, as well as cheaper and more reliable final product.

There is a SIESTA: "System of Intelligent Sensors for Experimental Avionic Applications" among four

PARSIMO project demonstrators. It is developed by ITE and Wroclaw University of Technology in close cooperation with Coventor and Silvaco companies. The PARSIMO-based toolset is devoted to assist designer on how to proceed with system optimization.

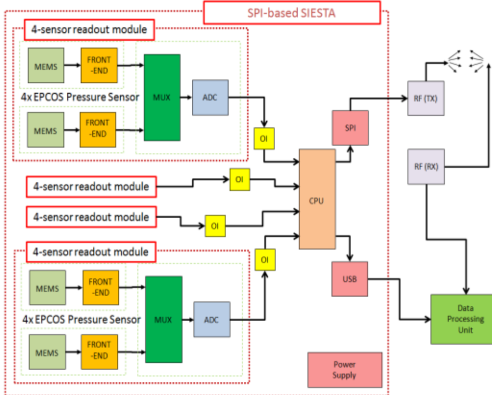

Figure 5. SIESTA structure as a result of optimization process driven by cost model.

Intermediate result of system optimization (initially performed manually) has been presented on Figure 5. System partitioning and optimization is based on the specification, availability of modules, IP's blocks, technologies, integration techniques and more. The profit is that better solutions will be achievable in a reduced time. Whole the knowledge related to the particular device block (the physical SiP component), functional module or a block is now being collected in the dedicated database

[*13*]. Power supply parameters, power consumption, interconnect reliability, bandwidth, physical extent, model availability, parameterization features, hardware availability in bare-chip layout, integrability and many more also definable in the future. All cost factors undergo the normalization process. Each cost factor has its specific weight assigned to reflect its importance in overall design.

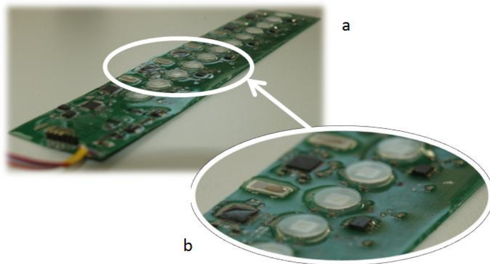

Figure 6. SIESTA demonstrator with encapsulated pressure sensors: a) overview of the system, b) focus on on-board electronics protected by elastic resin.

For example if it is more important to reduce device power budget, have a fast circuit or use less expensive fabrication/integration technology. It is currently being implemented for Parsimo weighted objective method (WOM) for multi-criteria optimization of target solution.

$$F(x) = \sum_{i=1}^{k} w_i f_i(x)$$

where k is number of cost functions $f_i(x)$, w_i is normalized weight factor and x cost factor vector composed from normalized parameter values. Novel optimization methods have been applied to development processes in frame of PARSIMO project. The SIESTA system developed as a project test-bed (Figure 6). It addresses the problem of detection of a transition between laminar and turbulent airflow conditions in close surrounding of an aircraft wing or rotor blade. The design optimization process driven by WOM effectively reflects several device specification and fabrication aspects like flexibility of substrate affecting its performance, reliability and price.

4 SMART SYSTEMS CO-DESIGN

Smart-system heterogeneous design should be performed in parallel by electro-mechanical co-simulation. The old fashioned approach profits from manual generation of Verilog-A physical model of the MEMS structure co-simulated in Cadence with readout electronics The novel approach Figure 7 being developed in frame of SMAC project relies on a MEMS model developed in MEMS+ software [12] supporting automated generation of full component for Cadence representing MEMS module for effective co-simulation.

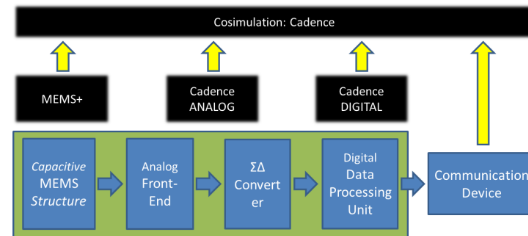

Figure 7. System development scenario in SMAC

There is also a challenging attempt made by ITE to join effors undertaken in frame of PARSIMO project to enrich smart system development with cost-modelling issues useful for 3D integration. It would profit for a microphone system being developed by ITE in frame of SMAC project. There are several application-dependent physical constrains and design challenges like interconnect reliability, linearity of MEMS characteristics, thermal stability of the mechanical structure affecting microphone dynamics, and more. Mechanical simulations and design optimization steps performed for the case of microphone being developed cover creation of the simplified microphone model using CoventorWare™ environment to find resonant frequencies, and stress/strain distribution under accoustic wave pressure imposed. After that microphone model simulations using Coventor MEMS+™ environment have been undertaken using initial simultion results achieved using CoventorWare™: 2µm thick, 1000x1000µm membrane, was selected for further modeling. Mentioned simulation results have been coherent with theoretical analysis, however some drawbacks have been faced like long simulation time, hard or even impossible integration of mechanical model with electronic model for co-simulation purposes, parameterization hard to handle with. Each

change of the material or geometrical parameters required subsequent, time consuming remeshing and recalculation of the model. Further analyses have been proceeded using Coventor MEMS+™ software capable to fill the co-simulation gap related to efficient optimization of the MEMS device model and full system co-simulation assured by Coventor MEMS+™ and Cadence.

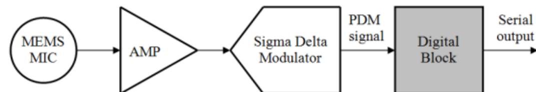

Figure 8. System diagram of the microphone developed by ITE in SMAC

5 CONCLUSIONS

This paper presented methodology of investigation for accelerated ageing of thin metallization layers commonly met in 3D heterogeneous structures prone to thermo-mechanical cycling which stimulates thermo-mechanical generation of mechanical stress and interconnect ageing. Methodology of ATMA measurements results reasoning is under development. All components have been successfully developed and undergo ageing procedure. Results are stimulating subsequent research on design optimization and lead autors for real improvements of the smart system development applied in practice across european research projects. This paper also addressed sample design scenario based on a development of SIESTA system with discussion of multicriteria optimization aspects like cost modeling reflecting not only device performance, but considering optimization as flexible process. Wide range of tools applied for system design, optimization and validation was presented and discussed on a real application samples.

6 REFERENCES

[1] M.Krüger, T.Eckert, N.F.Nissen, H.Reichl: "*Non-Destructive Electrical Measurement of Interconnect Degradation in Early States by the Use of RF Signals*", Proc. of 11'th Electronics Packaging Technology Conference.

[2] D.Kwon, M.H.Azarian, M.G.Pecht: "*Early Detection of Interconnect Degradation Using RF Impedance and SPRT*", Proceedings of 2008 International Conference on Prognostics and Health Management

[3] D.Kwon, M.H.Azarian, M.G.Pecht: "*Early Detection of Interconnect Degradation by Continuous Monitoring of RF Impedance*", IEEE Transactions on Volume:9 , Issue: 2

[4] R.Keller, R.Geiss, N.Barbosa, A.Slifka, D.Read: "*Strain-Induced Grain Growth during Rapid Thermal Cycling of Aluminum Interconnects*" Metal. Mater. Trans. 38A, 2263-2272 (2007).

[5] N.Barbarosa, R.Keller, D.Read, R.Geiss, and R.Vinci: "*Comparison of Electrical and Microtensile Evaluations of Mechanical Properties of an Aluminum Film*", The Minerals, Metals & Materials Society and ASM International 2007, VOL 38A, Sept. 2007.

[6] M.Strus, A.Chiaramonti, Y.Kim, Y.Jung, R.Keller: "Accelerated reliability testing of highly aligned single-walled carbon nanotube networks subjected to DC electrical stressing" Nanotechnology 22

[7] "Engineering Materials Vols. 345-346 (2007) pp 1115-1120, http://www.scientific.net

[8] G.Janczyk, T.Bieniek, J.Szynka, P.Grabiec: "*Reliability Aspects of 3D-Oriented Heterogeneous Device Related to Stress Sensitivity of MOS* Transistors", Proceedings of the IEEE International 3D Systems Conference 2009, San Francisco, USA, 28-30.09.2009, CD 2009, pp. 1-6.

[9] C.M.Sotomayor Torres, J.Ahopelto, A.Cappy, G.Fagas, P.Grabiec, M.W.M.Graef, G.Larrieu, R.Popp, W.Rosenstiel, T.Swahn, G.Wendin, D.Winkler, "*Recommendations on Beyond CMOS Nanoelectronics Research*", 2013

[10] G.Janczyk, T.Bieniek, P.Grabiec, J.Szynka, S.Kalicinski, P.Janus: "*Micro and Nano Device Reliability Control by MOS Transistors Mechanical Stress Sensitivity Estimation and Flexible, Customer Oriented Product Engineering Flow*", IRW 2010 IEEE International Integrated Reliability Workshop

[11] G.Janczyk, T.Bieniek, J.Wąsowski, P.Grabiec "*Investigation on Reliability of Interconnects in 3D Heterogeneous Systems by Ageing Beam Resonance Method*", TechConnect World Nanotech 2013

[12] G.Janczyk, T.Bieniek: "*Nanolayer Interconnect Structures Ageing by Beam Resonance Method*" Nanotech 2013 Vol. 2, Nanotechnology 2013: Electronics, Devices, Fabrication, MEMS, Fluidics and Computational (Volume 2), Chapter 3: MEMS & NEMS Devices & Applications,

[13] T.Bieniek, G.Janczyk, P.Janus, P.Grabiec, G.Wielgoszewski, T.Gotszalk, M.Moczała, E.Buitrago, A.Ionescu, M.Bolaños Badia: "*Reliability Investigation by Examination of dedicated MEMS/ASIC and NW's Test Structures related to novel 3D SiP and Nano-Sensors Systems*", Third IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits 3D-TEST,

[14] e-CUBES Project: www.e-cubes.org

[15] e-BRAINS Project, www.e-brains.org

[16] PARSIMO Project, eeepro.shef.ac.uk/parsimo

[17] SMAC Project, www.fp7-smac.org

[18] SE2A Project: www.eniac-se2a.com

[19] CORONA Project: www.corona-mnt.eu

7 ACKNOWLEDGEMENTS

This work profits from excellent project collaboration and is partially supported by the European Commission under European projects: e-BRAINS (Best Reliable Ambient Intelligent Nanosensor Systems by Heterogeneous Integration), PARSIMO (Partitioning and Modeling of SIP) and SMAC (Smart System CoDesign).