Ultra-Low Power Node for Body Sensor Network

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ABSTRACT

Body sensor network is an emerging paradigm in which the sensor nodes monitor the patient data (as blood pressure, diabetes) and alarm the patient/doctor in case of emergency. The sensor nodes must be ultra-low power since they are powered by harvested energy. In addition, they should have some encryption technique to protect the patient and the privacy of his data. In this paper, we study the use of asynchronous circuits to implement ultra-low power body sensor-node, which is secure against hardware attacks. The simulations showed very good results compared to the synchronous counterpart design.

***Keywords*:** body sensor-network, asynchronous circuits, hardware attacks, ultra-low power

1. Introduction

Medical electronics, especially implanted devices, are operated in harsh and unstable operating conditions. Temperature variations and physical stresses are common circumstances in which these systems must operate correctly. Medical electronics are usually powered using batteries and/or energy harvesters. This implies two important facts, they must be ultra-low power; and they must cope with supply voltage variations. Biosignals are usually band limited; and they are sparse in time domain. As a result, using uniform sampling for biosignals acquisition is costly and inefficient. Non-uniform sampling which is based on level crossing techniques is much efficient to be used in biomedical circuits [1].

In the emerging concept of "Body Sensor network", there are several sensors which are implanted in the body and communicate among each other and with the external world. There is a growing demand to secure the whole network against different attacks to guarantee the patient security and privacy [2].

Based on the above discussion, the hardware technology used to implement body sensor-network nodes must have the following characteristics: Ultra-low power, robustness against variations in the operating conditions, suitability for non-uniform sampling, and immunity to security attacks.

In this paper, a design of an ultra-low power body sensor-node is proposed; it is based on asynchronous circuits, which efficiently satisfies the required characteristics discussed above.

2. Background

Figure.1 depicts the basic view of a pipeline this is implemented in synchronous and asynchronous design styles. In synchronous design style, shown in Figure.1 (a), circuit functionality is implemented by combinational function blocks. Synchronous registers are sampling the output of these blocks. A global clock signal is controlling the sampling time of the registers. The clock period is fixed so that all function blocks correctly complete their operations and their data outputs are stable and ready to be sampled. That implies a global timing assumption, which is applied to the whole circuit. In 40 nm and beyond, uncertainty about the delay is drastically increased. That makes the global timing assumption of the clock is costly from performance point of view as more and more pessimism is added to compensate the delay uncertainty. In addition to this, clock trees in recent chips are huge and power hungry since they have transitions regardless the circuit is computing or not. Consequently, designing a chip with no clock could enhance the speed and the power consumption.

3. The Proposed Design

In asynchronous circuit as the one appears in Figure.1 (b), asynchronous registers have a local handshaking protocol which synchronizing the register with preceding and following registers. By means of this local handshaking protocol, the register informs the preceding stage that the input data is latched and preceding stage can process a new data (Input Acknowledgment). In addition, the stage register uses the handshaking protocol to inform the following stage that a new data is ready to be memorized (Output

Request). This localization of the circuit synchronization avoids problems caused by the generic timing assumption presented by the clock in synchronous circuit style. Asynchronous circuits can be classified based on their architecture style, timing assumptions or their handshaking protocol [3]. There are different architecture styles for realizing asynchronous circuit; the main two styles are shown in Figure.2.

Asynchronous circuits can be implemented as Bundled data Figure.2 (a). In these circuits there are two paths: the data path and the control path. In the data path, data are single rail and function blocks are normal combinational logic. The control path contains the Request and Acknowledge signals for implementing the handshaking protocol. To maintain correct behavior, matching delays have to be inserted in the request signal paths to compensate the propagation delays of the data path function blocks. In this way, there are many local timing assumptions inside the circuit instead of a single timing assumption as in the case of clocked circuits. Indeed this enhances the circuit performance as it reduces the pessimism. The second asynchronous circuit style is called 1-of-n coding style; appears in Figure.2 (b). In this style requests are encoded with the data which implies more complex function blocks as they should be hazard free circuits. Comparing the two styles, the main difference is replacement of the matching delay, Figure.2 (a), by encoded data path, Figure.2 (b). In 1-of-n style, there are no timing assumptions on the function blocks.

Including timing assumptions in the design makes it sensitive to delay variability. Any violation of the Clock timing assumption certainly causes a circuit failure. Localizing timing assumptions, as in Bundled data, or completely avoiding them, as in QDI, makes asynchronous circuits very robust against timing variability caused by PVT deviations. For example in QDI circuits, once the Isochronic Fork condition is satisfied, the circuit can cope any change of the circuit delay. The hazard free encoded data can be detected despite their propagation delay.

Clock trees are quit large especially in recent SOCs. Due to continuous high-frequency switching, they are consuming a considerable amount of the total power consumption of the chip. By removing the clock tree in asynchronous circuits, total power consumption is significantly reduced. Data flow in asynchronous circuits is based on local handshaking, which makes them data driven circuits in their nature. In this case, circuits tend to consume only the necessary dynamic power. Due to their robustness against supply voltage change, power consumption in asynchronous circuits can be efficiently optimized using Dynamic Voltage Scaling “DVS” techniques [6].

In addition to their interesting power consumption, asynchronous circuits have very interesting power distribution (equivalently current distribution). Synchronous circuits generate radio frequency interference at the clock frequency. Figure.4 shows a comparison between the current spectrum in synchronous and asynchronous FIR filter. In synchronous circuits, the clock synchronizes the circuit events. This means that all the circuit components start processing at the active edge of the clock which concentrates the current consumption near this edge. In the contrary, asynchronous circuits are locally synchronizing events. This distributes the total circuit activity in time. This behavior of asynchronous circuits gives them a better current shaping (equivalently better EMI characteristics). In [5] the authors successfully showed how asynchronous handshaking protocol could be used for shaping the current consumption.

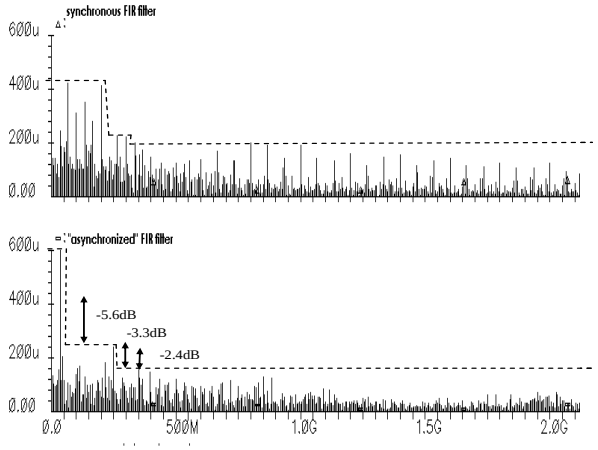

Figure 4: Comparing Current Spectrum of Asynchronous and Synchronous FIR Filter

Because they are data driven, asynchronous circuits have timely distributed power consumption profile. This reduces the EMI and makes the design more secure against hardware attacks as Deferential Power Attack (DPA). Biosignals are usually band limited; sample them uniformly generates unnecessary samples, which waste power in their sampling and processing. Non-uniform sampling (level-crossing) is a proven technique to sample such signals [4]. Asynchronous circuits can be used to efficiently implement non-uniform sampling.

Body sensor-network has different sensors which measure different metrics and transmit them outside the body, as shown in Figure.3. The proposed design is an implementation of body sensor node using Quasi Delay Insensitive logic (QDI) [3]. The system level design is shown in Figure. 5.

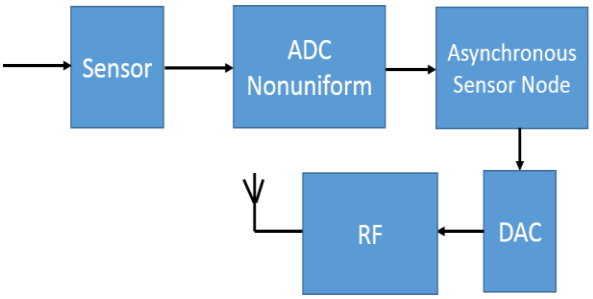

Figure 5: System level of the proposed body sensor-node. This paper focuses on the digital design of the sensor node

The implementation of the proposed node is realized using 65 nm technology and compared to synchronous counterparts (on simulation level). The design implements simple function that compares the blood pressure readings, sampled from the user, with normal reference values. The node invokes an alarm signal that is supposed to be transmitted to warn the patient that his blood pressure is high. The incoming/outgoing data is encrypted to protect the patient security and privacy. The Advanced Encryption Standard is used for the encryption. A complete 128 asynchronous crypto processor is implemented to handle the data encryption.

The simulation results show interesting enhancements in power consumption in both the sensor node and crypto processor. In addition, the asynchronous implementation works correctly on very low supply levels, which reduce the total power consumption by enabling very efficient DVS.

4. References

[1] Yongjia Li; Wouter A. Serdijn "A Continuous-Time Level-Crossing ADC with 1-Bit DAC and 3-Input Comparator". Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), 2012.

[2] Heydt-Benjamin, T.S. ; Ransford, B. ; Clark, S.S. ; Defend, B. ; Morgan, W. ; Fu, K. ; Kohno, T. ; Maisel, W.H. "Pacemakers and Implantable Cardiac Defibrillators: Software Radio Attacks and Zero-Power Defenses". IEEE Symposium on security and Privacy, 2008.

[3] Jens SparsØ, Steve Furber: Principles of Asynchronous Circuit Design. A System Perspective. Kluwer Academic Publishers (2001).

[4] Zhang X., Willett P., Bar-Shalom Y. "Uniform versus nonuniform sampling when tracking in clutter". IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS VOL. 42, NO. 2 APRIL 2006

[5] Eslam Yahya, Marc Renaudin and Gregory Lopin: "Standard-Logic Quasi Delay Insensitive Registers".VLSI-SOC'08 pp:465- 468

[6] Mohammed Es Salhiene , Laurent Fesquet and Marc Renaudin: "Dynamic Voltage Scheduling for Real Time Asynchronous Systems", PATMOS 2002, pp. 390-399.

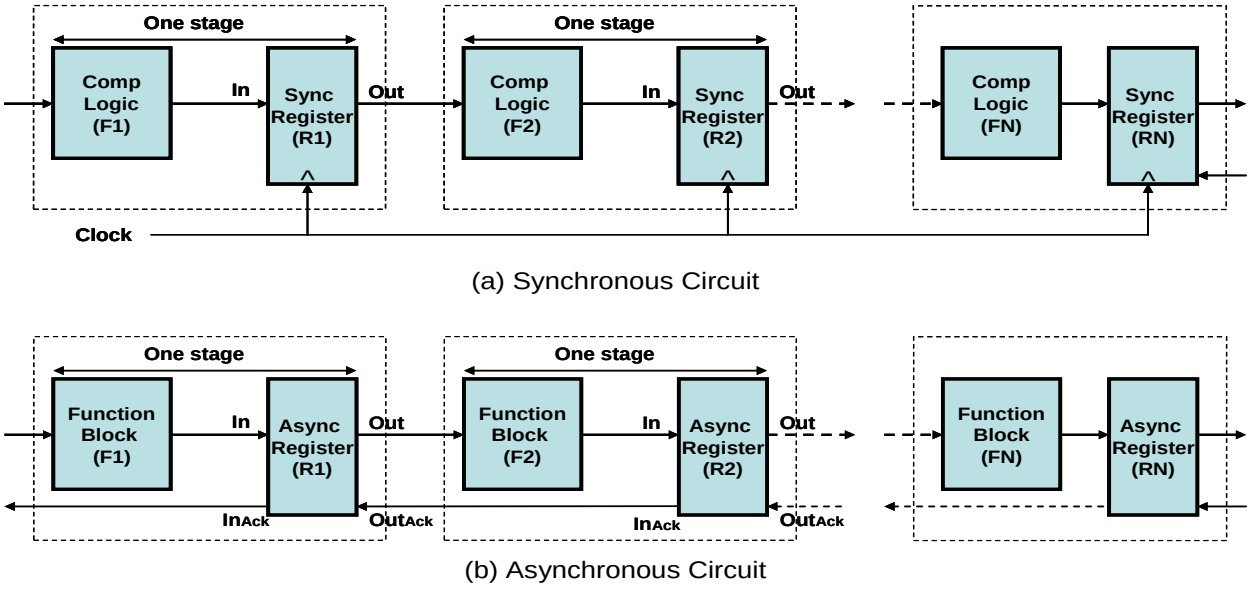

Figure 1: Comparison between the basic architecture of synchronous and asynchronous circuits. Data flow in asynchronous circuit is based on local handshaking between the adjacent blocks. The global clock is avoided which gives asynchronous style lower power and interesting EMI characteristics.

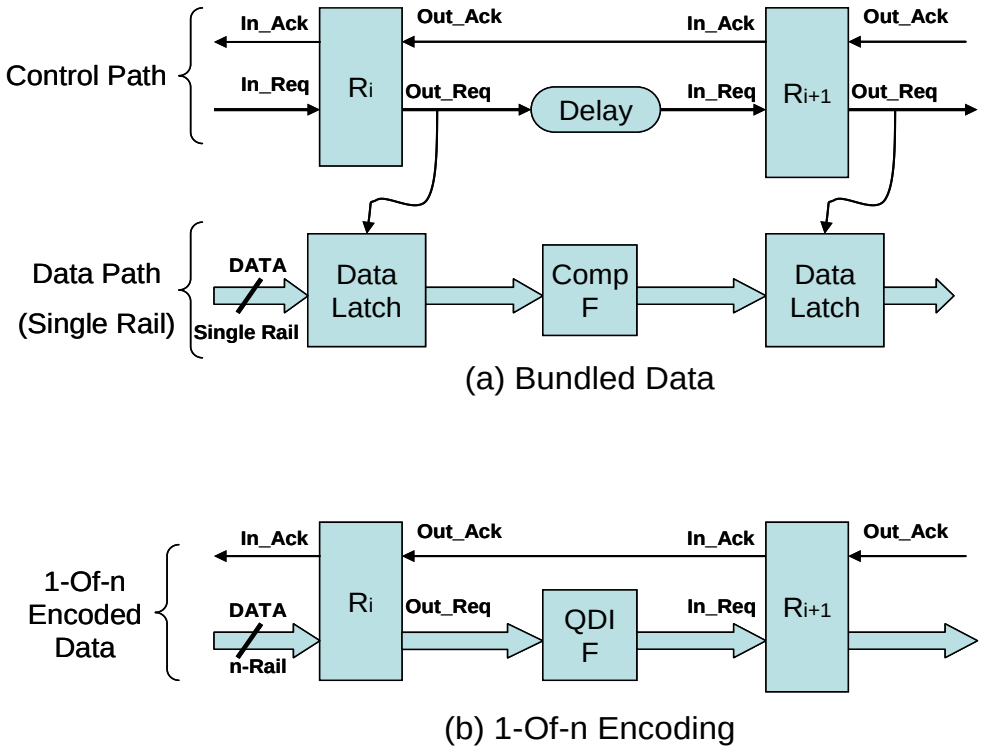

Figure 2: Asynchronous Circuit Styles. a) Bundled Data b) 1-of-n Encoding

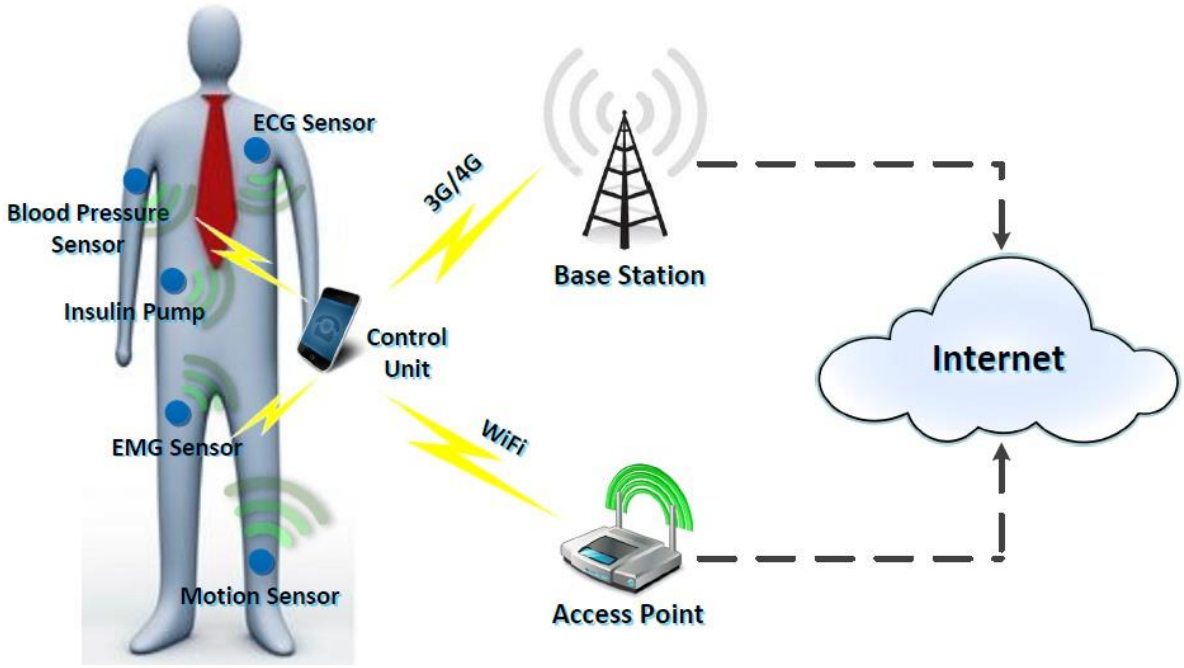

Figure 3: An example of body wireless network. The sensor nodes are required to capture the patient data by using nonuniform ADC and process with very limited power budget. The data then is sent to outside the body to be stored, monitored, and/or analyzed by health specialists.