RF-noise Modeling in MOSFETs: Excess Noise, Symmetry, and Causality

(Invited)

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ABSTRACT

We present new RF-noise measurement data from a commercial 40nm-technology, thereby reconfirming the accuracy and universality of our excess noise model (published in Ref. [1, 2]). In addition, we discuss symmetry and causality requirements for noise models, in order to be compliant with advanced noise analysis methodologies in today's circuit simulators. We present a generic method that can be applied to SPICE models in order to facilitate meeting these requirements.

Keywords: RF noise, SPICE model, PSP model, symmetry

1 Introduction

Modeling of RF-noise in MOSFET channels is a cornerstone of RF-CMOS-circuit design. Deep sub-micron technology nodes necessitate a proper treatment of excess noise [1] as well as detailed modeling of parasitics. In addition, demanding circuit applications require advanced noise analysis methods (such as time-domain noise simulations). All of these put increasingly high requirements on SPICE models.

In this paper, we present a new 40-nm measurement data set that reconfirms the accuracy and universality of our previously published noise model [1, 2]. Moreover, we show a generally applicable method to implement RF-noise models in a circuit simulator, which is consistent with symmetry and causality requirements for advanced noise analysis methods.

2 Excess noise

In our previous work [3–5], we have extensively demonstrated that accurate predictive modeling of RF-noise in MOSFETs based on pure Nyquist noise is possible down to $\sim$ 100 nm channel lengths, provided that short-channel effects and parasitics are correctly accounted for. When the channel length is decreased further, an additional field-dependent effect must be included in the microscopic noise model. This new model is sufficient to have (almost) predictive noise modeling for the 90-nm node and beyond. We have supported our claim with experimental data from several technology nodes and different foundries [1, 2]. The excess noise model is now publicly available as part of the industry-standard PSP-model [6].

Here, we present a new set of RF-noise data from a 40-nm process from another, independent foundry not yet shown in our previous work, that further establishes the universality of our theory and the accuracy of the PSP noise model. The drain current noise measurements for three different channel lengths are shown in Fig. 1. To enable noise simulations, first a geometry-scaled parameter set was created for the PSP-model to describe the dc-behavior and S-parameters of an n-type RF-MOS device over bias and geometry. The resulting simulations of the conventional, Nyquist-noise based noise model (i.e., PSP without excess noise) are also depicted in Fig. 1. As expected, this gives a good match for the $L = 120$ nm device, but an increasing discrepancy towards shorter devices. In Fig. 2, the same trend is visible (red triangles), but —in addition—it becomes visible that these data quantitatively align with the behavior observed in devices across several foundries and technology nodes. The new data is at the lower end of the spectrum, but the scatter seen in this figure is of the same magnitude that may occur due to differences in noise measurement setup and deembedding method.

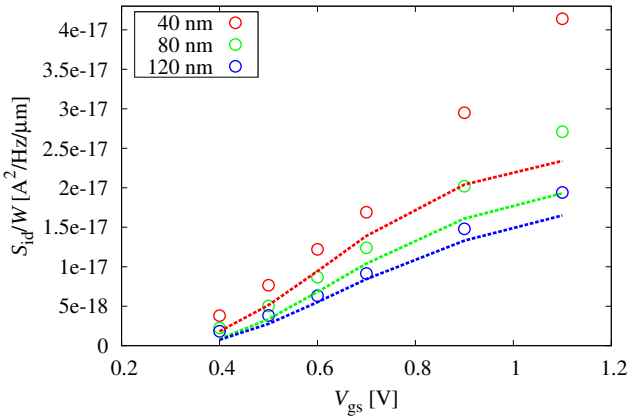

Figure 1: Measured S_{id} versus V_{gs} at $V_{ds} = 1.1$ V from RF devices with various channel lengths in a commercial 40-nm technology (symbols). These data correspond to the first entry in Table 1 and the red triangles in Figs. 2 and 4. PSP noise model (dashed lines) *without* excess noise is also shown.

Invoking the excess noise model in PSP by tuning one single model parameter leads to Fig. 3. Now, both the bias-dependence and the geometry-dependence of observed noise are accurately captured. In addition, as can be seen in Fig. 4, the value of the fitting parameter is consistent with the theoretical predictions in our previous work [1].

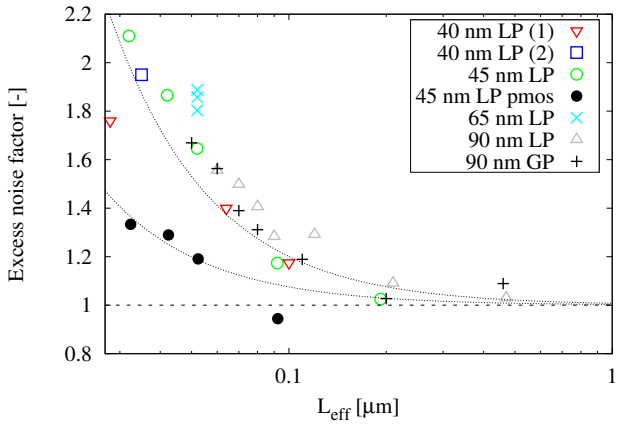

Figure 2: Excess noise factor (i.e., the ratio of the measured S_{id} to the PSP prediction *without* microscopic excess noise) versus effective channel length L_{eff} for five different technologies. The contribution of gate resistance has been removed from the data. The data points were taken at $f = 10$ GHz, V_{ds} at the supply voltage and V_{gs} around or above maximum g_m. Thin dashed lines are a guide to the eye. Horizontal dashed line is PSP prediction *without* microscopic excess noise. More details of the measured devices can be found in Table 1.

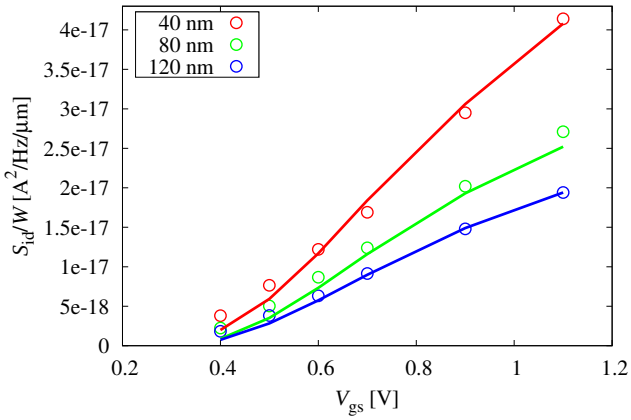

Figure 3: Same measurement data as Fig. 1 (symbols) and PSP noise model *with* excess noise (solid line). This result was obtained by fitting one single model parameter as compared to Fig. 1.

3 Noise model symmetry

3.1 Gummel symmetry

SPICE models used in industry for MOS devices typically contain equations for $V_{ds} \geq 0$ only. When $V_{ds} < 0$, the whole model is mirrored such that the equations for positive drain bias can be reused. It is important but nontrivial to make the model behavior smooth across $V_{ds} = 0$, especially for RF applications. This explains the attention for Gummel symmetry [7] in publications about SPICE models. However, the noise model is usually not taken into account when the model's symmetry is reviewed. Still, it has been observed that discontinuities in the noise spectral density across $V_{ds} = 0$ may cause convergence issues in time-domain noise simulations, demonstrating the importance of Gummel symmetry also for the noise model.

Table 1: Overview of devices, technologies, and foundries in Figs. 2 and 4.

techn. node	foundry	type	#geometries
40 nm LP (1)	A	n	3
40 nm LP (2)	B	n	1
45 nm LP	C	n	5
45 nm LP	C	p	4
65 nm LP	D	n	3
90 nm LP	D	n	7
90 nm GP	D	n	7

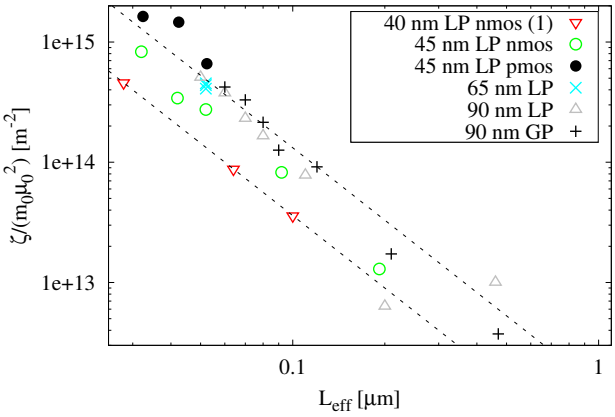

Figure 4: Extracted excess noise parameter versus effective channel length for same technologies and foundries as shown in Fig. 2. Dashed lines show the expected $\propto 1/L_{eff}^2$ scaling trend. More background can be found in Ref. [1].

3.2 Conventional implementation

Any good RF-noise model should include drain current noise, induced gate noise, and their correlation. In order to achieve this, SPICE models are equipped with a number of noise sources, such that at the model terminals the desired noise powers and correlations are observed.

A physics-based method to implement thermal noise is partitioning the channel into segments and placing a noise current source in parallel to each segment. This automatically gives correct modeling of induced gate noise as well as correlation between gate and drain noise. However, SPICE models usually avoid channel segmentation—which lead to additional internal nodes—for reasons of computational efficiency. Instead, a few dedicated noise sources are connected directly to the device terminals and separate equations are provided for their noise spectral density and correlations as a function of bias.

In this paper, we denote the noise currents, spectral densi-

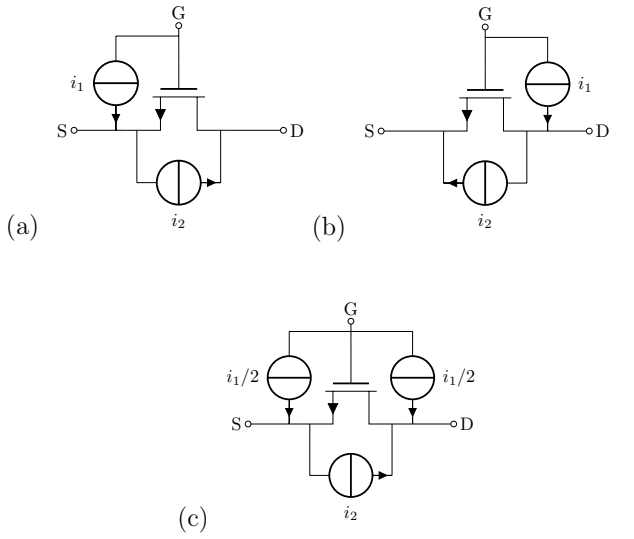

Figure 5: Configuration of noise sources in original model for $V_{ds} > 0$ (a) and $V_{ds} < 0$ (b). In the new model, the configuration is the same for any V_{ds} (c). The model equation for the noise current spectral density $S_1 = \langle i_1 \cdot i_1^* \rangle$ is identical in all cases.

ties, and correlations associated with the *sources in the model* by numbered subscripts (e.g., noise current i_1 with spectral density $S_1 = \langle i_1 \cdot i_1^* \rangle$). Noise currents and spectral power densities observed at the *device terminals* are subscripted with the terminal names (e.g., noise current i_g and spectral density $S_{ig} = \langle i_g \cdot i_g^* \rangle$)

Traditionally, compact MOS models have the noise source(s) that should produce i_g located at the source-side of the device (e.g. BSIM4, BSIM6 [8], MOS Model 11 [9], and older versions of PSP [6]). When $V_{ds} < 0$, this source is moved to the drain-side of the device, in order to keep the model symmetric as described above. This procedure is illustrated in Fig. 5(a,b). However, such an implementation gives rise to a discontinuity at $V_{ds} = 0$ in the observed drain current noise, because of the (dis)appearing contribution of i_1. At low frequency, when S_1 is small, this effect may be negligible. But because $S_1 \propto \omega^2$, beyond a certain frequency we will have $S_1 \gtrsim S_2$ and this contribution starts visibly impacting the noise observed at the source/drain terminals. Indeed, Fig. 6 shows that this discontinuity is clearly visible in the simulated S_{id}. The magnitude of the step will increase quickly with frequency.

3.3 Improved model

This issue can in principle be solved by introducing bias-dependent partitioning of the induced gate noise between drain and source [10], analogous to what is common practice for charges [11].

Here, we take a much simpler approach: we split the induced gate noise *equally* between source and drain, see Fig. 5(c). Fig. 6 shows that this is sufficient to directly remove the discontinuity at $V_{ds} = 0$, without any undesired

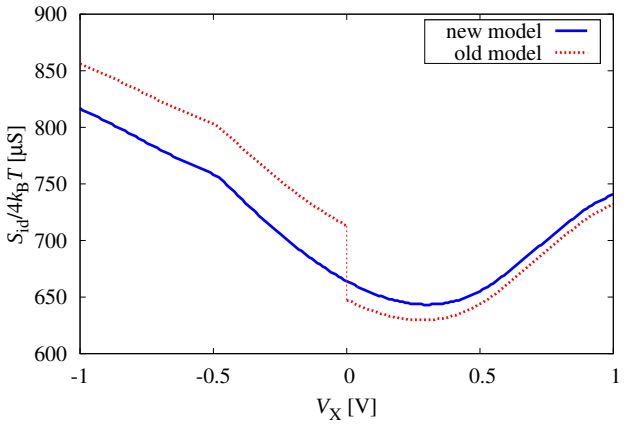

Figure 6: Simulated S_{id} versus V_X. Red dashed curve is the original model (cf. Fig 5(a) and (b)), where the discontinuity at $V_{ds} = 0$ is clearly visible. Blue curve shows new model (cf. Fig 5(c)), where discontinuity at $V_{ds} = 0$ is removed. Here, $V_S = -V_X/2$, $V_D = V_X/2$, while $V_G = 1$ and $V_B = 0$ are fixed. Simulation frequency is chosen such that S_{ig} is just non-negligible w.r.t. S_{id}.

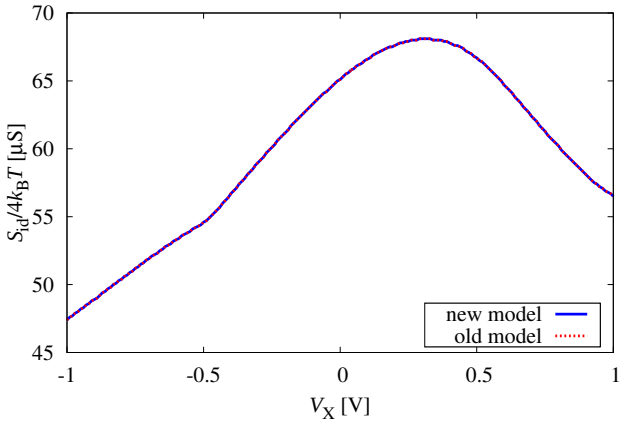

Figure 7: Simulated S_{ig} versus V_X. As intended, for this quantity the original and new model give identical results. Simulation conditions are the same as in Fig. 6.

side-effects on S_{id} simulation results.

Fig. 7 confirms that the new model gives exactly the same simulation results for S_{ig} as the original model. Indeed, if the noise currents of the two sources in Fig. 5(c) are setup to have half the value of the original noise current i_1 and are fully correlated, their combined noise spectral densities at the gate terminal will add up to the original value.

The cross-correlation spectrum $S_{12} = \langle i_1 \cdot i_2 \rangle$ is also kept the same as in the original model. In Fig. 8, it is shown that—as a result—the imaginary part of the correlation coefficient c between i_g and i_d maintains the correct value. Here, c is defined as $S_{igid}/\sqrt{S_{ig} \cdot S_{id}}$, with $S_{igid} = \langle i_g \cdot i_d^* \rangle$. The very small impact of the modified model on $\mathrm{im}(c)$ is entirely caused by its effect on S_{id}. As a side remark, note that $\mathrm{im}(c)$ approaches the theoretical value of ~ 0.4 in saturation. More-

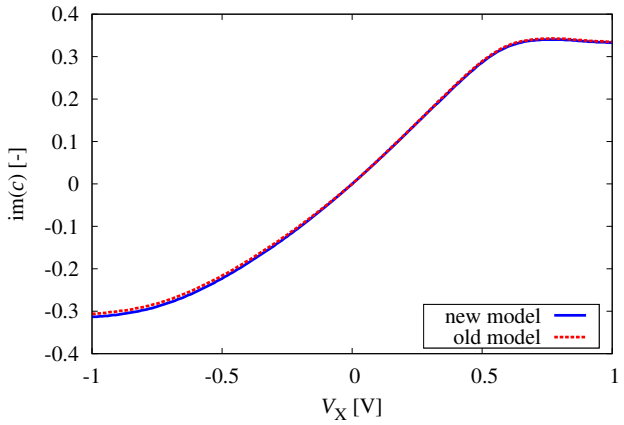

Figure 8: Simulated imaginary part of correlation coefficient $\mathrm{Im}(c)$ versus V_X. The new model approach has virtually no impact on its value. Simulation conditions are the same as in Fig. 6.

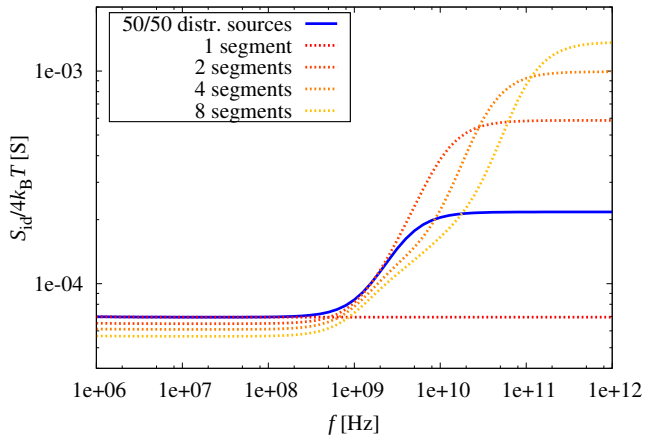

Figure 9: Simulated frequency dependence of S_{id} in our model with 50/50 split of induced gate noise (blue line). For comparison, S_{id} is also shown for a segmented model with various numbers of segments (dashed red/orange lines). The onset of the non-quasi-static effect is correctly captured.

over, it smoothly changes sign at $V_{ds} = 0$, as dictated by basic symmetry principles [12].

The 50/50-split of the gate-noise source between source and drain is very general. It can be used to improve any model that has the noise source on one side only.

This method to improve the noise model has an additional advantage. While in the original model S_{id} has no frequency dependence for $V_{ds} > 0$, in the new model the new i_1-noise source at the drain side will start to affect S_{id} at high frequency. In fact, this behavior is completely physical: the new model correctly captures the onset of non-quasi-static effects in the drain current noise, which would be naturally produced by a segmented noise model. This is demonstrated by Fig. 9, which compares the frequency-dependence of our new model with that of a segmented model.

4 Causality

Next to continuity of noise spectral densities across bias, causality is a strict requirement for enabling time-domain (noise) simulations. It means that complex-valued physical quantities must obey a certain mathematical constraint that connects their real and imaginary part: the Kramers-Kronig relations. Causality is, however, easily violated when directly prescribing the frequency dependence of the noise sources, especially when implementing high-frequency limitation to the induced gate noise.

A natural method to maintain causality in a noise model is to use only white noise sources. Frequency dependence and correlations can be constructed by creating transfers in a passive network of (noiseless) resistors and capacitors and deriving noise currents from that with linear controlled sources. In fact, the popular Verilog-A language [13] enforces such an approach by not allowing direct prescription of user-defined frequency dependencies.

Any noise model which is created in this way (in particular for correlation and high-frequency limiting of S_{ig}) *is* guaranteed to be causal. This method does require additional voltage nodes in the model (two, in case of PSP), which comes with some computational overhead. However, when the exact frequency dependent noise powers derived from this construction are directly implemented in a circuit simulator, causality is maintained (e.g., PSP in SiMKit [6,9])

5 Conclusion

We have presented new measurement data that confirms the accuracy and physical background of our physics-based compact model to describe excess noise in sub-100nm CMOS devices. In addition, we describe a new, generic method to implement RF noise models in a circuit simulator, which is consistent with symmetry and causality requirements for time-domain noise simulations. The method is demonstrated to work in the industry-standard PSP-model.

REFERENCES

[1] G.D.J. Smit, A.J. Scholten, R.M.T. Pijper, L.F. Tiemeijer, R. van der Toorn, D.B.M. Klaassen, "RF-Noise Modeling in Advanced CMOS Technologies", *Trans. Electron Devices*, vol. 61, Feb. 2014.

[2] G.D.J. Smit, A.J. Scholten, R.M.T. Pijper, R. van Langevelde, L.F. Tiemeijer, and D.B. M. Klaassen, "Experimental demonstration and modeling of excess RF Noise in sub-100-nm CMOS technologies," *Electron Device Letters*, vol 31, pp. 884–886, Aug. 2010.

[3] A.J. Scholten *et al.*, "Accurate thermal noise model for deep-submicron CMOS," IEDM '99. Technical Digest., pp. 155–158, 1999.

[4] R. van Langevelde, J.C.J. Paasschens, A.J. Scholten, R.J. Havens, L.F. Tiemeijer, and D.B.M. Klaassen,

"New Compact Model for Induced Gate Current Noise," in *IEDM Tech. Dig.*, 2003, pp. 867-870.
[5] A.J. Scholten, "Modeling and characterization of noise in 90-nm RF CMOS technology," ICNF 2005, AIP Conf. Proc. 780, pp. 735–740, 2005.
[6] [Online:] http://psp.ewi.tudelft.nl
[7] C.C. McAndrew, "Validation of MOSFET model Source& Drain Symmetry", *Trans. Electron Devices*, vol. 53, pp. 2202–2206, Sep. 2006.
[8] [Online:] http://www-device.eecs.berkeley.edu/bsim/
[9] [Online:] http://www.nxp.com/models/simkit
[10] J.C. Ranuárez, M.J. Deen, Chih-Hung Chen, "Modeling the partition of noise from the gate-tunneling current in MOSFETs", *Electron Device Letters*, vol. 26, pp. 550–552, Aug. 2005.
[11] D.E. Ward and R.W. Dutton, "A charge-oriented model for MOS transistor capacitances", *J. Solid-State Circuits*, vol. 13, May 1978.
[12] A.J. Scholten, R. van Langevelde, L.F. Tiemeijer, and D.B.M. Klaassen, "Compact modeling of noise in CMOS", *Custom Integrated Circuits Conference 2006*, pp. 711–716.
[13] [Online:] http://www.designers-guide.org/verilogams/vams231.pdf